RCA Solid State

COS/MOS Integrated Circuits

B-Series Logic
A-Series Logic
Telecommunications
Display Drivers
Interface Devices

RCA COS/MOS Integrated Circuits

This DATABOOK contains complete technical information on RCA standard commercial COS/MOS integrated circuits. It covers the full line of RCA standard A- and B-series digital logic circuits, and special-function circuits (telecommunications and special interface and display driver circuits). An Index to Devices provides a complete listing of types.

The DATABOOK is divided into nine major sections. The first section includes classification and selection charts, functional diagrams, and photographs of available package options. This section is followed by a discussion of general considerations that should be taken into account in the operation and application of COS/MOS integrated circuits.

Three separate data sections provide definitive ratings and characteristics for (1) high-voltage B-series types, (2) A-series types, (3) special-function types.

Data pages for individual devices are included as nearly as possible in alphanumerical sequence of type numbers. Because some devices are grouped together to show similarity of function or data, individual type numbers may be out of sequence. If you don't find the type number you're looking for where you expect it to be, check the Index to Devices.

The data sections are followed by a Dimensional Outlines section, an Application Notes section, and a section that lists RCA Sales Offices, Manufacturers' Representatives, and Authorized Distributors.

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The device data shown for some types are indicated as preliminary or objective. **Preliminary data** are intended for guidance purposes in evaluating devices for equipment design. Such data are shown for types currently being designed for inclusion in our standard line of commercially available products. **Objective data** are intended for engineering evaluation of types in the initial stages of design. The type designations and data are subject to change, unless otherwise arranged. No obligations are assumed for notice of change or future manufacture of these devices. For current information on the status of preliminary or objective programs, please contact your local RCA sales office.

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Index to Devices

This index does not include package designation suffix letters for individual type numbers; the various packages available are shown in the data section.

Index to Application Notes

Product Selection Guides

Product Classification Chart

GATES							MULTIVIBRATORS	
Single-Level				Multi-Level			Flip-Flops/Latches	
NOR/NAND		OR/AND	Buffers & Inverters	Multi-function/AOI	Decoders/ Encoders	Schmitt Trigger		
CD4000B	CD4012B	CD4071B	CD4007UB	CD4019B	CD4028B	CD4093B	CD4013B	CD4096B
CD4000UB	CD4012UB	CD4072B	CD4007A	CD4019A	CD4028A	CD40106B	CD4013A	CD4099B**
CD4000A	CD4012A	CD4073B	CD4009UB	CD4030B ▪	CD4514B		CD4027B	CD4508B
CD4001B	CD4023B	CD4075B	CD4009A	CD4030A ▪	CD4515B		CD4027A	CD4724B**
CD4001UB	CD4023UB	CD4081B	CD4010B	CD4037A	CD4532B		CD4042B	CD40174B
CD4001A	CD4023A	CD4082B	CD4010A	CD4048B	CD4555B*		CD4042A	**Astable/ Monostable**
CD4002B	CD4025B		CD4041UB	CD4048A	CD4556B*		CD4043B	
CD4002UB	CD4025UB		CD4041A	CD4070B▪	CD40147B		CD4043A	
CD4002A	CD4025A		CD4049UB	CD4077B▪			CD4044B	
CD4011B	CD4068B		CD4049A	CD4085B			CD4044A	CD4047B
CD4011UB	CD4078B		CD4050B	CD4086B			CD4076B**	CD4047A
CD4011A	CD40107B		CD4050A				CD4095B	
			CD4069UB					**Monostable**
			CD4502B	▪See Comparators	*See Demultiplexers		**See Storage Registers	CD4098B
			CD4503B					CD4538B
			CD40107B					

REGISTERS			COUNTERS		MULTIPLEXERS/ DEMULTIPLEXERS	PHASE-LOCKED LOOP	QUAD BILATERAL SWITCHES	INTERFACE CIRCUITS
Shift	Storage	FIFO Buffer	Binary Ripple	Synchronous	Analog/Digital Data Selectors			
CD4006B	CD4076B	CD40105B	CD4020B	CD4017B	CD4016B △	CD4046B	CD4016B ◆	CD4009UB
CD4006A	CD4099B		CD4020A	CD4017A	CD4016A △	CD4046A	CD4016A ◆	CD4009A
CD4014B	CD4724B		CD4024B	CD4018B	CD4019B		CD4066B ◆	CD4010B
CD4014A	CD40108B•		CD4024A	CD4018A	CD4019A		CD4066A ◆	CD4010A
CD4015B	CD40208B•		CD4040B	CD4022B	CD4051B			CD4049UB
CD4015A			CD4040A	CD4022A	CD4052B			CD4049A
CD4021B			CD4060B	CD4029B	CD4053B			CD4050B
CD4021A			CD4060A	CD4029A	CD4066B △			CD4050A
CD4031B				CD4059A	CD4066A △			CD40107B
CD4031A •				CD4510B	CD4067B			CD40109B
CD4034B •			**TIMERS**	CD4516B	CD4097B			CD40115 ▽
CD4034A				CD4518B	CD4512B			CD40116 ▽
CD4035B			CD4045B	CD4520B	CD4555B ⊕			
CD4035A			CD4045A	CD40102B	CD4556B ⊕			
CD4062A			CD4536B	CD40103B	CD40257B			
CD4094B				CD40160B				
CD4517B				CD40161B				
CD40100B	•See Multiport Register			CD40162B	△See Quad Bilateral Switch ⊕See Decoders/ Encoders		◆See Multiplexers	
CD40104B				CD40163B				
CD40194B				CD40192B				
				CD40193B				

ARITHMETIC CIRCUITS				DISPLAY DRIVERS			TELECOMMUNICATION CIRCUITS	
Adders/ Comparators	ALU/Rate Multipliers	Parity Generator/ Checker	Multiport Register	With Counter	For LCD* Drive	For LED•• Drive	Crosspoint Switches	Tone Generator
CD4008B	CD4057A	CD40101B	CD40108B*	CD4026B	CD4054B	CD4511B	CD22100 ▽	CD22859 ▽
CD4008A	CD4089B		CD40208B*	CD4026A	CD4055B		CD22101 ▽	
CD4030B +	CD4527B		CD4034B*	CD4033B	CD4056B		CD22102 ▽	
CD4030A +	CD40181B		CD4034A*	CD4033A	CD22104 ▽			
CD4032B	CD40182B			CD40110B	CD22104A ▽			
CD4032A					CD22105 ▽			
CD4038B					CD22105A ▽			
CD4038A								
CD4063B								
CD4070B+	+See Multifunction/AOI		*See Storage Register		*Liquid Crystal Display	••Light Emitting Diode		
CD4077B+								
CD4585B								

▽ Indicates types designed for special applications. Ratings and characteristics data for these types differ in some aspects from the standardized data for A- and B-series types. Refer to RCA data bulletin on these types for specific differences. Data bulletin file numbers are shown on functional diagrams.

Function Selection Chart

Function	Type No.	No. of Pins
Gates		
NOR/NAND		
Dual 4-input NOR	**CD4002B**	14
	CD4002UB	14
	CD4002A	14
Dual 4-input NAND	**CD4012B**	14
	CD4012UB	14
	CD4012A	14
Triple 3-input NOR	**CD4025B**	14
	CD4025UB	14
	CD4025A	14
Triple 3-input NAND	**CD4023B**	14
	CD4023UB	14
	CD4023A	14
Quad 2-input NOR	**CD4001B**	14
	CD4001UB	14
	CD4001A	14
Quad-2 input NAND	**CD4011B**	14
	CD4011UB	14
	CD4011A	14
8-input NOR/OR	**CD4078B**	14
8-input NAND/AND	**CD4068B**	14
Dual 3-input NOR plus inverter	**CD4000B**	14
	CD4000UB	14
	CD4000A	14
Dual 2-input NAND buffer/driver	**CD40107B**	8,14
OR/AND		
Dual 4-input OR	**CD4072B**	14
Dual 4-input AND	**CD4082B**	14
Triple 3-input OR	**CD4075B**	14
Triple 3-input AND	**CD4073B**	14
Quad 2-input OR	**CD4071B**	14
Quad 2-input AND	**CD4081B**	14
Buffers and Inverters		
Dual complementary pair plus inverter	**CD4007UB**	14
	CD4007A	14
Hex inverter	**CD4069UB**	14
Hex inverter/buffer (3-state)	**CD4502B**	16
Hex buffer (3-state non-inverting)	**CD4503B**	16
Hex buffer/converter (inverting)	**CD4009UB**	16
	CD4009A	16
Hex buffer/converter (inverting)	**CD4049UB**	16
	CD4049A	16
Hex buffer/converter (non-inverting)	**CD4010B**	16
	CD4010A	16
Hex buffer/converter (non-inverting)	**CD4050B**	16
	CD4050A	16
Quad true/complement buffer	**CD4041UB**	14
	CD4041A	14
Dual 2-input NAND buffer/driver	**CD40107B**	8,14
Multifunction/AOI		
Triple AND-OR bi-phase pairs	**CD4037A**	14
Quad exclusive-OR	**CD4030B**	14
	CD4030A	14
Quad exclusive-OR	**CD4070B**	14
Quad exclusive-NOR	**CD4077B**	14

Function	Type No.	No. of Pins
Gates (cont'd)		
Multifunction/AOI (cont'd)		
Quad AND/OR Select	**CD4019B**	16
	CD4019A	16
Dual 2-wide, 2-input AND/OR invert (AOI)	**CD4085B**	14
Expandable 4-wide, 2-input AND/OR invert (AOI)	**CD4086B**	14
Multifunctional expandable 8-input (3-state output)	**CD4048B**	16
	CD4048A	16
Decoders/Encoders		
BCD-to-decimal decoder	**CD4028B**	16
	CD4028A	16
8-input priority encoder	**CD4532B**	16
10-line to 4-line BCD priority encoder	**CD40147B**	16
4-bit latch/4-to-16 line decoder (outputs high)	**CD4514B**	24
4-bit latch/4-to-16 line decoder (outputs low)	**CD4515B**	24
Dual 1-of-4 decoder/demultiplexer (outputs high)	**CD4555B**	16
Dual 1-of-4 decoder/demultiplexer (outputs low)	**CD4556B**	16
Schmitt Trigger		
Quad 2-input NAND	**CD4093B**	14
Hex	**CD40106B**	14
Interface		
Quad low-to-high voltage	**CD40109B**	16
Hex high-to-low voltage (inverting)	**CD4009UB**	16
	CD4009A	16
	CD4049UB	16
	CD4049A	16
Hex high-to-low voltage (non-inverting)	**CD4010B**	16
	CD4010A	16
	CD4050B	16
	CD4050A	16
Dual 2-input NAND buffer/driver	**CD40107B**	8,14
8-bit bidirectional CMOS-to-TTL level converter	**CD40115** ▽	22
8-bit bidirectional CMOS-to-TTL level converter	**CD40116** ▽	22
Multivibrators		
Monostable/astable	**CD4047B**	14
	CD4047A	14
Dual monostable	**CD4098B**	16
Dual precision monostable	**CD4538B**	16
Flip-Flops		
Dual "D" with set/reset capability	**CD4013B**	14
	CD4013A	14
Dual "J-K" with set/reset capability	**CD4027B**	16
	CD4027A	16
Gated "J-K" (non-inverting)	**CD4095B**	14
Gated "J-K" (inverting and non-inverting)	**CD4096B**	14

▽ Indicates types designed for special applications. Ratings and characteristics data for these types differ in some aspects from the standardized data for A- and B-series types. Refer to RCA data bulletin on these types for specific differences. Data bulletin file numbers are shown on functional diagrams.

Function Selection Chart

Function	Type No.	No. of Pins
Multivibrators (cont'd)		
Flip-Flops		
Hex "D"	**CD40174B**	16
4-bit "D" with 3-state outputs	**CD4076B**	14
Latches		
Quad clocked "D"	**CD4042B**	16
	CD4042A	16
Quad NOR R/S (3-state outputs)	**CD4043B**	16
	CD4043A	16
Quad NAND R/S (3-state outputs)	**CD4044B**	16
	CD4044A	16
Dual 4-bit	**CD4508B**	24
8-bit addressable	**CD4099B**	16
	CD4724B	16
Registers		
Shift Registers-Static		
Dual 4-stage with serial input/parallel output	**CD4015B**	16
	CD4015A	16
18-stage	**CD4006B**	14
	CD4006A	14
64-stage	**CD4031B**	16
	CD4031A	16
Dual 64-bit	**CD4517B**	16
8-stage with synchronous parallel or serial input/serial output	**CD4014B**	16
	CD4014A	16
8-stage with asynchronous parallel input or synchronous serial input/serial output	**CD4021B**	16
	CD4021A	16
4-stage parallel-in/parallel-out with J-K input and true/complement output	**CD4035B**	16
	CD4035A	16
4-bit universal bidirectional with 3-state outputs	**CD40104B**	16
4-bit universal bidirectional with asynchronous master reset	**CD40194B**	16
8-stage bidirectional parallel or serial input/parallel output	**CD4034B**	24
	CD4034A	24
32-bit left/right	**CD40100B**	16
8-stage shift-and-store bus	**CD4094B**	16
Shift Registers-Dynamic		
200-stage	**CD4062A**	12
Storage Registers		
8-bit addressable latch	**CD4099B**	16
	CD4724B	16
4-bit "D"-type with 3-state outputs	**CD4076B**	16
4 X 4 Multiport	**CD40108B**	24
4 X 4 Multiport	**CD40208B**	24
FIFO Buffer Registers		
4-bit X 16 word	**CD40105B**	16
Counters		
Binary Ripple		
7-stage	**CD4024B**	14
	CD4024A	14
12-stage	**CD4040B**	16
	CD4040A	16
14-stage	**CD4020B**	16
	CD4020A	16
Counters (cont'd)		
Binary Ripple		
14-stage counter/divider and oscillator	**CD4060B**	16
	CD4060A	16
Timers		
21-stage	**CD4045B**	14
	CD4045A	14
Programmable	**CD4536B**	16
Synchronous		
Decade counter/divider plus 10 decoded decimal outputs	**CD4017B**	16
	CD4017A	16
Divide-by-8 counter/divider with 8 decimal outputs	**CD4022B**	16
	CD4022A	16
Presettable divide-by-"N" counter, fixed or programmable	**CD4018B**	16
	CD4018A	16
Programmable-divide-by-"N" counter	**CD4059A**	24
Presettable up/down counter, binary or BCD-decade	**CD4029B**	16
	CD4029A	16
Presettable 4-bit BCD up/down counter	**CD4510B**	16
Presettable 4-bit binary up/down counter	**CD4516B**	16
Presettable 2-decade BCD down counter	**CD40102B**	16
Presettable 8-bit binary down counter	**CD40103B**	16
Presettable 4-bit BCD up/down counter	**CD40192B**	16
Presettable 4-bit binary up/down counter	**CD40193B**	16
Dual BCD up counter	**CD4518B**	16
Dual binary up counter	**CD4520B**	16
Decade counter/asynchronous clear	**CD40160B**	16
Binary counter/asynchronous clear	**CD40161B**	16
Decade counter/synchronous clear	**CD40162B**	16
Binary counter/synchronous clear	**CD40163B**	16
Display Drivers		
With Counter		
Decade counter/divider with 7-segment display outputs and display enable	**CD4026B**	16
	CD4026A	16
Decade counter/divider with 7-segment display outputs and ripple blanking	**CD4033B**	16
	CD4033A	16
Up/Down Counter-Latch-Decoder-Driver	**CD40110B**	16
For Liquid-Crystal-Display Drive		
4-segment display driver	**CD4054B**	16
BCD-to-7-segment decoder/driver with "display-frequency" output	**CD4055B**	16
BCD-to-7-segment decoder/driver with strobed-latch function	**CD4056B**	16
4-digit decoder/driver with hexidecimal display	**CD22104**▽	40

Function	Type No.	No. of Pins
Display Drivers (cont'd)		
For Liquid-Crystal-Display Drive		
4-digit decoder/driver with decimal display	CD22104A ∇	40
4-digit decoder/driver with hexidecimal display	CD22105 ∇	40
4-digit decoder/driver with decimal display	CD22105A ∇	40
For Light-Emitting-Diode Drive		
BCD-to-7-segment latch decoder/driver	CD4511B	16
Multiplexers/Demultiplexers		
Analog		
Triple 2-channel	CD4053B	16
Differential 4-channel	CD4052B	16
Single 8-channel	CD4051B	16
Differential 8-channel	CD4097B	24
Single 16-channel	CD4067B	24
Quad bilateral switch	CD4016B	14
	CD4016A	14
Quad bilateral switch	CD4066B	14
	CD4066A	14
Digital (Data Selectors)		
Quad AND/OR select	CD4019B	16
	CD4019A	16
Dual 1-of-4 decoder/demultiplexer (outputs high)	CD4555B	16
Dual 1-of-4 decoder/demultiplexer (outputs low)	CD4556B	16
Quad 2-line-to-1-line	CD40257B	16
8-channel	CD4512B	16
Phase-Locked Loop		
Micropower	CD4046B	16
	CD4046A	16
Arithmetic Circuits		
Adders/Comparators		
4-bit full adder with parallel carry out	CD4008B	16
	CD4008A	16
Triple serial adder, positive logic	CD4032B	16
	CD4032A	16

Function	Type No.	No. of Pins
Arithmetic Circuits (Cont'd)		
Adders/Comparators		
Triple serial adder, negative logic	CD4038B	16
	CD4038A	16
4-bit magnitude comparator	CD4063B	16
	CD4585B	16
Quad exclusive-OR gate	CD4030B	14
	CD4030A	14
Quad exclusive-OR gate	CD4070B	14
Quad exclusive-NOR gate	CD4077B	14
ALU/Rate Multipliers		
4-bit arithmetic logic unit	CD40181B	24
	CD4057A	28
BCD rate multiplier	CD4527B	16
Binary rate multiplier	CD4089B	16
Look-ahead-carry block	CD40182B	16
Parity Generator/Checker		
9-bit	CD40101B	14
Multiport Register		
4 X 4	CD40108B	24
4 X 4	CD40208B	24
8 X 1	CD4034B	24
8 X 1	CD4034A	24
Quad Bilateral Switches		
For transmission or multiplexing of analog or digital signals	CD4016B	14
	CD4016A	14
	CD4066B	14
	CD4066A	14
Telecommunication Circuits		
Crosspoint Switches		
4 X 4 crosspoint switch with control memory	CD22100 ∇	16
4 X 4 X 2 crosspoint switch with control memory	CD22101 ∇	24
4 X 4 X 2 crosspoint switch with control memory	CD22102 ∇	24
Tone Generator		
Dual-tone multifrequency tone generator	CD22859 ∇	16

∇ Indicates types designed for special applications. Ratings and characteristics data for these types differ in some aspects from the standardized data for A- and B-series types. Refer to RCA data bulletin on these types for specific differences. Data bulletin file numbers are shown on functional diagrams.

COS/MOS Microprocessor, Memory, and Timekeeping Circuits

In addition to the logic and special-function integrated circuits listed in the preceding pages, RCA also offers a comprehensive and expanding line of COS/MOS microprocessor, memory, and timekeeping integrated circuits.

The microprocessor and memory circuits include central-processing units (CPU's), custom and standard read-only memories (ROM's), programmable read-only memories (PROM's), random-access memories (RAM's), general-purpose memories, system expanders, input/output

COS/MOS Microprocessor and Memory Products

		No. of Pins
Microprocessors		
CDP1802	COSMAC 8-Bit CPU	40
CDP1804	COSMAC 8-Bit Microcomputer	40
Standard ROM's (Firmware)		
CDPR512	UT4 Utility Program	24
CDPR522	Microterminal Controller	24
CDPR582	Fixed-Point Arithmetic	24
Custom ROM's (Mask Programmable)		
CDP1831	512×8	24
CDP1832	512×8	24
CDP1833	1024×8	24
CDP1834	1024×8	24
EPROM's		
CDP18U42	256×8 UV Erasable	24
RAM's		
CD4036A	4×8	24
CD4039A	4×8	24
CD4061A	256×1	16
CD40061A	256×1	16
CD40114B	16×4	16
CDP1821	1024×1	16
CDP1822	256×4	22
CDP1823	128×8	24
CDP1824	32×8	18
CDP1825	1024×4	18
MWS5101	256×4	22
MWS5114	1024×4	18
System Expanders		
CDP1856	4-Bit Bus Buffer (For Memory)	16
CDP1857	4-Bit Bus Buffer (For I/O)	16
CDP1858	4-Bit Latch/Decoder (256×4 Memory)	16
CDP1859	4-Bit Latch/Decoder (1K×1 Memory)	16
CDP1866	4-Bit Latch/Decoder (1K×4 Memory)	18
CDP1867	4-Bit Latch/Decoder (4K×1 Memory	18
CDP1868	4-Bit Latch/Decoder (1K×4 Memory, Latched Chip Enable)	18
General-Purpose I/O		
CDP1851	Programmable I/O (20 Lines)	40
CDP1852	Byte-Wide I/O (8 Lines)	24
CDP1853	N Line Decoder	16
CDP1854A	UART	40
CDP1855	Multiply-Divide Unit	28
General-Purpose I/O		
CDP1856	4-Bit Bus Buffer (For Memory)	16
CDP1857	4-Bit Bus Buffer (For I/O)	16
CDP1858	4-Bit Latch/Decoder (256×4 Memory)	16
CDP1859	4-Bit Latch/Decoder (1K×1 Memory)	16
CDP1863	Programmable Frequency Generator	16
CDP1866	4-Bit Latch/Decoder (1K×4 Memory)	18
CDP1867	4-Bit Latch/Decoder (4K×1 Memory)	18
CDP1868	4-Bit Latch/Decoder (1K×4 Memory, Latched Chip Enable)	18
CDP1872	High-Speed 8-Bit Input Port (1873 Compatible)	22
CDP1873	High-Speed 1 of 8 Decoder (8205 Pinout)	16
CDP1874	High-Speed 8-Bit Input Port (1853 Compatible)	22
CDP1875	High-Speed 8-Bit Output Port	22
Special-Purpose I/O		
CDP1861	Video Display Controller	24
CDP1862	Color Generator Controller	24
CDP1864	PAL Video Controller	40
CDP1869	VIS Address Plus Sound Generator	40
CDP1870	VIS Color Video Generator	40
CDP1871	VIS Compatible Keyboard Encoder	40
CDP1876	VIS Color Video Generator (RGB Bondout)	40
COSMAC Microboard Computer Systems		
Single-Board Computers		
Memory Boards		
I/O Expansion Boards		
Prototyping Systems		
System Development Aids		
COSMAC Development and Support Systems		
Development, Prototyping and Evaluation Systems		
System Support Components		
System Support Software		
System Support Modules		

(I/O) circuits, COSMAC microboard computer systems and COSMAC development and support systems.

For descriptive information on RCA microprocessor and memory circuits, refer to the RCA "COSMAC Microprocessor Product Guide", MPG-108B; to the RCA technical data bulletins on specific types; or to the RCA DATABOOK "COS/MOS Memories, Microprocessors, and Support Systems", SSD-260.

The timekeeping circuits include standard "off-the-shelf" circuits for watches and auto clocks. Plus a custom design capability to tailor these products to meet specific requirements. The watch products include LCD display circuits from 3½ to 6 digits and from 5 to 6 functions with additional features such as stopwatch and alarm. The auto clocks are stepping-motor-drive clock circuits, 2-, 3-, and 4-MHz crystal-operated.

For descriptive information on RCA timekeeping circuits, refer to the RCA technical data bulletins on specific types.

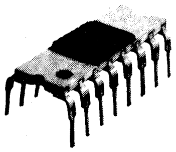
COS/MOS Timekeeping Products

Function	Type No.	No. of Pins
Timekeeping		
Watches		
3½ Digit		
5 function LCD watch with stopwatch	CD22003	Chip
4 Digit		
6 function LCD watch with alarm	CD22007V2	Chip
6 Digit		
6 function LCD watch with stopwatch	CD22008V1	Chip
6 function LCD watch with alarm	CD22018	Chip
Auto Clocks		
Quartz analog auto clock (0.5-Hz push-pull)	CD22012	14
Quartz analog auto clock (60-Hz)	CD22014	8
Quartz analog auto clock (30-Hz push-pull)	CD22015	12

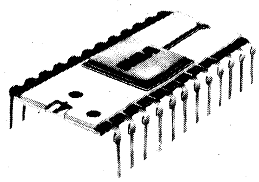
COS/MOS IC Packages

Packages

D Suffix
Ceramic Dual-In-Line Packages

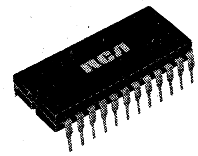


Welded-Seal 14,16,24, and 28-lead Versions



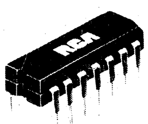
22, 40-Lead Side-Brazed Versions

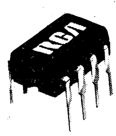
F Suffix
Frit-Seal Ceramic Dual-In-Line Packages



14,16, and 24-lead Versions

E Suffix
Plastic Dual-In-Line Packages

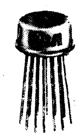




MiniDIP

8,14,16,18,22,24, and 40-lead Versions

T Suffix
12-Lead TO-5 Style Package



CD4024A and CD4062A only

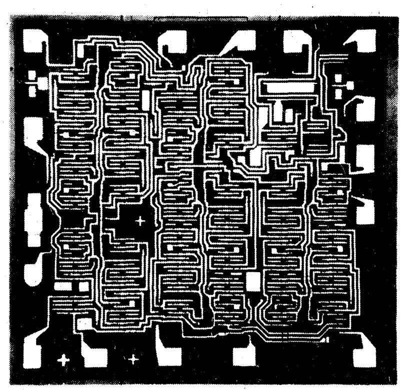
Ordering Information

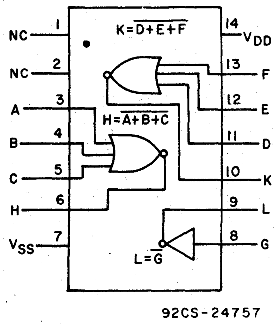
Most RCA COS/MOS integrated circuits are available in the following package styles and are identified by the Suffix Letters indicated below: dual-in-line ceramic, dual-in-line frit-seal ceramic, dual-in-line plastic, and in chip form. Some types are only available in one or two package styles. The available package styles for any specific type are given in the technical data for that type.

When ordering COS/MOS devices, it is important that the appropriate suffix letter be affixed to the type number of the device required. For example, a CD4016B in a dual-in-line ceramic package will be identified as the CD4016BD.

Package	Suffix Letters
Dual-In-Line Welded-Seal or Side-Brazed Ceramic	D
Dual-In-Line Frit-Seal Ceramic	F
Dual-In-Line Plastic	E
TO-5 Style	T
Chip	H

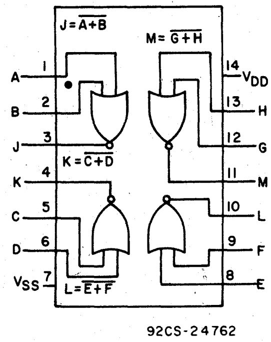
H Suffix
COS/MOS Chip





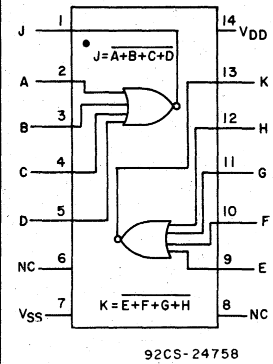
Dual 3-Input NOR Gate Plus Inverter

CD4000A	(Page 442)
CD4000B	(Page 50)
CD4000UB	(Page 54)



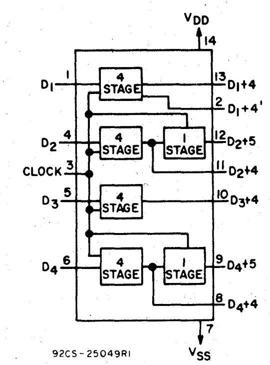
Quad 2-Input NOR Gate

CD4001A	(Page 442)
CD4001B	(Page 50)
CD4001UB	(Page 54)



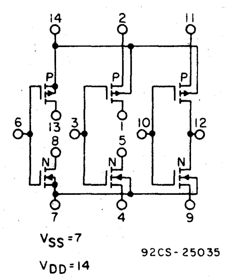
Quad 4-Input NOR Gate

CD4002A	(Page 442)
CD4002B	(Page 50)
CD4002UB	(Page 54)



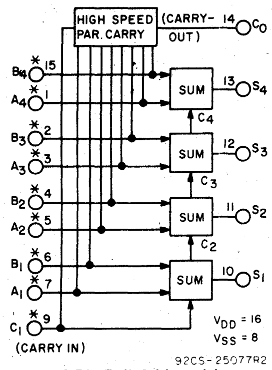
18-Stage Static Shift Register

CD4006A	(Page 445)
CD4006B	(Page 58)



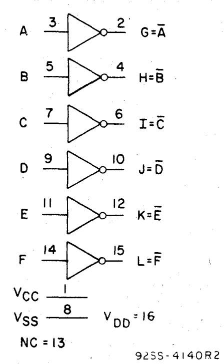
Dual Complementary Pair Plus Inverter

CD4007A	(Page 448)
CD4007UB	(Page 62)



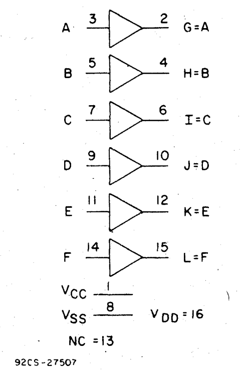
4-Bit Full Adder with Parallel Carry Out

CD4008A	(Page 451)
CD4008B	(Page 66)



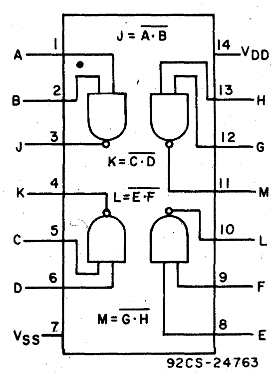
Hex Buffer/Converter Inverting Type

CD4009A	(Page 453)
CD4009UB	(Page 70)



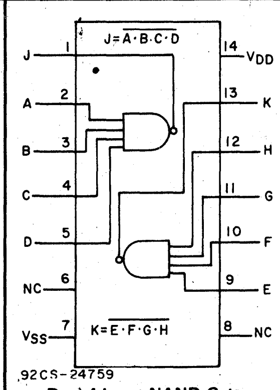
Hex Buffer/Converter Non-Inverting Type

CD4010A	(Page 453)
CD4010B	(Page 70)



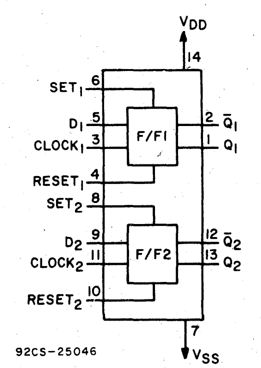
Quad 2-Input NAND Gate

CD4011A	(Page 456)
CD4011B	(Page 74)
CD4011UB	(Page 78)



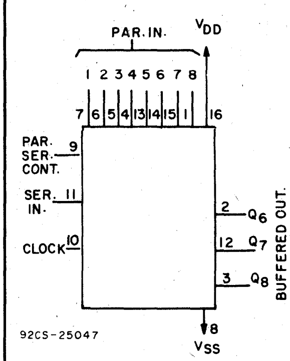
Dual 4-Input NAND Gate

CD4012A	(Page 456)
CD4012B	(Page 74)
CD4012UB	(Page 78)



Dual "D" Flip-Flop with Set/Reset Capability

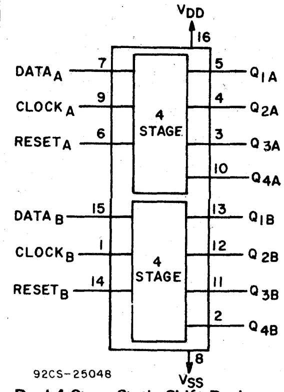
CD4013A	(Page 459)
CD4013B	(Page 82)



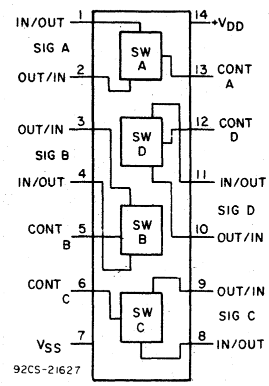
8-Stage Synchronous Shift Register with Parallel or Serial Input/Serial Output

CD4014A	(Page 462)
CD4014B	(Page 86)

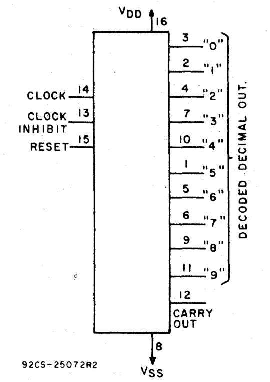
Functional Diagrams



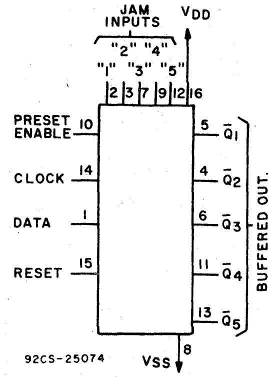
Dual 4-Stage Static Shift Register with Serial Input/Parallel Output
CD4015A (Page 464)
CD4015B (Page 91)



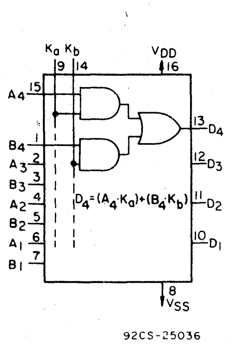
Quad Bilateral Switch
CD4016A (Page 324)
CD4016B (Page 95)



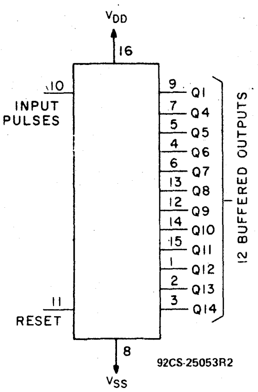
Decade Counter/Divider with 10 Decoded Decimal Outputs
CD4017A (Page 471)
CD4017B (Page 100)



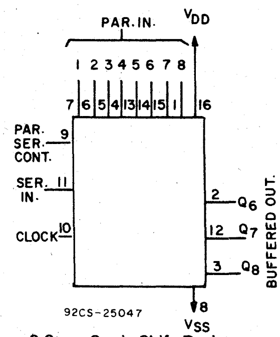
Presettable Divide-by-"N" Counter Fixed or Programmable
CD4018A (Page 475)
CD4018B (Page 105)



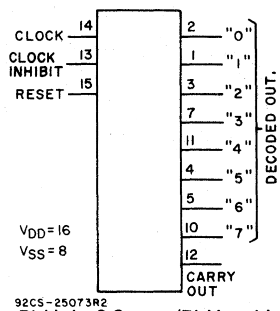
Quad AND/OR Select Gate
CD4019A (Page 478)
CD4019B (Page 110)



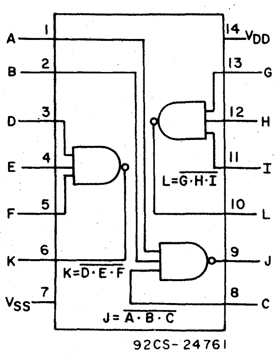
14-Stage Binary Ripple Counter
CD4020 (Page 480)
CD4020B (Page 114)



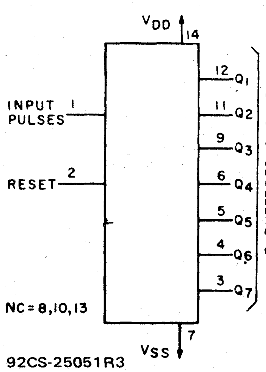
8-Stage Static Shift Register Asynchronous Parallel or Synchronous Serial Input/ Serial Output
CD4021A (Page 483)
CD4021B (Page 86)



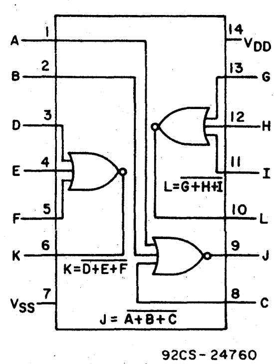
Divide-by-8 Counter/Divider with 8 Decoded Decimal Outputs
CD4022A (Page 486)
CD4022B (Page 100)



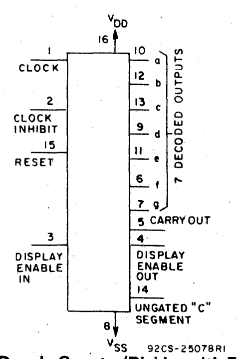
Triple 3-Input NAND Gate
CD4023A (Page 456)
CD4023B (page 74)
CD4023UB (Page 78)



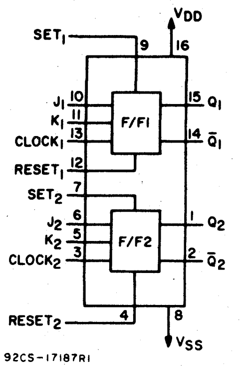
7-Stage Ripple-Carry Binary Counter/Divider
CD4024A (Page 489)
CD4024B (Page 114)



Triple 3-Input NOR Gate
CD4025A (Page 442)
CD4025B (Page 50)
CD4025UB (Page 54)

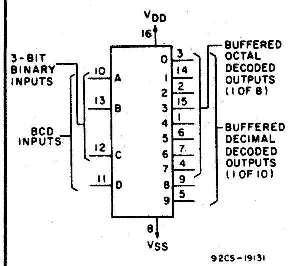


Decade Counter/Divider with 7-Segment Display Outputs and Display Enable
CD4026A (Page 492)
CD4026B (Page 118)



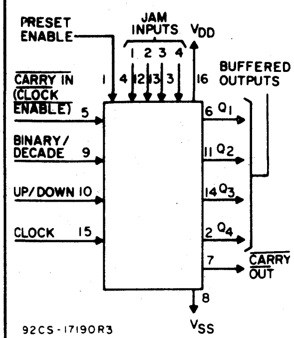
Dual J-K Master-Slave Flip-Flop with Set-Reset Capability

CD4027A (Page 496)
CD4027B (Page 124)



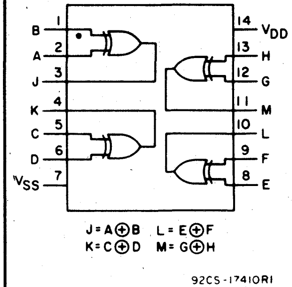
BCD-to-Decimal Decoder

CD4028A (Page 499)
CD4028B (Page 128)



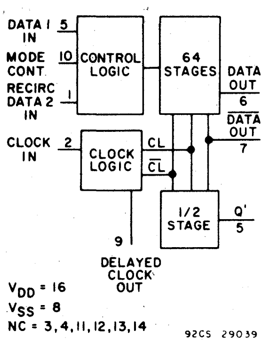
Presettable Up/Down Counter, Binary or BCD-Decade

CD4029A (Page 502)
CD4029B (Page 132)



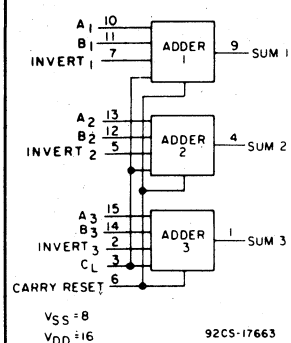
Quad Exclusive-OR Gate

CD4030A (Page 505)
CD4030B (Page 138)



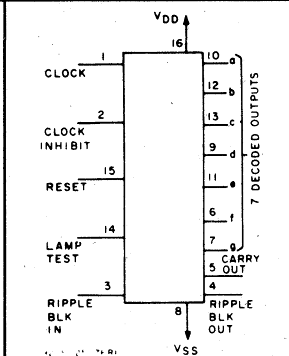
64-Stage Static Shift Register

CD4031A (Page 507)
CD4031B (Page 141)



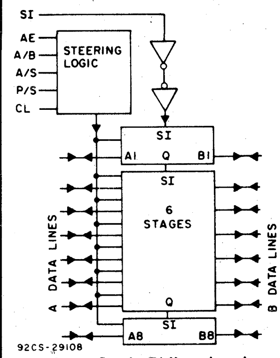
Triple Serial Adder Positive Logic

CD4032A (Page 510)
CD4032B (Page 146)



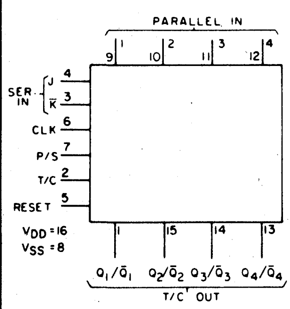
Decade Counter/Divider with 7-Segment Display Outputs and Ripple Blanking

CD4033A (Page 492)
CD4033B (Page 118)



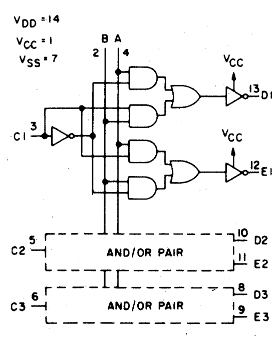
8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register

CD4034A (Page 513)
CD4034B (Page 150)



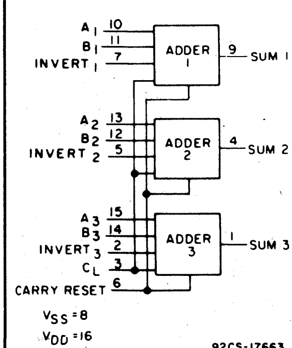
4-Stage Parallel In/Parallel Out Shift Register with J-K Serial Inputs and True/Complement Outputs

CD4035A (Page 517)
CD4035B (Page 156)



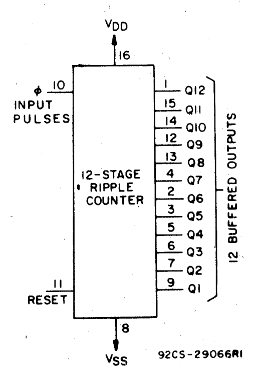
Triple AND/OR Bi-Phase Pair

CD4037A (Page 520)



Triple Serial Adder Negative Logic

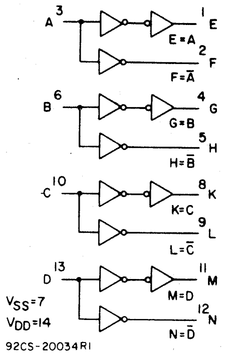
CD4038A (Page 510)
CD4038B (Page 146)



12-Stage Ripple-Carry Binary Counter/Divider

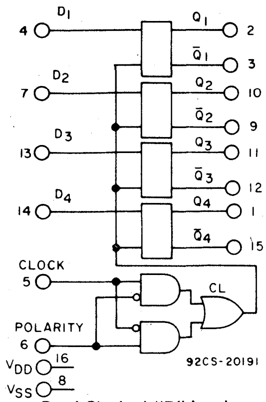
CD4040A (Page 522)
CD4040B (Page 114)

Functional Diagrams



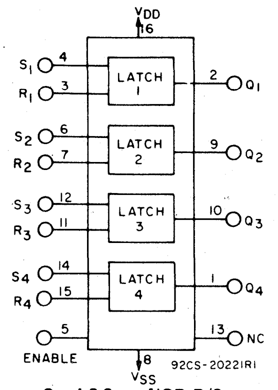
Quad True/Complement Buffer

CD4041A (Page 525)
CD4041UB (Page 161)



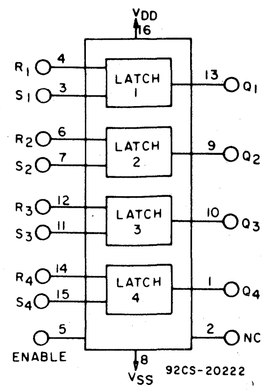
Quad Clocked "D" Latch

CD4042A (Page 529)
CD4042B (Page 164)



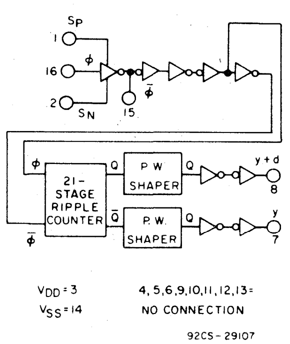
Quad 3-State NOR R/S Latch

CD4043A (Page 532)
CD4043B (Page 168)



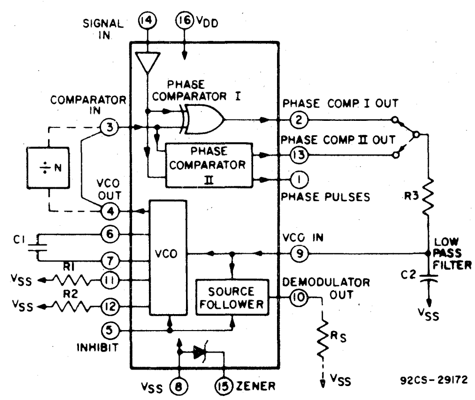
Quad 3-State NAND R/S Latch

CD4044A (Page 532)
CD4044B (Page 168)



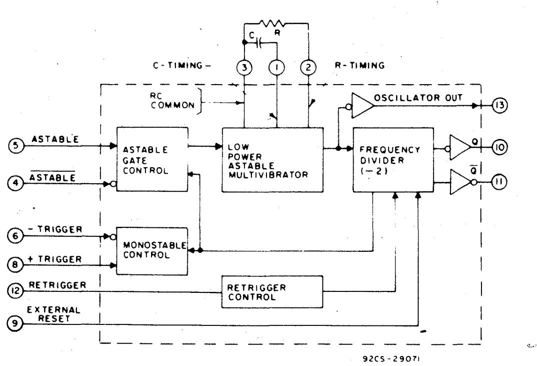
21-Stage Counter

CD4045A (Page 535)
CD4045B (Page 172)



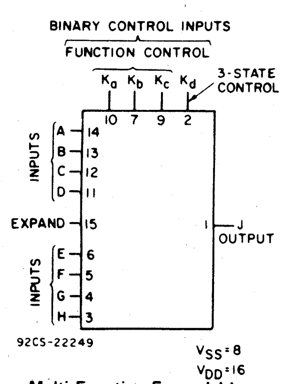
Micropower Phase-Locked Loop

CD4046A (Page 538)
CD4046B (Page 176)



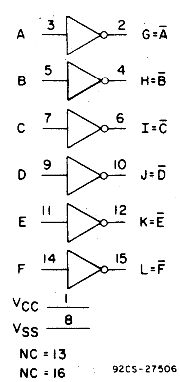
Low-Power Monostable/Astable Multivibrator

CD4047A (Page 543)
CD4047B (Page 182)



Multi-Function Expandable 8-Input Gate

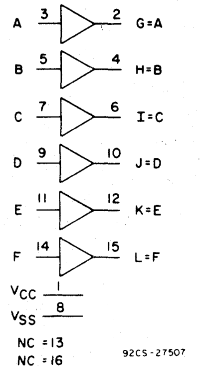
CD4048A (Page 549)
CD4048B (Page 189)



Hex Buffer/Converter Inverting Type

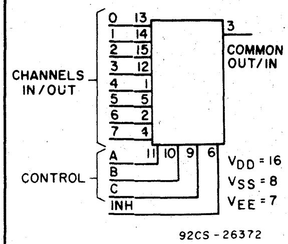
CD4049A (Page 554)
CD4049UB (Page 194)

Functional Diagrams



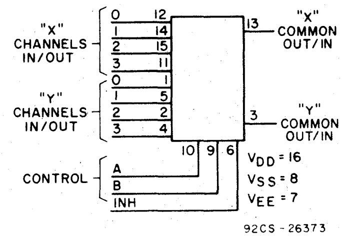
Hex Buffer/Converter Non-Inverting Type

CD4050A (Page 554)
CD4050B (Page 194)



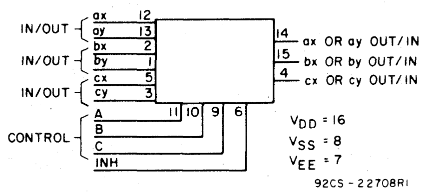
Single 8-Channel Analog Multiplexer/Demultiplexer

CD4051B (Page 198)



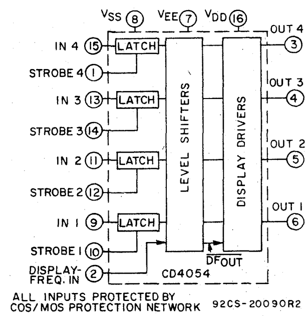
Differential 4-Channel Analog Multiplexer/Demultiplexer

CD4052B (Page 198)



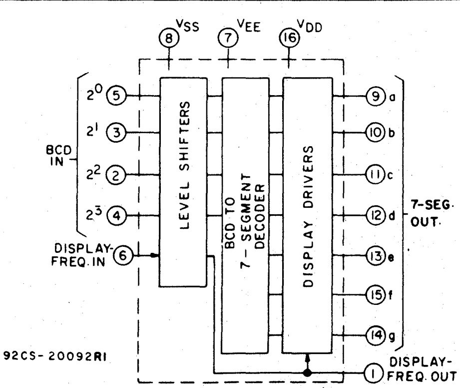
Triple 2-Channel Multiplexer/Demultiplexer

CD4053B (Page 198)



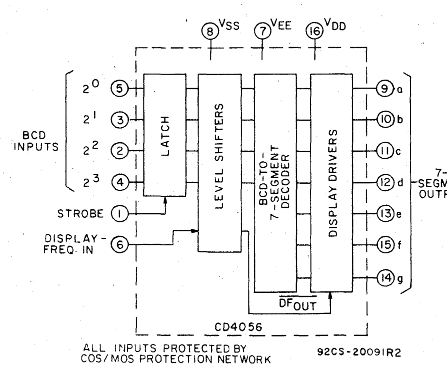
4-Segment Liquid-Crystal Display Driver

CD4054B (Page 205)



BCD-to-7-Segment Decoder/Driver with "Display-Frequency" Output Liquid-Crystal Display Driver

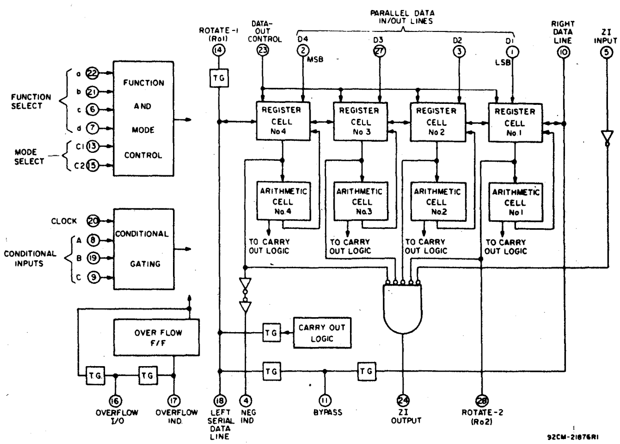
CD4055B (Page 205)



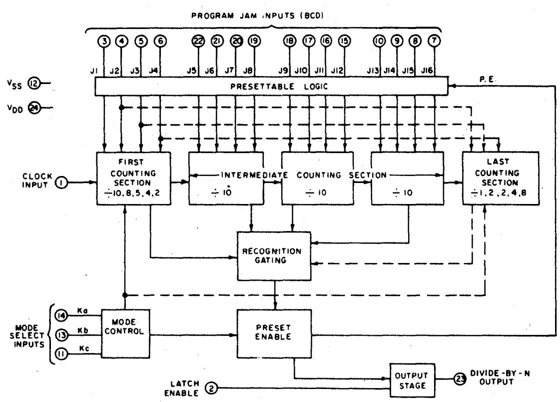
BCD-to-7-Segment Decoder/Driver with Strobed-Latch Function Liquid-Crystal Display Driver

CD4056B (Page 205)

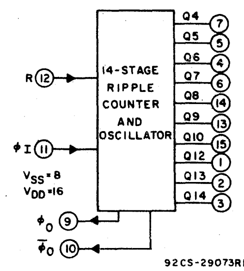
Functional Diagrams



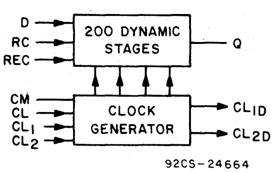
4-Bit Arithmetic Logic Unit
CD4057A (page 557)



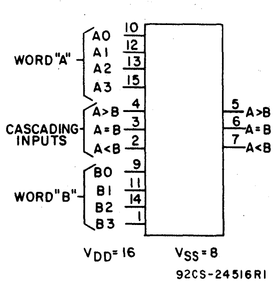
Programmable Divide-by-"N" Counter
CD4059A (Page 565)



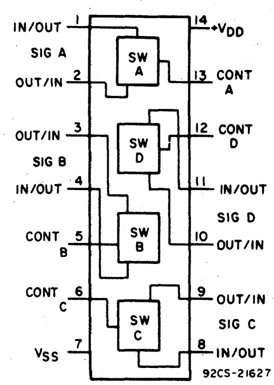
14-Stage Ripple-Carry Binary Counter/Divider and Oscillator
CD4060A (Page 573)
CD4060B (Page 210)



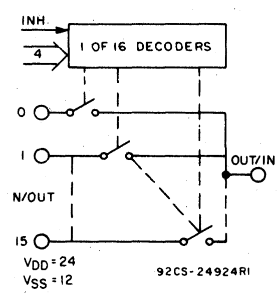
200-Stage Dynamic Shift Register
CD4062A (Page 576)



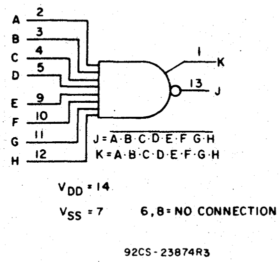
4-Bit Magnitude Comparator
CD4063B (Page 214)



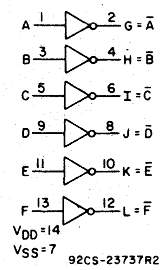
Quad Bilateral Switch
CD4066A (Page 580)
CD4066B (Page 218)



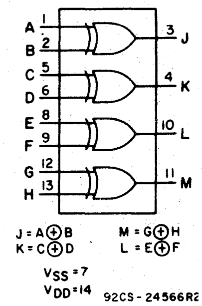
16-Channel Multiplexer/Demultiplexer
CD4067B (Page 223)



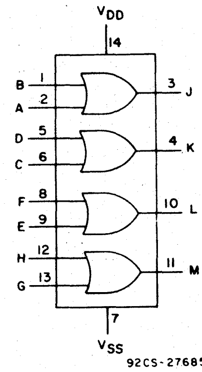
8-Input NAND/AND Gate
CD4068B (Page 229)



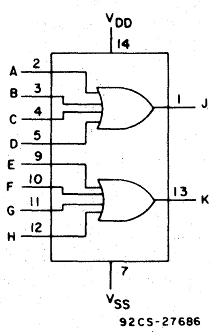
Hex Inverter
CD4069UB (Page 232)



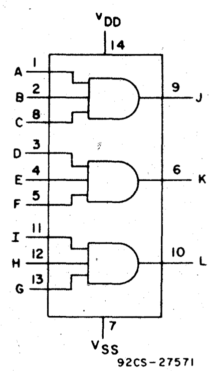
Quad Exclusive-OR Gate
CD4070B (Page 235)



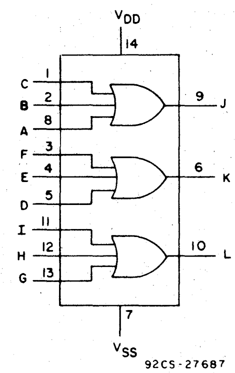
Quad 2-Input OR Gate
CD4071B (Page 238)



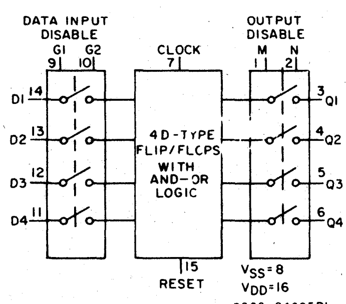
Dual 4-Input OR Gate
CD4072B (Page 238)



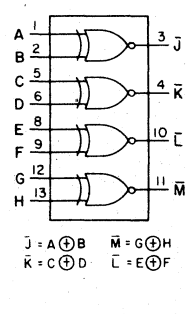
Triple 3-Input AND Gate
CD4073B (Page 242)



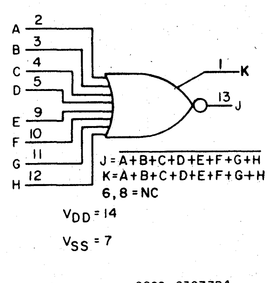
Triple 3-Input OR Gate
CD4075B (page 238)



4-Bit D-Type Register
CD4076B (Page 246)

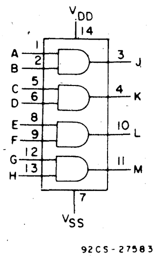


Quad Exclusive-NOR Gate
CD4077B (Page 235)



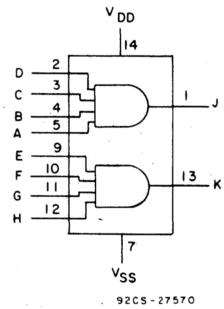
8-Input NOR/OR Gate
CD4078B (Page 250)

Functional Diagrams



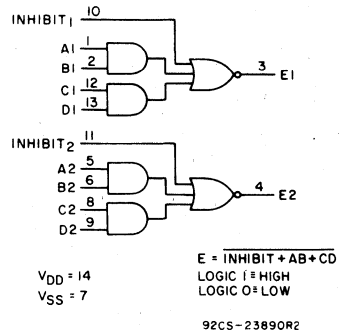
Quad 2-Input AND Gate

CD4081B (Page 242)



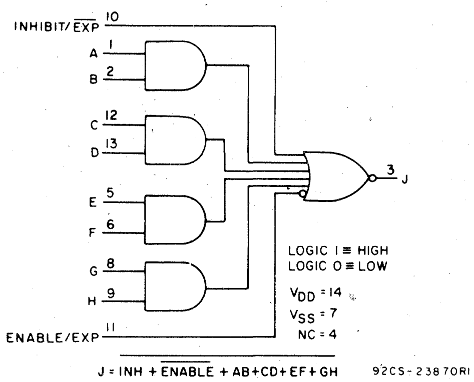
Dual 4-Input AND Gate

CD4082B (Page 242)



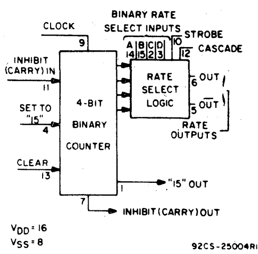
Dual 2-Wide, 2-Input AND-OR-INVERT (AOI) Gate

CD4085B (Page 253)



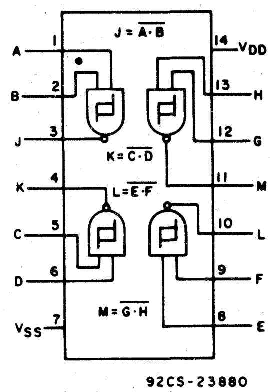
Expandable 4-Wide, 2-Input AND-OR-INVERT (AOI) Gate

CD4086B (Page 257)



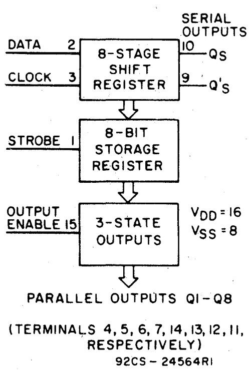
Binary Rate Multiplier

CD4089B (Page 261)



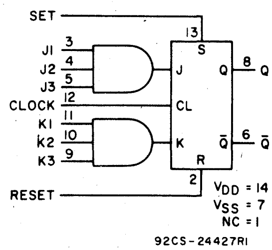
Quad 2-Input NAND Schmitt Trigger

CD4093B (Page 266)



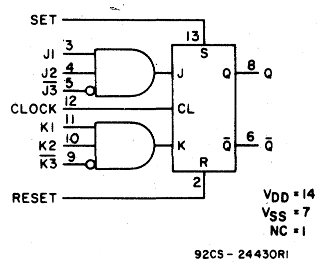
8-Stage Shift-and-Store Bus Register

CD4094B (Page 270)



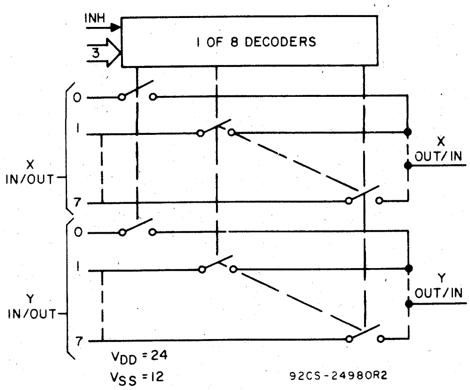
Gated J-K Master-Slave Flip-Flop, Non-Inverting Inputs

CD4095B (Page 274)



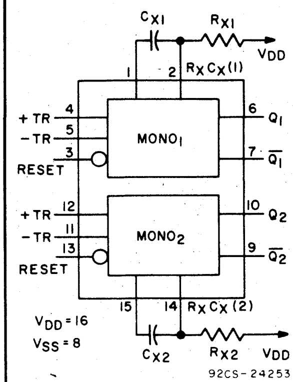
Gated J-K Master-Slave Flip-Flop, Inverting and Non-Inverting Inputs

CD4096B (Page 274)



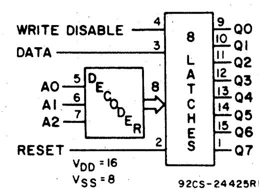
Differential 8-Channel Multiplexer/Demultiplexer

CD4097B (Page 223)



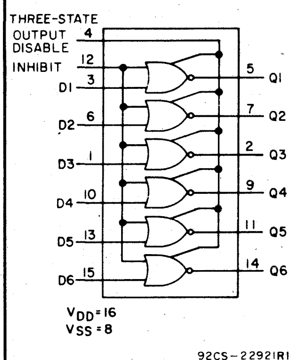
Dual Monostable Multivibrator

CD4098B (Page 278)



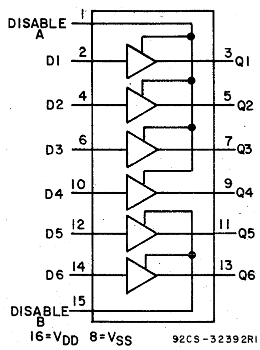
8-Bit Addressable Latch

CD4099B (Page 283)



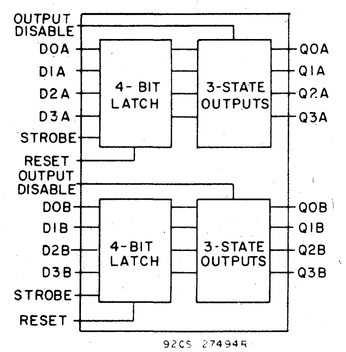
Strobed Hex Inverter/Buffer

CD4502B (Page 287)



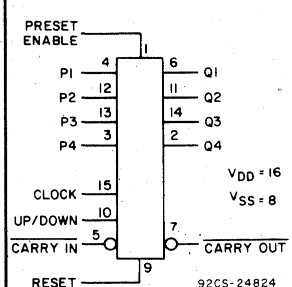
Hex Buffer 3-State Non-Inverting

CD4503B (Page 290)



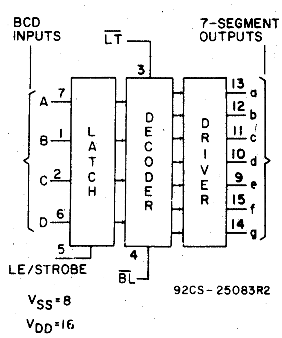
Dual 4-Bit Latch

CD4508B (Page 293)



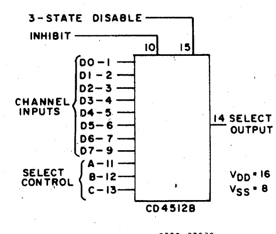
BCD Presettable Up/Down Counter

CD4510B (Page 297)



BCD-to-7-Segment Latch Decoder Driver

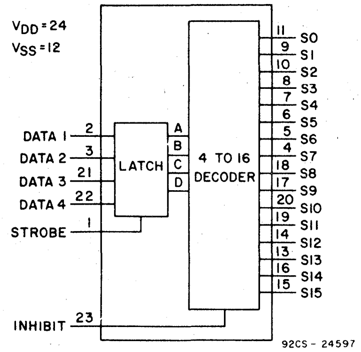
CD4511B (Page 302)



8-Channel Data Selector

CD4512B (Page 307)

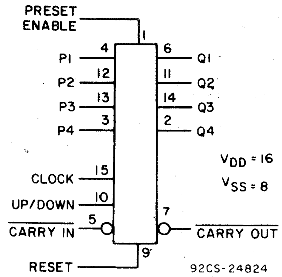
Functional Diagrams



4-Bit Latch/4-to-16 Line Decoder

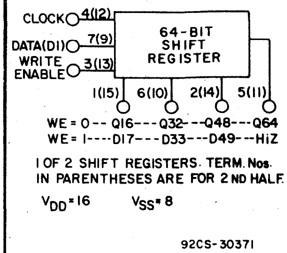
CD4514B (Page 310) Output "High" on Select

CD4515B (Page 310) Output "Low" on Select



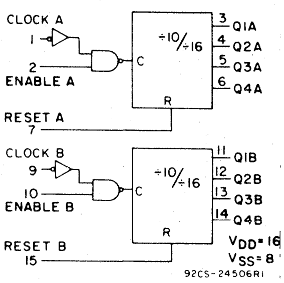
Binary Presettable Up/Down Counter

CD4516B (Page 297)



Dual 64-Bit Shift Register

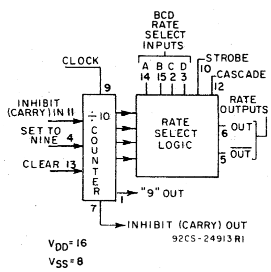
CD4517B (Page 314)



Dual Up Counter

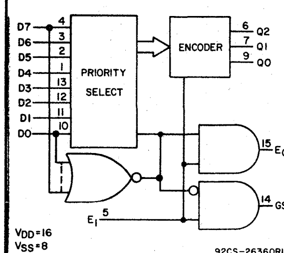
CD4518B (Page 319) BCD

CD4520B (Page 319) Binary



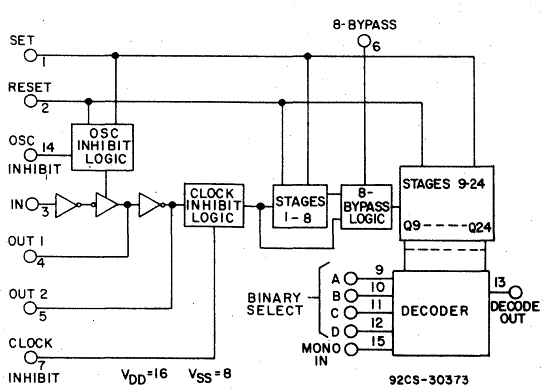
BCD Rate Multiplier

CD4527B (Page 324)



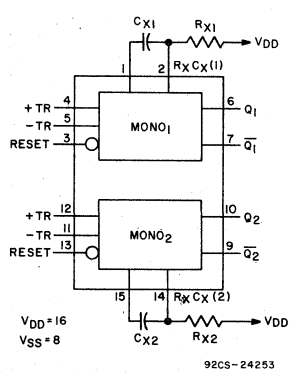
8-Bit Priority Encoder

CD4532B (Page 329)



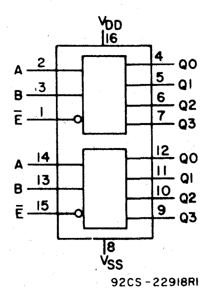
Programmable Timer

CD4536B (Page 333)



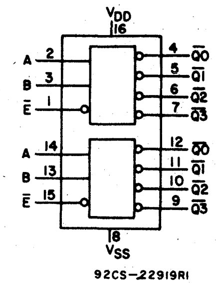
Dual Precision Monostable Multivibrator

CD4538B (Page 341)



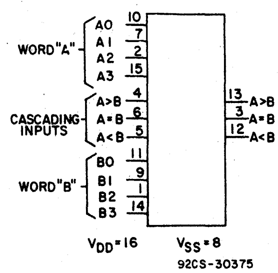
Dual Binary-to-1-of-4 Decoder/Demultiplexer Output "High" on Select

CD4555B (Page 344)



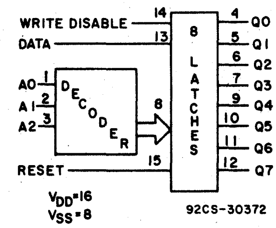
Dual Binary-to-1-of-4 Decoder/Demultiplexer Output "Low" on Select

CD4556B (Page 344)



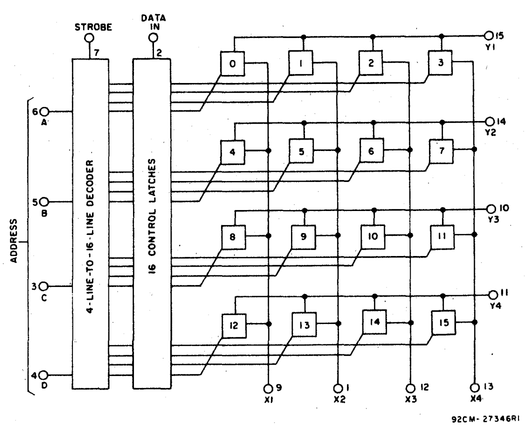
4-Bit Magnitude Comparator

CD4585B (Page 349)



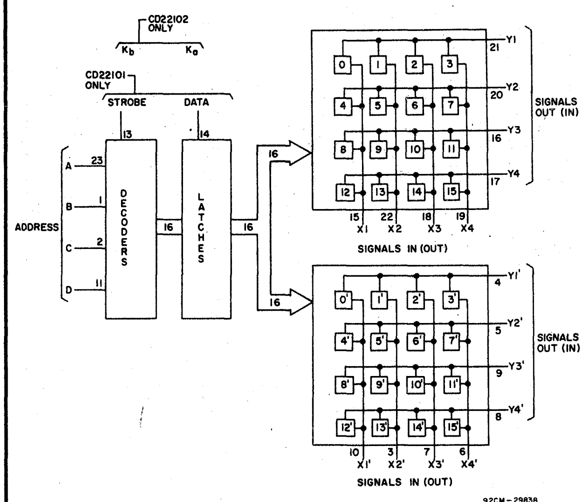
8-Bit Addressable Latch

CD4724B (Page 353)



4-by-4 Crosspoint Switch with Control Memory

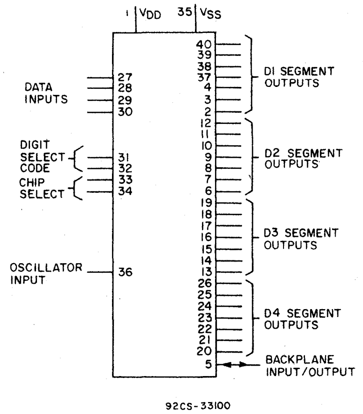
CD22100 (Page 584)



4-by-4-by-2 Crosspoint Switch with Control Memory

CD22101 (Page 589)
CD22102 (Page 589)

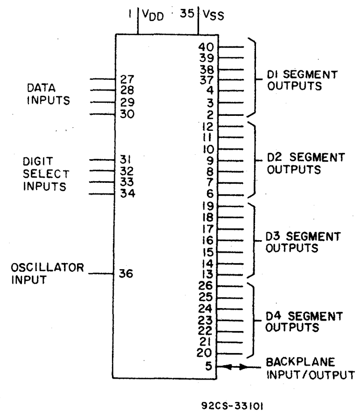
Functional Diagrams



4-Digit Decoder Driver

CD22104 (Page 593) Hexidecimal Display

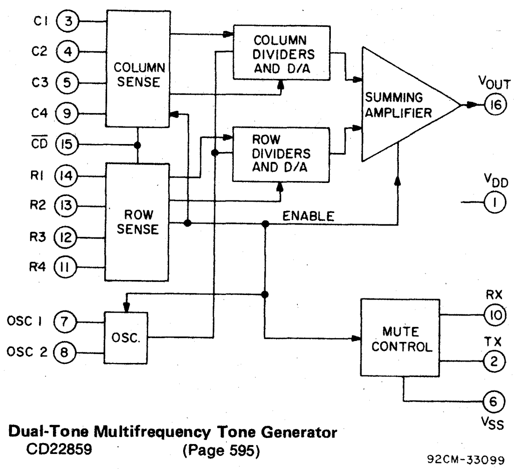
CD22104A (Page 593) Decimal Display



4-Digit Decoder Driver

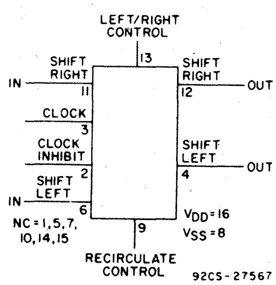
CD22105 (Page 594) Hexidecimal Display

CD22105A (Page 594) Decimal Display



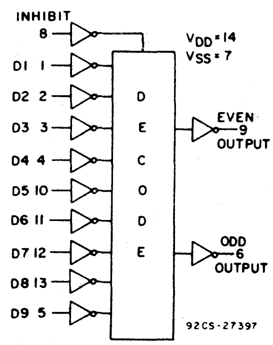
Dual-Tone Multifrequency Tone Generator

CD22859 (Page 595)



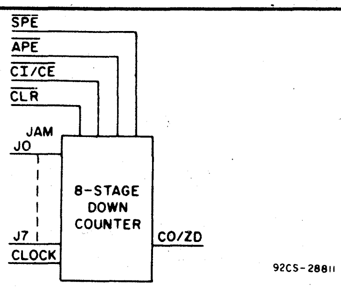
32-Stage Static Left/Right Shift Register

CD40100B (Page 357)



9-Bit Parity Generator/Checker

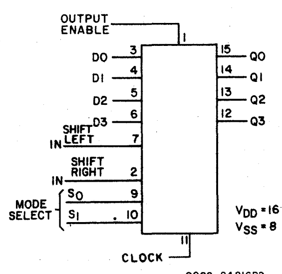
CD40101B (Page 362)



8-Stage Presettable Synchronous Down Counter

CD40102B (Page 365) 2-Decade BCD

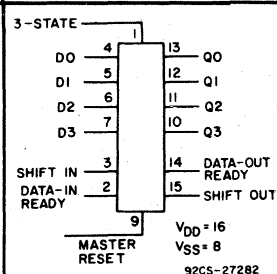
CD40103B (Page 365) 8-Bit Binary



4-Bit Universal Bidirectional Shift Register

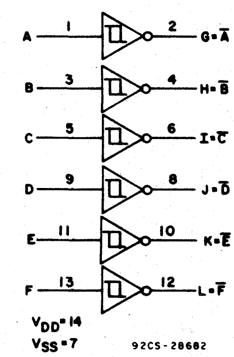
3-State Outputs

CD40104B (Page 372)



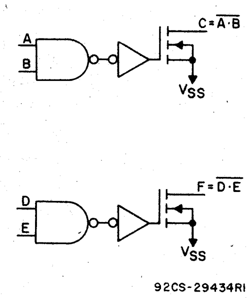
FIFO Register 4-Bits Wide by 16-Bits Long

CD40105B (Page 379)



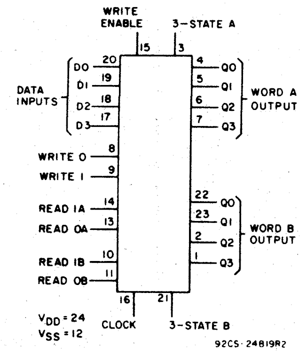
Hex Schmitt Trigger

CD40106B (Page 384)



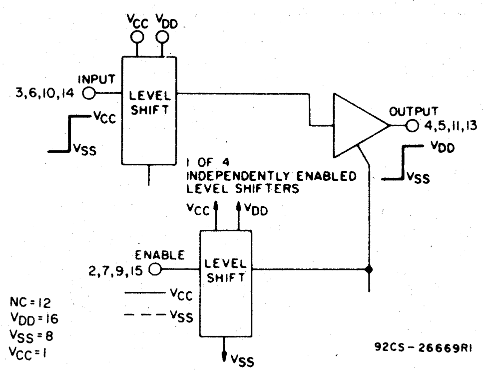
Dual 2-Input NAND Buffer/Driver

CD40107B (Page 388)



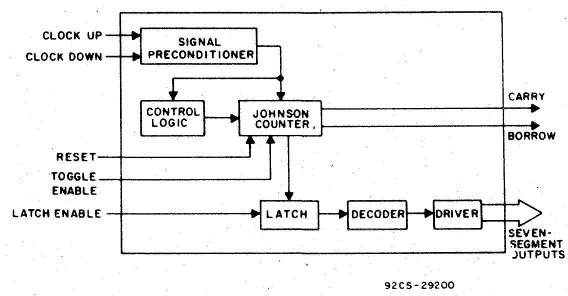
4-by-4 Multiport Register

CD40108B (Page 391)



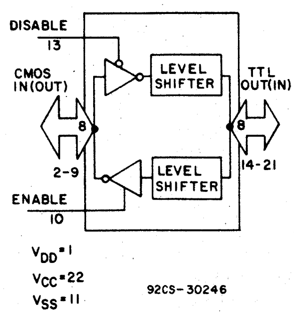
Quad Low-to-High Voltage Level Shifter

CD40109B (Page 396)



Decade Up-Down Counter/ Decoder/Latch/Driver

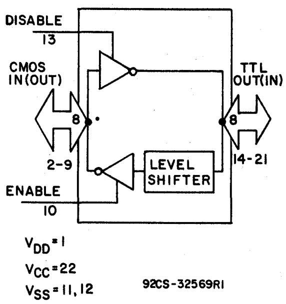
CD40110B (Page 400)



8-Bit Universal Bidirectional CMOS/TTL Level Converter

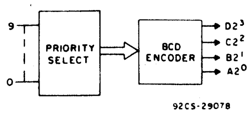
CD40115 (Page 599)

Functional Diagrams



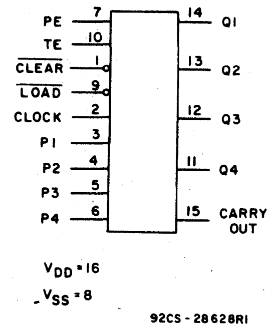
8-Bit Universal Bidirectional CMOS/TTL Level Converter

CD40116 (Page 601)



10-Line-to-4-Line BCD Priority Encoder

CD40147B (Page 405)



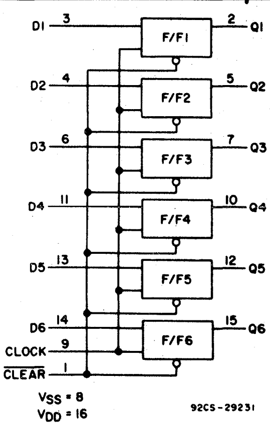
Synchronous 4-Bit Counter

CD40162B (Page 408)
Decade with Synchronous Clear

CD40163B (Page 408)
Binary with Synchronous Clear

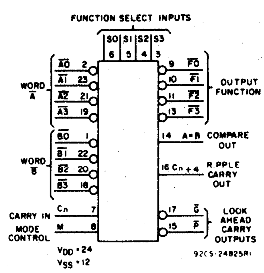
CD40160B (Page 408)
Decade with Asynchronous Clear

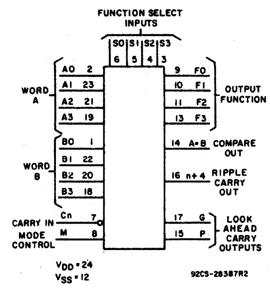
CD40161B (Page 408)
Binary with Asynchronous Clear



Hex "D" Type Flip-Flop

CD40174B (Page 415)

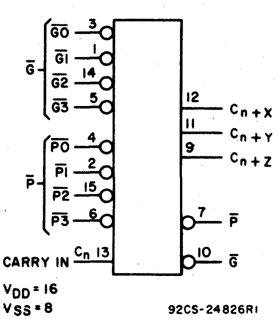




4-Bit Arithmetic Logic Unit

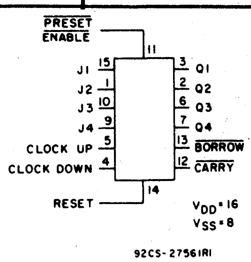
Active-Low Data **Active-High Data**

CD40181B (Page 419)



Look-Ahead Carry Generator

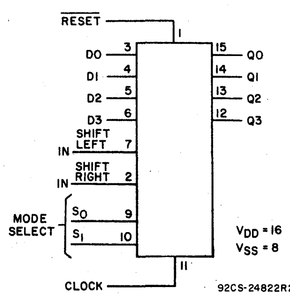
CD40182B (Page 424)



Presettable Up/Down Counter (Dual Clock with Reset)

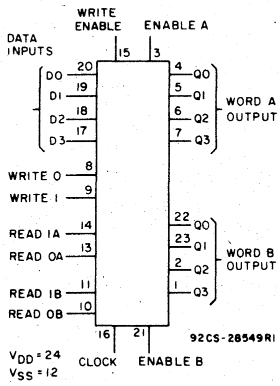
CD40192B (Page 428)
BCD

CD40193B (Page 428)
Binary



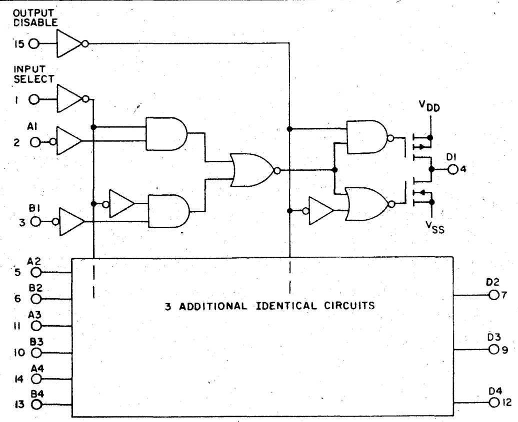
4-Bit Universal Bidirectional Shift Register with Asynchronous Master Reset

CD40194B (Page 372)



4-by-4 Multiport Register

CD40208B (Page 433)



Quad 2-Line-to-1-Line Data Selector/Multiplexer

92CM-28741R1

CD40257B (Page 438)

Cross-Reference Guide

This directory provides a quick reference to a wide variety of industry CMOS logic integrated circuits that can be replaced by RCA types.

The RCA types listed as replacements are electrically and mechanically equivalent to the corresponding industry types and can be used as direct replacements in most applications. The recommendations are based on the electrical and mechanical data published by various solid-state device manufacturers.

Before substituting any replacement type in a particular application, the user should review the operating conditions of the particular application with the specifications of the type he is planning to use as the substitute type.

Industry Type	RCA Replacement Type
CD4000CN	CD4000AE
CD4000MD	CD4000AD
CD4000MJ	CD4000AF
CD4001BCJ	CD4001BF
CD4001BCN	CD4001BE
CD4001BDM	CD4001BD
CD4001BMD	CD4001BD
CD4001BMJ	CD4001BF
CD4001BPC	CD4001BE
CD4002BDM	CD4002BD
CD4002BPC	CD4002BE
CD4002CN	CD4002AE
CD4002MD	CD4002AD
CD4002MJ	CD4002AF
CD4006BDM	CD4006BD
CD4006BPC	CD4006BE
CD4006CN	CD4006AE
CD4006MD	CD4006AD
CD4006MJ	CD4006AF
CD4007CN	CD4007AE
CD4007MD	CD4007AD
CD4007MJ	CD4007AF
CD4007UBDM	CD4007UBD
CD4007UBPC	CD4007UBE
CD4008BCJ	CD4008BF
CD4008BCN	CD4008BE
CD4008BDM	CD4008BD
CD4008BMD	CD4008BD
CD4008BMJ	CD4008BF
CD4008BPC	CD4008BE
CD4009CN	CD4009AE
CD4009MD	CD4009AD
CD4009MJ	CD4009AF
CD4010CN	CD4010AE
CD4010MD	CD4010AD
CD4010MJ	CD4010AF
CD4011BCJ	CD4011BF
CD4011BCN	CD4011BE
CD4011BDM	CD4011BD
CD4011BMD	CD4011BD

Industry Type	RCA Replacement Type
CD4011BMJ	CD4011BF
CD4011BPC	CD4011BE
CD4012BDM	CD4012BD
CD4012BPC	CD4012BE
CD4012CN	CD4012AE
CD4012MD	CD4012AD
CD4012MJ	CD4012AF
CD4013BCJ	CD4013BF
CD4013BCN	CD4013BE
CD4013BDM	CD4013BD
CD4013BMD	CD4013BD
CD4013BMJ	CD4013BF
CD4013BPC	CD4013BE
CD4014BDM	CD4014BD
CD4014BPC	CD4014BE
CD4014CN	CD4014AE
CD4014MD	CD4014AD
CD4014MJ	CD4014AF
CD4015BDM	CD4015BD
CD4015BPC	CD4015BE
C4015CN	CD4015AE
CD4015MD	CD4015AD
CD4015MJ	CD4015AF
CD4016BDM	CD4016BD
CD4016BPC	CD4016BE
CD4016CN	CD4016AE
CD4016MD	CD4016AD
CD4016MJ	CD4016AF
CD4017BCJ	CD4017BF
CD4017BCN	CD4017BE
CD4017BDM	CD4017BD
CD4017BMD	CD4017BD
CD4017BMJ	CD4017BF
CD4017BPC	CD4017BE
CD4018BCJ	CD4018BF
CD4018BCN	CD4018BE
CD4018BDM	CD4018BD
CD4018BMD	CD4018BD
CD4018BMJ	CD4018BF
CD4018BPC	CD4018BE

Industry Type	RCA Replacement Type
CD4019BCJ	CD4019BF
CD4019BCN	CD4019BE
CD4019BDM	CD4019BD
CD4019BMD	CD4019BD
CD4019BMJ	CD4019BF
CD4019BPC	CD4019BE
CD4020BCJ	CD4020BF
CD4020BCN	CD4020BE
CD4020BDM	CD4020BD
CD4020BMD	CD4020BD
CD4020BMJ	CD4020BF
CD4020BPC	CD4020BE
CD4021BDM	CD4021BD
CD4021BPC	CD4021BE
CD4021CN	CD4021AE
CD4021MD	CD4021AD
CD4021MJ	CD4021AF
CD4022BCJ	CD4022BF
CD4022BCN	CD4022BE
CD4022BDM	CD4022BD
CD4022BMD	CD4022BD
CD4022BMJ	CD4022BF
CD4022BPC	CD4022BE
CD4023BCJ	CD4023BF
CD4023BCN	CD4022BE
CD4023BDM	CD4023BD
CD4023BMD	CD4023BD
CD4023BMJ	CD4023BF
CD4023BPC	CD4023BE
CD4023CN	CD4023AE
CD4023MD	CD4023AD
CD4023MJ	CD4023AF
CD4024BCJ	CD4024BF
CD4024BCN	CD4024BE
CD4024BDM	CD4024BD
CD4024BMD	CD4024BD
CD4024BMJ	CD4024BF
CD4024BPC	CD4024BE
CD4025BCJ	CD4025BF
CD4025BCN	CD4025BE

Industry Type	RCA Replacement Type
CD4025BDM	CD4025BD
CD4025BMD	CD4025BD
CD4025BMJ	CD4025BF
CD4025BPC	CD4025BE
CD4025CN	CD4025AE
CD4025MD	CD4025AD
CD4025MJ	CD4025AF
CD4027BCJ	CD4027BF
CD4027BCN	CD4027BE
CD4027BDM	CD4027BD
CD4027BMD	CD4027BD
CD4027BMJ	CD4027BF
CD4027BPC	CD4027BE
CD4028BCJ	CD4028BF
CD4028BCN	CD4028BE
CD4028BDM	CD4028BD
CD4028BMD	CD4028BD
CD4028BMJ	CD4028BF
CD4028BPC	CD4028BE
CD4029BCJ	CD4029BF
CD4029BCN	CD4029BE
CD4029BDM	CD4029BD
CD4029BMD	CD4029BD
CD4029BMJ	CD4029BF
CD4029BPC	CD4029BE
CD4030BDM	CD4030BD
CD4030BPC	CD4030BE
CD4030CN	CD4030AE
CD4030MD	CD4030AD
CD4030MJ	CD4030AF
CD4031BCN	CD4031BE
CD4031BDM	CD4031BD
CD4031BMD	CD4031BD
CD4031BMJ	CD4031BF
CD4034BCN	CD4034BE
CD4034BDM	CD4034BD
CD4034BMD	CD4034BD
CD4034BMJ	CD4034BF
CD4034BPC	CD4034BE
CD4035BCN	CD4035BE
CD4035BDM	CD4035BD
CD4035BMD	CD4035BD
CD4035BMJ	CD4035BF
CD4035BPC	CD4035BE
CD4040BCJ	CD4040BF
CD4040BCN	CD4040BE
CD4040BDM	CD4040BD
CD4040BMD	CD4040BD
CD4040BMJ	CD4040BF
CD4040BPC	CD4040BE
CD4041BDM	CD4041BD
CD4041BPC	CD4041BE
CD4041CN	CD4041AE
CD4041MD	CD4041AD
CD4041MJ	CD4041AF
CD4042BCJ	CD4042BF
CD4042BCN	CD4042BE
CD4042BDM	CD4042BD
CD4042BMD	CD4042BD
CD4042BMJ	CD4042BF
CD4042BPC	CD4042BE
CD4043BDM	CD4043BD
CD4043BPC	CD4043BE
CD4043CN	CD4043AE
CD4043MD	CD4043AD

Industry Type	RCA Replacement Type
CD4043MJ	CD4043AF
CD4044BDM	CD4044BD
CD4044BPC	CD4044BE
CD4044CN	CD4044AE
CD4044MD	CD4044AD
CD4044MJ	CD4044AF
CD4045BDM	CD4045BD
CD4045BPC	CD4045BE
CD4046BCN	CD4046BE
CD4046BDM	CD4046BD
CD4046BMD	CD4046BD
CD4046BMJ	CD4046BF
CD4046BPC	CD4046BE
CD4047BCN	CD4047BE
CD4047BDM	CD4047BD
CD4047BMD	CD4047BD
CD4047BMJ	CD4047BF
CD4047BPC	CD4047BE
CD4048BCJ	CD4048BF
CD4048BCN	CD4048BE
CD4048BMD	CD4048BD
CD4048BMJ	CD4048BF
CD4049BDM	CD4049BD
CD4049BPC	CD4049BE
CD4049CN	CD4049AE
CD4049MD	CD4049AD
CD4049MJ	CD4049AF
CD4050BCJ	CD4050BF
CD4050BCN	CD4050BE
CD4050BDM	CD4050BD
CD4050BMD	CD4050BD
CD4050BMJ	CD4050BF
CD4050BPC	CD4050BE
CD4051BCJ	CD4051BF
CD4051BCN	CD4051BE
CD4051BDM	CD4051BD
CD4051BMD	CD4051BD
CD4051BMJ	CD4051BF
CD4051BPC	CD4051BE
CD4052BCJ	CD4052BF
CD4052BCN	CD4052BE
CD4052BDM	CD4052BD
CD4052BMD	CD4052BD
CD4052BMJ	CD4052BF
CD4052BPC	CD4052BE
CD4053BCJ	CD4053BF
CD4053BCN	CD4053BE
CD4053BDM	CD4053BD
CD4053BMD	CD4053BD
CD4053BMJ	CD4053BF
CD4053BPC	CD4053BE
CD4060BCJ	CD4060BF
CD4060BCN	CD4060BE
CD4060BMD	CD4060BD
CD4060BMJ	CD4060BF
CD4066BCJ	CD4066BF
CD4066BCN	CD4066BE
CD4066BDM	CD4066BD
CD4066BMD	CD4066BD
CD4066BMJ	CD4066BF
CD4066BPC	CD4066BE
CD4067BDM	CD4067BD
CD4067BPC	CD4067BE
CD4068BDM	CD4068BD
CD4068BPC	CD4068BE

Industry Type	RCA Replacement Type
CD4069CN	CD4069AE
CD4069MD	CD4069AD
CD4069MJ	CD4069AF
CD4069UBDM	CD4069UBD
CD4069UBPC	CD4069UBE
CD4070BCJ	CD4070BF
CD4070BCN	CD4070BE
CD4070BDM	CD4070BD
CD4070BMJ	CD4070BF
CD4070BPC	CD4070BE
CD4070CN	CD4070AE
CD4070MD	CD4070AD
CD4070MJ	CD4070AF
CD4071BCJ	CD4071BF
CD4071BCN	CD4071BE
CD4071BDM	CD4071BD
CD4071BMD	CD4071BD
CD4071BMJ	CD4071BD
CD4071BPC	CD4071BE
CD4072BDM	CD4072BD
CD4072BPC	CD4072BE
CD4073BCJ	CD4073BF
CD4073BCN	CD4073BE
CD4073BDM	CD4073BD
CD4073BMD	CD4073BD
CD4073BMJ	CD4073BF
CD4073BPC	CD4073BE
CD4075BCJ	CD4075BF
CD4075BCN	CD4075BE
CD4075BDM	CD4075BD
CD4075BMD	CD4075BD
CD4075BMJ	CD4075BF
CD4075BPC	CD4075BE
CD4076BCN	CD4076BE
CD4076BDM	CD4076BD
CD4076BMD	CD4076BD
CD4076BMJ	CD4076BF
CD4076BPC	CD4076BE
CD4077BDM	CD4077BD
CD4077BPC	CD4077BE
CD4078BMD	CD4078BD
CD4078BPC	CD4078BE
CD4081BCJ	CD4081BF
CD4081BCN	CD4081BE
CD4081BDM	CD4081BD
CD4081BMD	CD4081BD
CD4081BMJ	CD4081BF
CD4082BDM	CD4082BD
CD4082BPC	CD4082BE
CD4085BDM	CD4085BD
CD4085BPC	CD4085BE
CD4086BDM	CD4086BD
CD4086BPC	CD4086BE
CD4089BCJ	CD4089BF
CD4089BCN	CD4089BE
CD4089BMD	CD4089BD
CD4089BMJ	CD4089BF
CD4093BCJ	CD4093BF
CD4093BCN	CD4093BE
CD4093BDM	CD4093BD
CD4093BMD	CD4093BD
CD4093BMJ	CD4093BF
CD4093BPC	CD4093BE
CD4099BCJ	CD4099BF
CD4099BCN	CD4099BE

Cross-Reference Guide

Industry Type	RCA Replacement Type
CD4099BMD	CD4099BD
CD4099BMJ	CD4099BF
CD4510BCJ	CD4510BF
CD4510BCN	CD4510BE
CD4510BDM	CD4510BD
CD4510BMD	CD4510BD
CD4510BMJ	CD4510BF
CD4510BPC	CD4510BE
CD4511BCJ	CD4511BF
CD4511BCN	CD4511BE
CD4511BDM	CD4511BD
CD4511BMD	CD4511BD
CD4511BMJ	CD4511BF
CD4511BPC	CD4511BE
CD4512BDM	CD4512BD
CD4512BPC	CD4512BE
CD4514BDM	CD4514BD
CD4514BPC	CD4514BE
CD4515BDM	CD4515BD
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CD4516BMJ	CD4516BF
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CD4518BCJ	CD4518BF
CD4518BCN	CD4518BE
CD4518BDM	CD4518BD
CD4518BMD	CD4518BD
CD4518BMJ	CD4518BF
CD4518BPC	CD4518BE
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CD4527BMJ	CD4527BF
CD4527BPC	CD4527BE
CD4532BDM	CD4532BD
CD4532BPC	CD4532BE
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CD4555BPC	CD4555BE
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CD4724BMJ	CD4724BF
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CD40106BCN	CD40106BE
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CD40106BMJ	CD40106BF
CD40160BCJ	CD40160BF
CD40160BCN	CD40106BE
CD40160BDM	CD40160BD
CD40160BMD	CD40160BD
CD40160BMJ	CD40160BF
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CD40161BMJ	CD40161BF
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CD40162BCN	CD40162BE
CD40162BDM	CD40162BD
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CD40162BMJ	CD40162BF
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CD40163BMD	CD40163BD
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CD40193BCJ	CD40193BF
CD40193BCN	CD40193BE
CD40193BMD	CD40193BD
CD40193BMJ	CD40193BF
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F4001PC	CD4001BE
F4002DC	CD4002BF
F4002PC	CD4002BE
F4006DC	CD4006BF
F4006PC	CD4006BE
F4007DC	CD4007BF
F4007PC	CD4007BE
F4008DC	CD4008BF
F4008PC	CD4008BE
F4011DC	CD4011BF
F4011PC	CD4011BE
F4012DC	CD4012BF
F4012PC	CD4012BE
F4013DC	CD4013BF
F4013PC	CD4013BE
F4014DC	CD4014BF
F4014PC	CD4014BE
F4015DC	CD4015BF
F4015PC	CD4015BE
F4016DC	CD4016BF
F4016PC	CD4016BE
F4017DC	CD4017BF
F4017PC	CD4017BE
F4018DC	CD4018BF
F4018PC	CD4018BE
F4019DC	CD4019BF
F4019PC	CD4019BE
F4020DC	CD4020BF
F4020PC	CD4020BE
F4022DC	CD4022BF
F4022PC	CD4022BE
F4023DC	CD4023BF
F4023PC	CD4023BE
F4024DC	CD4024BF
F4024PC	CD4024BE
F4025DC	CD4025BF
F4025PC	CD4025BE
F4027DC	CD4027BF
F4027PC	CD4027BE
F4028DC	CD4028BF
F4028PC	CD4028BE
F4029DC	CD4029BF
F4029PC	CD4029BE
F4030DC	CD4030BF
F4030PC	CD4030BE
F4035DC	CD4035BF
F4035PC	CD4035BE
F4040DC	CD4040BF
F4040PC	CD4040BE
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F4041PC	CD4041BE
F4042DC	CD4042BF
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F4043DC	CD4043BF
F4043PC	CD4043BE
F4044DC	CD4044BF
F4044PC	CD4044BE
F4046DC	CD4046BF
F4046PC	CD4046BE
F4047DC	CD4047BF
F4047PC	CD4047BE
F4049DC	CD4049BF
F4049PC	CD4049BE
F4050DC	CD4050BF
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F4053PC	CD4053BE
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F4066PC	CD4066BE
F4067DC	CD4067BF
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F4068DC	CD4068BF
F4068PC	CD4068BE
F4069DC	CD4069UBF
F4069PC	CD4069UBE
F4070DC	CD4070BF
F4070PC	CD4070BE
F4071DC	CD4071BF
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F4072DC	CD4072BF
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F4075DC	CD4075BF
F4075PC	CD4075BE
F4076DC	CD4076BF
F4076PC	CD4076BE
F4077DC	CD4077BF
F4077PC	CD4077BE
F4078DC	CD4078BF
F4078PC	CD4078BE
F4081DC	CD4081BF
F4081PC	CD4081BE
F4082DC	CD4082BF
F4082PC	CD4082BE
F4085DC	CD4085BF

Industry Type	RCA Replacement Type
F4085PC	CD4085BE
F4086DC	CD4086BF
F4086PC	CD4086BE
F4510DC	CD4510BF
F4510PC	CD4510BE
F4511DC	CD4511BF
F4511PC	CD4511BE
F4512DC	CD4512BF
F4512PC	CD4512BE
F4514DC	CD4514BF
F4514PC	CD4514BE
F4515DC	CD4515BF
F4515PC	CD4515BE
F4516DC	CD4516BF
F4516PC	CD4516BE
F4518DC	CD4518BF
F4518PC	CD4518BE
F4520DC	CD4520BF
F4520PC	CD4520BE
F4527DC	CD4527BF
F4527PC	CD4527BE
F4532DC	CD4532BF
F4532PC	CD4532BE
F4555DC	CD4555BF
F4555PC	CD4555BE
F4556DC	CD4556BF
F4556PC	CD4556BE
F4581PC	CD40181BF
F4581DC	CD40181BE
F4582DC	CD40182BF
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F4724DC	CD4724BF
F4724PC	CD4724BE
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F40085PC	CD4585BE
F40160DC	CD40160BF
F40160PC	CD40160BE
F40161DC	CD40161BF
F40161PC	CD40161BE
F40162DC	CD40162BF
F40162PC	CD40162BE
F40163DC	CD40163BF
F40163PC	CD40163BE
F40174DC	CD40174BF
F40174PC	CD40174BE
F40192DC	CD40192BF
F40192PC	CD40192BE
F40193DC	CD40193BF
F40193PC	CD40193BE
F40194DC	CD40194BF
F40194PC	CD40194BE
HD174C04	CD4096BD
HD174C14	CD40106BD
HD174C86	CD4030BD
HD174C86	CD4070BD
HD174C160	CD40160BD
HD174C161	CD40161BD
HD174C162	CD40162BD
HD174C163	CD40163BD
HD174C164	CD4015BD
HD174C165	CD4021BD
HD174C173	CD4076BD
HD174C174	CD40174BD
HD174C192	CD40192BD
HD174C193	CD40193BD

Industry Type	RCA Replacement Type
HD374C04	CD4069BE
HD374C14	CD40106BE
HD374C86	CD4030BE
HD374C86	CD4070BE
HD374C160	CD40160BE
HD374C161	CD40161BE
HD374C162	CD40162BE
HD374C163	CD40163BE
HD374C164	CD4015BE
HD374C165	CD4021BE
HD374C173	CD4076BE
HD374C174	CD40174BE
HD374C173	CD4076BE
HD374C192	CD40192BE
HD374C193	CD40193BE
MC14000UBAL	CD4000UBD
MC14000UBCP	CD4000UBE
MC14001BAL	CD4001BD
MC14001BCP	CD4001BE
MC14001UBAL	CD4001UBD
MC14001UBCP	CD4001UBE
MC14002BAL	CD4002BD
MC14002BCP	CD4002BE
MC14002UBAL	CD4002UBD
MC14002UBCP	CD4002UBE
MC14006BAL	CD4006BD
MC14006BCP	CD4006BE
MC14007UBAL	CD4007UBD
MC14007UBCP	CD4007UBE
MC14008BAL	CD4008BD
MC14008BCP	CD4008BE
MC14011BAL	CD4011BD
MC14011BCP	CD4011BE
MC14011UBAL	CD4011UBD
MC14011UBCP	CD4011UBE
MC14012BAL	CD4012BD
MC14012BCP	CD4012BE
MC14012UBAL	CD4012UBD
MC14012UBCP	CD4012UBE
MC14013BAL	CD4013BD
MC14013BCP	CD4013BE
MC14014BAL	CD4014BD
MC14014BCP	CD4014BE
MC14015BAL	CD4015BD
MC14015BCP	CD4015BE
MC14016BAL	CD4016BD
MC14016BCP	CD4016BE
MC14017BAL	CD4017BD
MC14017BCP	CD4017BE
MC14018BAL	CD4018BD
MC14018BCP	CD4018BE
MC14020BAL	CD4020BD
MC14020BCP	CD4020BE
MC14021BAL	CD4021BD
MC14021BCP	CD4021BE
MC14022BAL	CD4022BD
MC14022BCP	CD4022BE
MC14023BAL	CD4023BD
MC14023BCP	CD4023BE
MC14023UBAL	CD4023UBD
MC14023UBCP	CD4023UBE
MC14024BAL	CD4024BD
MC14024BCP	CD4024BE
MC14025BAL	CD4025BD
MC14025BCP	CD4025BE

Industry Type	RCA Replacement Type
MC14025UBAL	CD4025UBD
MC14025UBCP	CD4025UBE
MC14027BAL	CD4027BD
MC14027BCP	CD4027BE
MC14028BAL	CD4028BD
MC14028BCP	CD4028BE
MC14029BAL	CD4029BD
MC14029BCP	CD4029BE
MC14032BAL	CD4032BD
MC14032BCP	CD4032BE
MC14034BAL	CD4034BD
MC14034BCP	CD4034BE
MC14035BAL	CD4035BD
MC14035BCP	CD4035BE
MC14038BAL	CD4038BD
MC14038BCP	CD4038BE
MC14040BAL	CD4040BD
MC14040BCP	CD4040BE
MC14042BAL	CD4042BD
MC14042BCP	CD4042BE
MC14043BAL	CD4043BD
MC14043BCP	CD4043BE
MC14044BAL	CD4044BD
MC14044BCP	CD4044BE
MC14046BAL	CD4046BD
MC14046BCP	CD4046BE
MC14049UBAL	CD4049UBD
MC14049UBCP	CD4049UBE
MC14050BAL	CD4050BD
MC14050BCP	CD4050BE
MC14051BAL	CD4051BD
MC14051BCP	CD4051BE
MC14052BAL	CD4052BD
MC14052BCP	CD4052BE
MC14053BAL	CD4053BD
MC14053BCP	CD4053BE
MC14066BAL	CD4066BD
MC14066BCP	CD4066BE
MC14068BAL	CD4068BD
MC14068BCP	CD4068BE
MC14069UBAL	CD4069UBD
MC14069UBCP	CD4069UBE
MC14070BAL	CD4070BD
MC14070BCP	CD4070BE
MC14071BAL	CD4071BD
MC14071BCP	CD4071BE
MC14072BAL	CD4072BD
MC14072BCP	CD4072BE
MC14073BAL	CD4073BD
MC14073BCP	CD4073BE
MC14075BAL	CD4075BD
MC14075BCP	CD4075BE
MC14076BAL	CD4076BD
MC14076BCP	CD4076BE
MC14077BAL	CD4077BD
MC14077BCP	CD4077BE
MC14078BAL	CD4078BD
MC14078BCP	CD4078BE
MC14081BAL	CD4081BD
MC14081BCP	CD4081BE
MC14082BAL	CD4082BD
MC14082BCP	CD4082BE
MC14093BAL	CD4093BD
MC14093BCP	CD4093BE
MC14094BAL	CD4094BD

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Industry Type	RCA Replacement Type
MC14094BCP	CD4094BE
MC14099BAL	CD4099BD
MC14099BCP	CD4099BE
MC14160BAL	CD40160BD
MC14160BCP	CD40160BE
MC14161BAL	CD40161BD
MC14161BCP	CD40161BE
MC14162BAL	CD40162BD
MC14162BCP	CD40162BE
MC14163BAL	CD40163BD
MC14163BCP	CD40163BE
MC14174BAL	CD40174BD
MC14174BCP	CD40174BE
MC14194BAL	CD40194BD
MC14194BCP	CD40194BE
MC14502BAL	CD4502BD
MC14502BCP	CD4502BE
MC14504BAL	CD40109BD
MC14504BCP	CD40109BE
MC14508BAL	CD4508BD
MC14508BCP	CD4508BE
MC14510BAL	CD4510BD
CD14510BCP	CD4510BE
MC14511BAL	CD4511BD
MC14511BCP	CD4511BE
MC14512BAL	CD4512BD
MC14512BCP	CD4512BE
MC14514BAL	CD4514BD
MC14514BCP	CD4514BE
MC14515BAL	CD4515BD
MC14515BCP	CD4515BE
MC14516BAL	CD4516BD
MC14516BCP	CD4516BE
MC14517BAL	CD4517BD
MC14517BCP	CD4517BE
MC14518BAL	CD4518BD
MC14518BCP	CD4518BE
MC14520BAL	CD4520BD
MC14520BCP	CD4520BE
MC14527BAL	CD4527BD
MC14527 BCP	CD4527BE
MC14532BAL	CD4532BD
MC14532BCP	CD4532BE
MC14536BAL	CD4536BD
MC14536BCP	CD4536BE
MC14555BAL	CD4555BD
MC14555BCP	CD4555BE
MC14556BAL	CD4556BD
MC14556BCP	CD4556BE
MC14581BAL	CD40181BD
MC14581BCP	CD40181BE
MC14582BAL	CD40182BD
MC14582BCP	CD40182BE
MC14584BAL	CD40106BD
MC14584BCP	CD40106BE
MC14585BAL	CD4585BD
MC14585BCP	CD4585BE
MM54C04D	CD4069UBD
MM54C160D	CD40160BD
MM54C161D	CD40161BD
MM54C162D	CD40162BD
MM54C163D	CD40163BD
MM54C173D	CD4076BD
MM54C174D	CD40174BD
MM74C04N	CD4069UBE

Industry Type	RCA Replacement Type
MM74C160N	CD40160BE
MM74C16IN	CD40161BE
MM74C162N	CD40162BE
MM74C163N	CD40163BE
MM74C164N	CD4015BE
MM74C165N	CD4021BE
MM74C173N	CD4076BE
MM74C174N	CD40174BE
SCL4000BC	CD4000BF
SCL4000BD	CD4000BD
SCL4000BE	CD4000BE
SCL4001BC	CD4001BF
SCL4001BD	CD4001BD
SCL4001BE	CD4001BE
SCL4001UBC	CD4001UBF
SCL4001UBD	CD4001UBD
SCL4001UBE	CD4001UBE
SCL4002BC	CD4002BF
SCL4002BD	CD4002BD
SCL4002BE	CD4002BE
SCL4006ABC	CD4006BF
SCL4006ABD	CD4006BD
SCL4006ABE	CD4006BE
SCL4007UBC	CD4007UBF
SCL4007UBD	CD4007UBD
SCL4007UBE	CD4007UBE
SCL4008BC	CD4008BF
SCL4008BD	CD4008BD
SCL4008BE	CD4008BE
SCL4009UBC	CD4009UBF
SCL4009UBD	CD4009UBD
SCL4009UBE	CD4009UBE
SCL4010BC	CD4010BF
SCL4010BD	CD4010BD
SCL4010BE	CD4010BE
SCL4011BC	CD4011BF
SCL4011BD	CD4011BD
SCL4011BE	CD4011BE
SCL4011UBC	CD4011UBF
SCL4011UBD	CD4011UBD
SCL4011UBE	CD4011UBE
SCL4012BC	CD4012BF
SCL4012BD	CD4012BD
SCL4012BE	CD4012BE
SCL4013BC	CD4013BF
SCL4013BD	CD4013BD
SCL4013BE	CD4013BE
SCL4014BC	CD4014BF
SCL4014BD	CD4014BD
SCL4014BE	CD4014BE
SCL4015BC	CD4015BF
SCL4015BD	CD4015BD
SCL4015BE	CD4015BE
SCL4016BC	CD4016BF
SCL4016BD	CD4016BD
SCL4016BE	CD4016BE
SCL4017BC	CD4017BF
SCL4017BD	CD4017BD
SCL4017BE	CD4017BE
SCL4018BC	CD4018BF
SCL4018BD	CD4018BD
SCL4018BE	CD4018BE
SCL4019BC	CD4019BF
SCL4019BD	CD4019BD
SCL4019BE	CD4019BE

Industry Type	RCA Replacement Type
SCL4020ABC	CD4020BF
SCL4020ABD	CD4020BD
SCL4020ABE	CD4020BE
SCL4021BC	CD4021BF
SCL4021BD	CD4021BD
SCL4021BE	CD4021BE
SCL4022ABC	CD4022BF
SCL4022ABD	CD4022BD
SCL4022ABE	CD4022BE
SCL4023BC	CD4023BF
SCL4023BD	CD4023BD
SCL4023BE	CD4023BE
SCL4024BC	CD4024BF
SCL4024BD	CD4024BD
SCL4024BE	CE4024BE
SCL4025BC	CD4025BF
SCL4025BD	CD4025BD
SCL4025BE	CD4025BE
SCL4026ABC	CD4026BF
SCL4026ABD	CD4026BD
SCL4026ABE	CD4026BE
SCL4027BC	CD4027BF
SCL4027BD	CD4027BD
SCL4027BE	CD4027BE
SCL4028BC	CD4028BF
SCL4028BD	CD4028BD
SCL4028BE	CD4028BE
SCL4029BC	CD4029BF
SCL4029BD	CD4029BD
SCL4029BE	CD4029BE
SCL4030BC	CD4030BF
SCL4030BD	CD4030BD
SCL4030BE	CD4030BE
SCL4033ABC	CD4033BF
SCL4033ABD	CD4033BD
SCL4033ABE	CD4033BE
SCL4034ABC	CD4034BF
SCL4034ABD	CD4034BD
SCL4034ABE	CD4034BE
SCL4035BC	CD4035BF
SCL4035BD	CD4035BD
SCL4035BE	CD4035BE
SCL4040ABC	CD4040BF
SCL4040ABD	CD4040BD
SCL4040ABE	CD4040BE
SCL4041UBC	CD4041UBE
SCL4041UBD	CD4041UBD
SCL4041UBE	CD4041UBE
SCL4042BC	CD4042BE
SCL4042BD	CD4042BD
SCL4042BE	CD4042BE
SCL4043ABC	CD4043BF
SCL4043ABD	CD4043BD
SCL4043ABE	CD4043BE
SCL4044ABC	CD4044BF
SCL4044ABD	CD4044BD
SCL4044ABE	CD4044BE
SCL4046BC	CD4046BF
SCL4046BD	CD4046BD
SCL4046BE	CD4046BE
SCL4049UBC	CD4049BF
SCL4049UBD	CD4049BD
SCL4049UBE	CD4049BE
SCL4050BC	CD4050BF
SCL4050BD	CD4050BD

Industry Type	RCA Replacement Type
SCL4050BE	CD4050BE
SCL4051BC	CD4051BF
SCL4051BD	CD4051BD
SCL4051BE	CD4051BE
SCL4052BC	CD4052BF
SCL4052BD	CD4052BD
SCL4052BE	CD4052BE
SCL4053BC	CD4053BF
SCL4053BD	CD4053BD
SCL4053BE	CD4053BE
SCL4060ABC	CD4060BF
SCL4060ABD	CD4060BD
SCL4060ABE	CD4060BE
SCL4066BC	CD4066BF
SCL4066BD	CD4066BD
SCL4066BE	CD4066BE
SCL4068BC	CD4068BF
SCL4068BD	CD4068BD
SCL4068BE	CD4068BE
SCL4069UBC	CD4069UBF
SCL4069UBD	CD4069UBD
SCL4069UBE	CD4069UBE
SCL4070BC	CD4070BF
SCL4070BD	CD4070BD
SCL4070BE	CD4070BE
SCL4071BC	CD4071BF
SCL4071BD	CD4071BD
SCL4071BE	CD4071BE
SCL4072BC	CD4072BF
SCL4072BD	CD4072BD
SCL4072BE	CD4072BE
SCL4073BC	CD4073BF
SCL4073BD	CD4073BD
SCL4073BE	CD4073BE
SCL4075BC	CD4075BF
SCL4075BD	CD4075BD
SCL4075BE	CD4075BE
SCL4076BC	CD4076BF
SCL4076BD	CD4076BD
SCL4076BE	CD4076BE
SCL4077BC	CD4077BF
SCL4077BD	CD4077BD
SCL4077BE	CD4077BE
SCL4078BC	CD4078BF
SCL4078BD	CD4078BD
SCL4078BE	CD4078BE
SCL4081BC	CD4081BF
SCL4081BD	CD4081BD
SCL4081BE	CD4081BE
SCL4082BC	CD4082BF
SCL4082BD	CD4082BD
SCL4082BE	CD4082BE
SCL4093BC	CD4093BF
SCL4093BD	CD4093BD
SCL4093BE	CD4093BE
SCL4160BC	CD40160BF
SCL4160BD	CD40160BD
SCL4160BE	CD40160BE
SCL4161BC	CD40161BF
SCL4161BD	CD40161BD
SCL4161BE	CD40161BE
SCL4162BC	CD40162BF
SCL4162BD	CD40162BD
SCL4162BE	CD40162BE
SCL4163BC	CD40163BF

Industry Type	RCA Replacement Type
SCL4163BD	CD40163BD
SCL4163BE	CD40163BE
SCL4502BC	CD4502BF
SCL4502BD	CD4502BD
SCL4502BE	CD4502BE
SCL4508BC	CD4508BF
SCL4508BD	CD4508BD
SCL4508BE	CD4508BE
SCL4510BC	CD4510BF
SCL4510BD	CD4510BD
SCL4510BE	CD4510BE
SCL4511BC	CD4511BF
SCL4511BD	CD4511BD
SCL4511BE	CD4511BE
SCL4512BC	CD4512BF
SCL4512BD	CD4512BD
SCL4512BE	CD4512BE
SCL4514BC	CD4514BF
SCL4514BD	CD4514BD
SCL4514BE	CD4514BE
SCL4515BC	CD4515BF
SCL4515BD	CD4515BD
SCL4515BE	CD4515BE
SCL4516BC	CD4516BF
SCL4516BD	CD4516BD
SCL4516BE	CD4516BE
SCL4517BC	CD4517BF
SCL4517BD	CD4517BD
SCL4517BE	CD4517BE
SCL4518BC	CD4518BF
SCL4518BD	CD4518BD
SCL4518BE	CD4518BE
SCL4520BC	CD4520BF
SCL4520BD	CD4520BD
SCL4520BE	CD4520BE
SCL4527BC	CD4527BF
SCL4527BD	CD4527BD
SCL4527BE	CD4527BE
SCL4555BC	CD4555BF
SCL4555BD	CD4555BD
SCL4555BE	CD4555BE
SCL4556BC	CD4556BF
SCL4556BD	CD4556BD
SCL4556BE	CD4556BE
SCL4581BC	CD4581BF
SCL4581BD	CD4581BD
SCL4581BE	CD4581BE
SCL4582BC	CD4582BF
SCL4582BD	CD4582BD
SCL4582BE	CD4582BE
SCL4585BC	CD4585BF
SCL4585BD	CD4585BD
SCL4585BE	CD4585BE
TP4000AN	CD4000AE
TP4001AN	CD4001AE
TP4001BN	CD4001BE
TP4002AN	CD4002AE
TP4007AN	CD4007AE
TP4007UBN	CD4007UBE
TP4008AN	CD4008AE
TP4008BN	CD4008BE
TP4009AN	CD4009AE
TP4009UBN	CD4009UBE
TP4010AN	CD4010AE
TP4010BN	CD4010BE

Industry Type	RCA Replacement Type
TP4011AN	CD4011AE
TP4011BN	CD4011BE
TP4012AN	CD4012AE
TP4013AN	CD4013AE
TP4013BN	CD4013BE
TP4014AN	CD4014AE
TP4015AN	CD4015AE
TP4015BN	CD4015BE
TP4016AN	CD4016AE
TP4016UBN	CD4016BE
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TP4018BN	CD4018BE
TP4019AN	CD4019AE
TP4019BN	CD4019BE
TP4020AN	CD4020AE
TP4020BN	CD4020BE
TP4021AN	CD4021AE
TP4022AN	CD4022AE
TP4023AN	CD4023AE
TP4024AN	CD4024AE
TP4024BN	CD4024BE
TP4025AN	CD4025AE
TP4027AN	CD4027AE
TP4027BN	CD4027BE
TP4028AN	CD4028AE
TP4028BN	CD4028BE
TP4029AN	CD4029AE
TP4030AN	CD4030AE
TP4030BN	CD4030BE
TP4035BN	CD4035BE
TP4040AN	CD4040AE
TP4040BN	CD4040BE
TP4042AN	CD4042AE
TP4042BN	CD4042BE
TP4043AN	CD4043AE
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TP4044AN	CD4044AE
TP4044BN	CD4044BE
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TP4051BN	CD4051BE
TP4052AN	CD4052AE
TP4052BN	CD4052BE
TP4053AN	CD4053AE
TP4053BN	CD4053BE
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TP4070BN	CD4070BE
TP4071BN	CD4071BE
TP4072BN	CD4072BE
TP4073BN	CD4073BE
TP4075BN	CD4075BE
TP4081BN	CD4078BE
TP4082BN	CD4081BE
TP4083BN	CD4082BE
TP4511BN	CD4511BE
TP4512BN	CD4512BE
µPD4001C	CD4001AE

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Industry Type	RCA Replacement Type
μPD4002C	CD4002AE
μPD4011C	CD4011AE
μPD4012C	CD4012AE
μPD4013C	CD4013AE
μPD4014C	CD4014AE
μPD4015C	CD4015AE
μPD4017C	CD4017BE
μPD4019C	CD4019AE
μPD4020C	CD4020AE
μPD4021C	CD4021AE
μPD4023C	CD4023AE
μPD4024C	CD4024BE
μPD4025C	CD4025AE
μPD4027C	CD4027AE
μPD4028C	CD4028AE
μPD4029C	CD4029AE
μPD4030C	CD4030AE

Industry Type	RCA Replacement Type
μPD4034C	CD4034BE
μPD4035C	CD4035BE
μPD4040C	CD4040BE
μPD4042C	CD4042AE
μPD4043C	CD4043BE
μPD4044C	CD4044BE
μPD4049C	CD4049AE
μPD4050C	CD4050AE
μPD4051C	CD4051BE
μPD4052C	CD4052BE
μPD4053C	CD4053BE
μPD4063C	CD4063BE
μPD4066C	CD4066AE
μPD4069C	CD4069UBE
μPD4071C	CD4071BE
μPD4072C	CD4072BE
μPD4073C	CD4073BE

Industry Type	RCA Replacement Type
μPD4075C	CD4075BE
μPD4081C	CD4081BE
μPD4082C	CD4082BE
μPD4093C	CD4093BE
μPD4094C	CD4094BE
μPD4099C	CD4099BE
μPD4508C	CD4508BE
μPD4510C	CD4510BE
μPD4511C	CD4511BE
μPD4514C	CD4514BE
μPD4515C	CD4515BE
μPD4516C	CD4516BE
μPD4518C	CD4518BE
μPD4520C	CD4520BE
μPD4532C	CD4532BE
μPD4555C	CD4555BE
μPD4556C	CD4556BE

General Operating and Application Considerations

General Operating and Application Considerations

This section is intended as a guide to circuit and equipment designers in the operation and application of MOS integrated circuits. It covers general operating and handling considerations with respect to the following critical factors:

- Operating supply-voltage range
- Power dissipation and derating
- System noise considerations
- Power-source rules
- Gate-oxide protection networks
- Input signals and ratings
- Chip assembly and storage
- Device mounting
- Testing

More specific information is then given on significant features, special design and application requirements, and standard ratings and electrical characteristics for COS/MOS A- and B-series logic circuits, and on COS/MOS special - function circuits (telecommunications and special interface and display driver circuits).

GENERAL OPERATING AND HANDLING CONSIDERATIONS

The following paragraphs discuss some key operating and handling considerations that must be taken into account to achieve maximum advantage of the COS/MOS technology. Additional information on the operation and handling of COS/MOS integrated circuits is given in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits," included in the Application Notes Section of this DATABOOK.

Operating Supply-Voltage Range

Because logic systems occasionally experience transient conditions on the power-supply line which, when added to the nominal power-bus voltage, could exceed the safe limits of circuits connected to the power bus, the recommended operating supply-voltage ranges are 3 to 12 volts for A-series devices and 3 to 18 volts for B-series devices. The recommended maximum power-supply limit is substantially below the minimum primary breakdown limit for the devices to allow for limited power-supply transient and regulation limits. For circuits that operate in a linear mode over a portion of the voltage range, such as RC or crystal oscillators, a minimum supply voltage of 4 volts is recommended.

Power Dissipation and Derating

The power dissipation of a COS/MOS integrated circuit is the sum of a dc (quiescent) component and an ac (dynamic) component. The dc component is the sum of the net integrated-circuit reverse diode-junction current and the surface leakage current times the supply voltage. In standard A- or B-series logic devices, the dc dissipation typically ranges, depending upon device complexity, from 100 to 400 nanowatts for a supply voltage of 10 volts. Worst-case dc dissipation is the product of the maximum quiescent current (given in the data sheet on each device) and the dc supply voltage V_{DD}.

Dynamic power dissipation has 3 components:

a) The dissipation that results from current that charges and discharges the external load capacitance of the output buffers. The dissipation of each output buffer is equal to CV^2f, where C is the load capacitance, V is the supply voltage, and F is the switching frequency of that output.
b) The dissipation that results from current that charges and discharges the internal node capacitances.
c) The dissipation caused by the current spikes through the PMOS and NMOS transistors in series at the instant of switching. This component amounts to approximately 10 per cent of the total dissipation, shown graphically in the data sheets of most RCA COS/MOS circuits.

All COS/MOS devices are rated at 200 mW per package at the maximum operating ambient temperature rating (T_A) for the package type (85°C for plastic packages and 125°C for ceramic packages). Power ratings for temperatures below the maximum operating temperature are shown in the standard COS/MOS thermal derating chart in Fig. 1. This chart assumes that (a) the device is mounted and soldered (or placed in a socket) on a PC board; (b) there is natural convection cooling, with the PC board mounted horizontally; and (c) the pressure is standard (14.7 psia). In addition to the over-all package dissipation, device dissipation per output transistor is limited to 100 mW maximum over the full package operating-temperature range.

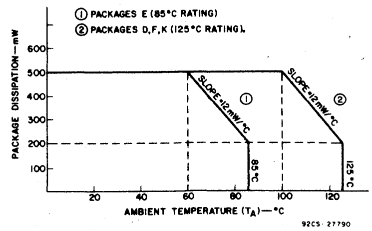


Fig. 1—Standard COS/MOS thermal derating chart.

System Noise Considerations

In general, COS/MOS devices are much less sensitive to noise on power and ground lines than bipolar logic families (such as TTL or DTL). However, this sensitivity varies as a function of the power-supply voltage, and more importantly as a function of synchronism between noise spikes and input transitions. Good power distribution in digital systems requires that the power bus have a low dynamic impedance; for this purpose, discrete decoupling capacitors should be distributed across the power bus. A more detailed discussion of COS/MOS noise immunity is provided by ICAN-6587, "Noise Immunity of B-series COS/MOS Integrated Circuits," in the Application Notes Section.

Power-Source Rules

Fig. 2 shows the basic COS/MOS inverter and its gate-oxide protection network plus inherent diodes. The safe operating procedures listed below can be understood by reference to this inverter:

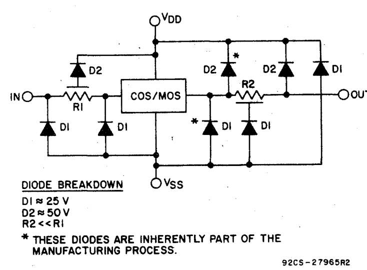


Fig. 2—Basic COS/MOS inverter with B-series types protection network.

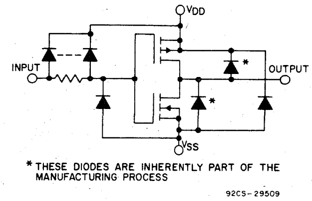
1. When separate power supplies are used for the COS/MOS device and for the device inputs, the device power supply should always be turned on

before the independent input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leq V_I \leq V_{DD}$ as a maximum limit). This rule will prevent overdissipation and possible damage to the D2 input-protection diode when the device power supply is grounded. When the device power supply is an open circuit, violation of this rule can result in undesired circuit operation although device damage should not result; ac inputs can be rectified by diode D2 to act as a power supply.

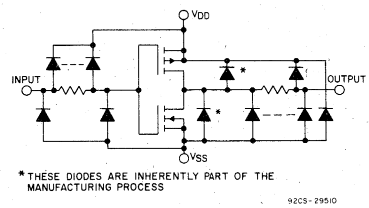
2. The power-supply operating voltage should be kept safely below the absolute maximum supply rating, as indicated previously.
3. The power-supply polarity for COS/MOS circuits should not be reversed. The positive (V_{DD}) terminal should never be more than 0.5 volt negative with respect to the negative (V_{SS}) terminal ($V_{DD} - V_{SS} > -0.5$ V). Reversal of polarities will forward-bias and short the structural and protection diode between V_{DD} and V_{SS}.
4. V_{DD} should be equal to or greater than V_{CC} for COS/MOS buffers which have two power supplies (except for the CD40109B, and in particular, for CD-4009 and CD4010 COS/MOS-to-TTL "down"-conversion devices).
5. Power-source current capability should be limited to as low a value as reasonable to assure good logic operation.
6. Large values of resistors in series with V_{DD} or V_{SS} should be avoided; transient turn-on of input protection diodes can result from drops across such resistors during switching.

Gate-Oxide Protection Network

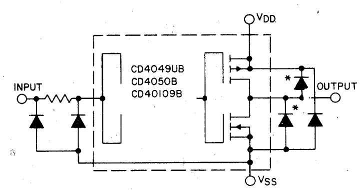
A problem occasionally encountered in handling and testing low-power semiconductor devices, including MOS and small-geometry bipolar devices, has been damage to gate oxide and/or p-n junctions. Fig. 3 shows the gate-oxide protection circuits used to protect COS/MOS devices from static electricity damage. ICAN-6572 gives further information on protection circuits. Although these circuits are included in all COS/MOS devices, the handling precautions in ICAN-6572 and ICAN-6525 should be observed.



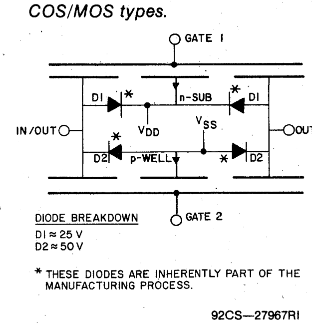
(a) For standard A-series COS/MOS product.



(b) For improved B-series COS/MOS product.



(c) For CD4049UB, CD4050B, and CD40109B COS/MOS types.



(d) For COS/MOS transmission gates.

Fig. 3—Gate-oxide protection networks used in RCA COS/MOS integrated circuits.

Input Signals and Ratings

1. Input signals should be maintained within the power-supply voltage range, $V_{SS} \leq V_I \leq V_{DD}$. If the input signal exceeds the recommended input-signal-swing range, the input current should be limited to ±100 μA to minimize cross talk between input signals on adjacent terminals, and also to minimize any reduction in noise immunity.

   The absolute-maximum input-current rating of ±10 mA, shown in the published data, protects the device against the possible occurence of an induced $V_{DD} - V_{SS}$ latch condition, or damage to the input protection diodes. Latch-up conditions are explained in ICAN-6525.
2. All COS/MOS inputs should be terminated. An exception can be made in the case of unbuffered NOR and NAND gates (A-series and UB types) where terminating one of the series inputs to the proper polarity will not permit current flow caused by a floating input. Thus, tying low one of the inputs of an unbuffered NAND gate, or tying high one of the inputs of an unbuffered NOR gate will satisfy this requirement.

   When COS/MOS inputs are wired to edge card connectors with COS/MOS drive coming from another PC board, a shunt resistor in the range of 100 kohms should be connected to V_{DD} or V_{SS}, as applicable, in case the inputs become unterminated with the power supply on.
3. When COS/MOS circuits are driven by TTL logic, a " pull-up" resistor should be connected from the COS/MOS input to 5 volts (further information is given in ICAN-6602).

Output Rules

1. The power dissipation in a COS/MOS package should not exceed the rated value for the ambient temperature specified. The actual dissipation should be calculated when (a) shorting outputs directly to V_{DD} or V_{SS}, (b) driving low-impedance loads, or (c) directly driving the base of p-n-p or n-p-n bi-polar transistor.
2. Output short circuits often result from testing errors or improper board assembly. Shorts on buffer outputs or across power supplies greater than 5 volts can damage COS/MOS devices.
3. COS/MOS, like active pull-up TTL, cannot be connected in the "wire-OR" configuration because an "on" PMOS and an "on" NMOS transistor

General Operating and Application Considerations

could be directly shorted across the power-supply rails. (Exception: CD-40107B)

4. Paralleling inputs and outputs of gates is recommended only when the gates are within the same IC package.
5. Output loads should return to a voltage within the supply-voltage range (V_{DD} to V_{SS}).
6. Large capacitive loads (greater than 5000 pF) on COS/MOS buffers or high-current drivers act like short circuits and may over-dissipate output transistors.
7. Output transistors may be over-dissipated by operating buffers as linear amplifiers or using these types as one-shot or astable multivibrators.

Noise Immunity and Noise Margin

The complementary structure of the inverter, common to all COS/MOS logic devices, results in a near-ideal input-output transfer characteristic, with switching point midway (45% to 55%) between the 0 and 1 output logic levels. The result is high dc noise immunity.

Fig. 4 shows a typical transfer curve that may be used to define the dc noise immunity of COS/MOS integrated circuits. The noise-immunity voltage (V_{IL} or V_{IH}) is the noise voltage at any one input that does not propagate through the system. Minimum noise immunity for buffered B-series COS/MOS devices is 30, 30, and 27 per cent, respectively for supply voltages V_{DD} of 5, 10, and 15 volts and 20 per cent of V_{DD} for all unbuffered gates. The V_{IL} and V_{IH} specifications define the maximum permissible additive noise voltage at an input terminal when input signals are within 50 millivolts of the supply rails.

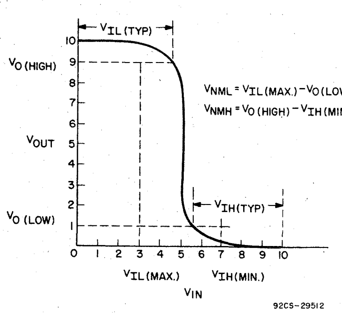


Fig. 4—Typical transfer curve for a inverting gate at V_{DD} = 10 V.

Noise margin is the difference between the noise-immunity voltage (V_{IL} or V_{IH}) and the output voltage V_O. Noise-margin voltage is the maximum voltage that can be impressed upon an input voltage V_{IN} (where V_{IN} is the V_{OL} or V_{OH} voltage of the preceding stage) at any (or all) logic I/O terminals without upsetting the logic or causing any output to exceed the output voltage (V_O) conditions specified for V_{IL} and V_{IH} ratings. Fig. 5 illustrates the noise-margin concept in a simple system. Minimum noise margins for buffered B-series COS/MOS devices are 1, 2, and 2.5 volts, respectively, for supply voltages of 5, 10, and 15 volts.

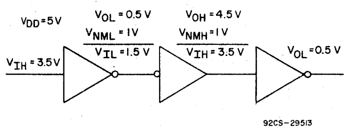


Fig. 5—Noise margin example using inverters.

Of the two noise-limitation specifications (noise immunity and noise margin), RCA considers noise immunity to be more practical for COS/MOS devices because COS/MOS outputs are normally within 50 millivolts of supply rails.

Noise immunity increases as the input pulse width becomes less than the propagation delay of the circuit. This condition is often described as ac noise immunity. (Further information on noise immunity is given in ICAN-6587).

Clock Rise- and Fall-Time Requirements

Most COS/MOS clocked devices have maximum rise- and fall-time ratings (normally 5 to 15 microseconds). With longer rise or fall times, a device may not function properly because of data ripple-through, false triggering problems, etc. Some B-series COS/MOS counters have Schmitt-trigger shaping circuits built into the clock circuit, removing the restriction for input rise or fall times. Long rise and fall times on COS/MOS buffer-type inputs cause increased power dissipation which may exceed device capability for operating power-supply voltages greater than 5 volts.

Parallel Clocking

Process variations leading to differences in input threshold voltage among random device samples can cause loss of data between certain synchronously clocked sequential circuits, as shown in Fig. 6. This problem can be avoided if the maximum clock rise time (t_rCL) for cascading any two CMOS sequential devices is limited in accordance with the following equations:

A Series Types

$$\text{Maximum } t_r\text{CL} = \frac{0.8\,V_{DD}\ (v)}{1.25\ (v)} \times t_p(ns)$$

B Series Types

$$\text{Maximum } t_r\text{CL} = \frac{0.8\,V_{DD}\ (v)}{1.15\ (v)} \times t_p(ns)$$

where $t_p = t_{PHL}$ or t_{PLH} (whichever is smaller) for the unit A in Fig. 6 as specified on the device data sheet at the specified value of V_{DD} and loading conditions. Schmitt trigger circuits such as the CD-4093B are an ideal solution to applications requiring wave-shaping.

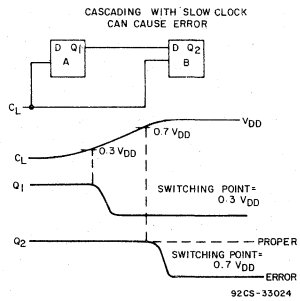


Fig. 6—Error effect that results from a slow clock in cascaded circuits.

Three-State Logic

Three-state logic can be easily implemented by use of a transmission gate in the output circuit; this technique provides a solution to the wire-OR problem in many cases.

Chip Assembly and Storage

RCA COS/MOS integrated circuits are provided in chip form (H suffix) to allow customer design of special and complex circuits to suit individual needs. COS/MOS chips are electrically identical to and offer the features of their counterparts sealed in ceramic and plastic packages. The following paragraphs describe mounting considerations, packaging, shipping and storage criteria, handling criteria, visual inspection criteria, testing criteria, and bonding pad layout and dimensions for each chip.

Mounting Considerations. All COS/MOS chips are non-gold backed and require the use of epoxy mounting. DuPont No's. 6838 or 5504A conductive silver paste or equivalent is recommended. In any case the manufacturer's recommendations for storage and use should be followed. If DuPont No., 6838 or 5504A paste is used, the bond should be cured at temperatures between 185°C and 200°C for 75 minutes.

In COS/MOS circuits MOS-transistor p-channel substrates (n-type bulk material) are connected to V_{DD}, therefore, when chips are mounted and a conductive paste is used care must be taken to keep the active substrate isolated from ground or other circuit elements.

Packing, Shipping, and Storage Criteria. Solid-state chips, being small in size and unencapsulated, are physically fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40°C max.
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment.
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to a moist and contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably affect their performance and/or reliability.

Handling Criteria. The user should find the following suggested precautions helpful in handling COS/MOS chips.

Because of the extremely small size and fragile nature of chips, the equipment designer should exercise care in handling these devices.

For additional handling considerations for COS/MOS devices, refer to ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

1. Grounding

a. Bonders, pellet pick-up tools, table tops, trim and form tools, sealing equipment, and other equipment used in chip handling should be properly grounded.
b. The operator should be properly grounded.

2. In-Process Handling

a. Assemblies or subassemblies of chips should be transported and stored in conductive carriers.
b. All external leads of the assemblies or subassemblies should be shorted together.

3. Bonding Sequence

a. Connect V_{DD} first to external connections, for example, terminal 14 of the CD4001AH.
b. Remaining functions may be connected to their external connections in any sequence.

4. Testing

a. Transport all assemblies of chips in conductive carriers.
b. In testing chip assemblies or subassemblies, the operator should be properly grounded.

Visual Inspection Criteria. All standard commercial COS/MOS chips undergo a visual inspection which is patterned after MIL-STD-883, Method 2010, Condition B with modifications reflecting COS/MOS requirements.

Testing Criteria. COS/MOS chips are dc electrically tested 100% in accordance with the same standards prescribed for RCA devices in standard packages.

Device Testing

RCA COS/MOS circuits are 100-percent tested by circuit probe in the wafer stage and are 100-percent tested again after they have been packaged. DC tests of RCA devices are performed at 5, 10, 15, and 20 volts; functionality is checked at 2.8, 17, and 20 volts depending on family (i.e., A or B series). Sample testing is used to assure adherence to quality requirements and ac specifications.

Static tests, high-speed functional and dc parametric tests, are performed at wafer and package stages by means of a Teradyne J283 test set. A Teradyne S157CM test set and a Marcodata MD154 test set are used in dynamic testing. Dynamic tests are performed with 15 and 50 picofarad loads. Testing at 15 picofarads is accomplished primarily by laboratory "bench-test" techniques; automatic testing at 15 picofarads is difficult because of the high input capacitance (approximately 20 to 35 picofarads) of most automatic ac test sets.

Users should follow the sequence below when testing COS/MOS devices:

1. Insert the device into the test socket.
2. Apply V_{DD}.
3. Apply the input signal.
4. Perform the test.
5. On completion of test, remove the input signal.
6. Turn off the power supply (V_{DD}).
7. Remove the device from the test socket and insert it into a conductive carrier. COS/MOS devices under test must not be exposed to electrostatic discharge or forward biasing of the intrinsic protective diodes shown in Fig. 3.

Detailed information on the techniques employed in the testing of RCA COS/MOS integrated circuits are described in ICAN-6532 included in the Application Notes section of this DATABOOK.

Device Mounting

Integrated circuits are normally supplied with lead-tin plated leads to facilitate soldering into circuit boards. In those relatively few applications requiring welding of the device leads, rather than soldering, the devices may be obtained with nickel-plated Kovar leads.* It should be recognized that this type of plating will not provide complete protection against lead corrosion in the presence of high humidity and mechanical stress.

*MIL-M-38510, paragraph 3,5,6,1 (a), lead material

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In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead. It is also extremely important that the ends of bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

A-SERIES COS/MOS INTEGRATED CIRCUITS

RCA CD4000A-series types have a maximum dc supply-voltage rating of −0.5 to 15 volts, and a recommended operating supply-voltage range of 3 to 12 volts. The major features of this series are as follows:

- Quiescent current specified to 15 volts
- 5-volt and 10-volt parametric ratings
- Maximum input leakage of 1 μA at 15 volts over the full package operating-temperature range
- 1-volt noise margin (full package temperature range)

Table I shows the maximum ratings and the recommended operating supply-voltage range for RCA A-series COS/MOS integrated circuits.

Static Electrical Characteristics

Table II shows the standard dc electrical characteristics for A-series types. The data sheet for each of these types contains the family characteristics shown in Table I plus additional dc characteristics that are type-dependent.

Dynamic Electrical Characteristics

A-series dynamic electrical characteristics are specified for individual types under the following conditions: $V_{DD} = 5$ V and 10 V; $T_A = 25°C$ (temperature coefficient is typically 0.3%/°C); $C_L = 15$ pF; t_r and t_f of inputs = 20 ns.

HIGH-VOLTAGE B-SERIES COS/MOS INTEGRATED CIRCUITS

RCA-CD4000B-series types have a maximum dc supply-voltage rating of −0.5 to 20 volts, and a recommended operating supply-voltage range of 3 to 18 volts. The major features of this series are as follows:

- High-voltage (20-V) ratings
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full-package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =

  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices

JEDEC Minimum Standard

Under the sponsorship of the Joint Electron Devices Engineering Council (JEDEC) of the Electronic Industries Association (EIA), minimum industrial standards have been established for the

Table I — Maximum Ratings and Recommended Operating Conditions for A-series COS/MOS Integrated Circuits

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, V_{DD} (Voltages referenced to V_{SS} terminal) .... −0.5 to +15V
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5 to V_{DD} +0.5 V
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (Package Type E) .... 500 mW
For T_A = +60 to +85°C (Package Type E) .... Derate Linearly to 200 mW
For T_A = −55 to +100°C (Package Types D, H) .... 500 mW
For T_A = +100 to +125°C (Package Types D, H) .... Derate Linearly to 100 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full package-temperature range (All package types) .... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
Package Types D, H .... −55 to +125°C
Package Type E .... −40 to +85°C
STORAGE-TEMPERATURE RANGE T_{STG}) .... −65 to 150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. .... +265° C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operaation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	12	V

Table II — A-Series Static Electrical Characteristics (Full Package Temperature Range)

SYMBOL	PARAMETER	CONDITIONS				LIMITS			UNITS
		V_{IN}	V_O (volts)		V_{DD}				
		VOLTS	MIN.	MAX.	VOLTS	MIN.	TYP.	MAX.	
V_{OL}	Output Low Voltage	5 10	— —	— —	5 10	— —	0 0	0.05 0.05	V V
V_{OH}	Output High Voltage	0 0	— —	— —	5 10	4.95 9.95	5 10	— —	V V
V_{NL} (SSI Types)	Noise Voltage (Input Low)	— —	3.6 7.2	— —	5 10	1.5 3	2.25 4.5	— —	V V
V_{NH} (SSI Types)	Noise Voltage (Input High)	— —	— —	1.4 2.8	5 10	1.5 3	2.25 4.5	— —	V V
V_{NL} (MSI Types)	Noise Voltage (Input Low)	— —	4.2 9.0	— —	5 10	1.5 3	2.25 4.5	— —	V V
V_{NH} (MSI Types)	Noise Voltage (Input High)	— —	— —	0.8 1.0	5 10	1.5 3	2.25 4.5	— —	V V
V_{NML}	Noise Margin (Input Low)	— —	4.5 9.0	— —	5 10	1 1	— —	— —	V V
V_{NMH}	Noise Margin (Input High)	— —	— —	0.5 1.0	5 10	1 1	— —	— —	V V
I_{IL}, I_{IH}	Input Leakage Low	—	—	—	15	—	$\pm 10^{-5}$	±1	μA
I_L	Quiescent Device Leakage	—	—	—	5, 10, 15	See Data Sheets			μA
I_{DN}, I_{DP}	Output Source and Sink current	—	—	—	5,10	See Data Sheets			mA

Note: Logic Level Inversion Assumed in Table II.

maximum ratings, static and ac electrical characteristics of B-series CMOS integrated circuits. The JEDEC standard (JEDEC Tentative Standard No. 13B) defines B-series CMOS integrated circuits as a uniform family of both buffered and unbuffered types that have an absolute dc supply-voltage rating of at least 18 volts.

Buffered CMOS devices are types in which the output "on" impedance is independent of any and all valid input logic conditions, both preceding and present. All such CMOS product are designated by the suffix "B" following the basic type number.

Unbuffered CMOS devices are types that meet all B-series specifications except that the logical outputs are not buffered and the noise-immunity voltages, V_{IL} and V_{IH}, are specified as 20 and 80 per cent, respectively, of V_{DD} for operation from 5 or 10 volts, and 17 and 83 per cent, respectively, of V_{DD} for operation from 15 volts. All such CMOS product are designated by the suffix "UB".

The JEDEC minimum standard also includes in the B-series CMOS types that have analog inputs or outputs and, in addition, have maximum ratings and logical input and output parameters that conform to B-series specifications wherever applicable. These CMOS devices are also designated by the suffix "B".

All B-series CMOS devices can directly replace their A-series counterparts in most applications. The UB types are high-voltage versions of corresponding A-series (unbuffered) types.

Table III lists the JEDEC minimum standards established for the maximum ratings and recommended operating conditions for B-series CMOS integrated circuits.

Table IV shows the JEDEC standards for the static electrical characteristics of CMOS B-series integrated circuits.

Standardized RCA Ratings and Static Characteristics

RCA B-series COS/MOS integrated circuits meet or exceed the most stringent requirements of the JEDEC B-series specifications. Table V shows the standardized maximum ratings and recommended operating supply-voltage range for RCA B-series COS/MOS integrated circuits. The standardized static electrical characteristics for these devices are shown in Table VI. As with the JEDEC specifications, the RCA standardized characteristics classifies the B-series devices into three leakage (quiescent-device-current) categories. Table VII lists the RCA types in each category and indicates types that, although they are still B-series types, differ in one or more static characteristics.

Tables V and VI show that, in a number of important respects, RCA has established new performance standards for B-series COS/MOS logic circuits:

1. **Tight limits for all packages**
   RCA devices use the same set of limits for all package styles. The JEDEC standard establishes two sets of limits for most dc (static) parameters; a

General Operating and Application Considerations

Table III – JEDEC Minimum Standards for Maximum Ratings and Recommended Operating Conditions for B-series CMOS Integrated Circuits*

Absolute Maximum Ratings (Voltages referenced to V_{SS}):

DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage	V_{IN}	−0.5 to V_{DD} +0.5	Vdc
DC Input Current (any one input)	I_{IN}	±10	mAdc
Storage-Temperature Range	T_S	−65 to +150	°C

Recommended Operating Conditions:

DC Supply Voltage	V_{DD}	+3 to +15	Vdc
Operating-Temperature Range, T_A			
Military-Range Devices		−55 to +125	°C
Commercial-Range Devices		−40 to +85	°C

*Reprinted from JEDEC Tentative Standard No. 13-B, "Standard Specifications for Description of B-Series CMOS Devices."

Table IV – JEDEC Standard for Static Characteristics of B-Series CMOS Integrated Circuits▲

PARAMETER		TEMP. RANGE	V_{DD} (Vdc)	CONDITIONS	LIMITS T_{LOW}* Min	T_{LOW}* Max	+25°C Min	+25°C Typ	+25°C Max	T_{HIGH}* Min	T_{HIGH}* Max	Units
I_{DD}	Quiescent Device Current GATES	Mil	5	$V_{IN} = V_{SS}$ or V_{DD}		0.25			0.25		7.5	uAdc
			10			0.5			0.5		15	uAdc
			15			1.0			1.0		30	uAdc
		Comm	5	All valid input combinations		1.0			1.0		7.5	uAdc
			10			2.0			2.0		15	uAdc
			15			4.0			4.0		30	uAdc
	BUFFERS, FLIP-FLOPS	Mil	5	$V_{IN} = V_{SS}$ or V_{DD}		1.0			1.0		30	uAdc
			10			2.0			2.0		60	uAdc
			15			4.0			4.0		120	uAdc
		Comm	5	All valid input combinations		4			4		30	uAdc
			10			8			8		60	uAdc
			15			16			16		120	uAdc
	MSI	Mil	5	$V_{IN} = V_{SS}$ or V_{DD}		5			5		150	uAdc
			10			10			10		300	uAdc
			15			20			20		600	uAdc
		Comm	5	All valid input combinations		20			20		150	uAdc
			10			40			40		300	uAdc
			15			80			80		600	uAdc
V_{OL}	Low-Level Output Voltage	All	5	$V_{IN} = V_{SS}$ or V_{DD}, $\|I_O\| < 1uA$		0.05			0.05		0.05	Vdc
			10			0.05			0.05		0.05	Vdc
			15			0.05			0.05		0.05	Vdc
V_{OH}	High-Level Output Voltage	All	5	$V_{IN} = V_{SS}$ or V_{DD}, $\|I_O\| < 1uA$	4.95		4.95			4.95		Vdc
			10		9.95		9.95			9.95		Vdc
			15		14.95		14.95			14.95		Vdc
V_{IL}	Input Low Voltage B Types	All	5	V_O = 0.5V or 4.5V		1.5			1.5		1.5	Vdc
			10	V_O = 1.0V or 9.0V		3.0			3.0		3.0	Vdc
			15	V_O = 1.5V or 13.5V, $\|I_O\| < 1uA$		4.0			4.0		4.0	Vdc
	UB Types	All	5	V_O = 0.5V or 4.5V		1.0			1.0		1.0	Vdc
			10	V_O = 1.0V or 9.0V		2.0			2.0		2.0	Vdc
			15	V_O = 1.5V or 13.5V, $\|I_O\| < 1uA$		2.5			2.5		2.5	Vdc
V_{IH}	Input High Voltage B Types	All	5	V_O = 0.5V or 4.5V	3.5		3.5			3.5		Vdc
			10	V_O = 1.0V or 9.0V	7.0		7.0			7.0		Vdc
			15	V_O = 1.5V or 13.5V, $\|I_O\| < 1uA$	11.0		11.0			11.0		Vdc
	UB Types	All	5	V_O = 0.5V or 4.5V	4.0		4.0			4.0		Vdc
			10	V_O = 1.0V or 9.0V	8.0		8.0			8.0		Vdc
			15	V_O = 1.5V or 13.5V, $\|I_O\| < 1uA$	12.5		12.5			12.5		Vdc

Table IV - JEDEC Standard for Static Characteristics of B-series CMOS Integrated Circuits (cont'd)

PARAMETER		TEMP. RANGE	V_{DD} (Vdc)	CONDITIONS	LIMITS T_{LOW}* Min	T_{LOW}* Max	+25° C Min	+25° C Typ	+25° C Max	T_{HIGH}* Min	T_{HIGH}* Max	Units
I_{OL}	Output Low (Sink) Current	Mil	5	V_O = 0.4V, V_{IN} = 0 or 5V	0.64		0.51			0.36		mAdc
			10	V_O = 0.5V, V_{IN} = 0 or 10V	1.6		1.3			0.9		
			15	V_O = 1.5V, V_{IN} = 0 or 15V	4.2		3.4			2.4		
		Comm	5	V_O = 0.4V, V_{IN} = 0 or 5V	0.52		0.44			0.36		
			10	V_O = 0.5V, V_{IN} = 0 or 10V	1.3		1.1			0.9		
			15	V_O = 1.5V, V_{IN} = 0 or 15V	3.6		3.0			2.4		
I_{OH}	Output High (Source) Current	Mil	5	V_O = 4.6V, V_{IN} = 0 or 5V	-0.25		-0.2			-0.14		mAdc
			10	V_O = 9.5V, V_{IN} = 0 or 10V	-0.62		-0.5			-0.35		
			15	V_O = 13.5V, V_{IN} = 0 or 15V	-1.8		-1.5			-1.1		
		Comm	5	V_O = 4.6V, V_{IN} = 0 or 5V	-0.2		-0.16			-0.12		
			10	V_O = 9.5V, V_{IN} = 0 or 10V	-0.5		-0.4			-0.3		
			15	V_O = 13.5V, V_{IN} = 0 or 15V	-1.4		-1.2			-1.0		
I_{IN}	Input Current	Mil	15	V_{IN} = 0 or 15V		±0.1			±0.1		±1.0	uAdc
		Comm	15	V_{IN} = 0 or 15V		±0.3			±0.3		±1.0	uAdc
I_{OUT}max	3-State Output Leakage Current	Mil	15	V_{IN} = 0 or 15V		±0.4			±0.4		±12	uAdc
		Comm	15	V_{IN} = 0 or 15V		±1.6			±1.6		±12	uAdc
C_{IN}	Input Capacitance per Unit Load	All	—	Any Input					7.5			pF

*T_{LOW} = −55° C for Military Temp. Range device, −40° C for Commercial Temp. Range device
*T_{HIGH} = +125° C for Military Temp. Range device, +85° C for Commercial Temp. Range device
▲ Reprinted from JEDEC Tentative Standard No. 13-B, "JEDEC Standard Specification for Description of B-series CMOS Devices."

tight set for products having a full operating temperature range of −55°C to +125°C (normally used for ceramic packages), and a relaxed set for products having a limited temperature range of −40°C to +85°C (normally used for plastic packages). Because RCA supplies only one premium grade of B-series product in all package styles (i.e., fall-out chips are *not* used), all B-series COS/MOS devices are specified to the tight set of limits only.

2. Improved voltage rating
All RCA B-series devices are tested to voltages that insure safe operation at the absolute maximum dc supply voltage rating of 20 volts. This higher rating permits greater derating for reliable 15-volt operation, permits greater 15-volt supply tolerance and peak transients, and permits system use to 18-volts with confidence.

3. Wider operating range
All RCA B-series devices have a recommended maximum operating voltage of 18 volts. This higher limit permits 18-volt system supply operation, and also permits wider power-source tolerances and transients for supplies normally set up to 18 volts.

4. Lower leakage current
The JEDEC standard establishes three sets of limits for quiescent device current (I_{DD}) intended to match chip complexity to device leakage current as realistically as possible.

General Operating and Application Considerations

Table V – RCA Standardized Maximum Ratings and Recommended Operating Conditions for B-Series COS/MOS Integrated Circuits

Maximum Ratings, Absolute-Maximum Values

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) .... –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS .... –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT .... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60° C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) .... Derate Linearly at 12mW/°C to 200 mW
For T_A = –55 to +100° C (PACKAGE TYPES D, F) .... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPES D, F) .... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) .... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H .... –55 to +125° C
PACKAGE TYPE E .... –40 to +85° C
STORAGE-TEMPERATURE RANGE (T_{stg}) .... –65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max .... +265° C

Recommended Operating Conditions:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

For all three levels of chip complexity, all RCA B-series devices (regardless of package) conform to the tighter set of limits established in the standard. In addition, a maximum rating is specified at 20V, as well as at 5V, 10V, and 15V. As a result:

(a) In current-limited applications, COS/MOS users can depend on one tight leakage limit independent of package style selected.

(b) Customer use of COS/MOS product up through 18 volts is protected by a published tight leakage current specification at 20 volts (as well as by an input leakage specification at 18 volts).

5. Symmetrical output

Most RCA B-series devices have balanced complementary output drive (i.e., the output high current I_{OH} rating is the same as the output low current I_{OL} rating) specified to the tighter set of limits established in the JEDEC standard. The balanced output provides uniform rise and fall time performance, improved system noise energy (dynamic) immunity, optimum device speed for both output switching low-to-high (t_{PLH}) and output switching high-to-low (t_{PHL}), and in general the identical high and low dc and ac characteristics normally associated with a good complementary output drive circuit. MOS system design, simulation, and performance are significantly enhanced by equal high and low dc and ac performance ratings and one tight specification limit for all package styles.

6. Improved input current (leakage) ratings

All RCA B-series devices (regardless of package) have a maximum input leakage current (I_{IN}) rating of 100 nA specified at voltages up to 18 V, and a maximum limit of 1 μA at the upper limit of the package-temperature range. Actually, the 100 nA rating is a practical specification limited by the inability of commercial test equipment to measure lower currents. Laboratory tests show that input leakage currents of RCA B-series COS/MOS devices are significantly lower than this limit, typically ranging from 10 to 100 pA.

7. Buffered and unbuffered gates

The new industry standard establishes a suffix "UB" for CMOS products that meet all B-series specifications except that the logical outputs of the devices are not buffered and the V_{IL} and V_{IH} specifications are relaxed. The suffix "B" defines only buffered-output devices in which the output "on" impedance is independent of any and all valid input logic conditions, both preceding and present.

General Operating and Application Considerations

Table VI – RCA B-Series COS/MOS Standardized Electrical Characteristics

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D,F,H Packages Values at -40, +25, +85 Apply to E Package -55	-40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max. Gates, Inverters▲	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Buffers, Flip-Flops, Latches, Multi-Level Gates (MSI-1 Types)▲		0,5	5	1	1	30	30	–	0.02	1	
		0,10	10	2	2	60	60	–	0.02	2	
		0,15	15	4	4	120	120	–	0.02	4	
		0,20	20	20	20	600	600	–	0.04	20	
Complex Logic (MSI-2 Types)▲		0,5	5	5	5	150	150	–	0.04	5	
		0,10	10	10	10	300	300	–	0.04	10	
		0,15	15	20	20	600	600	–	0.04	20	
		0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	–	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	–	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max. B Types	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5, 13.5	–	15	4				–	–	4	
UB Types	0.5, 4.5	–	5	1				–	–	1	
	1,9	–	10	2				–	–	2	
	1.5, 13.5	–	15	2.5				–	–	2.5	
Input High Voltage, V_{IH} Min. B Types	0.5, 4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5, 13.5	–	15	11				11	–	–	
UB Types	0.5, 4.5	–	5	4				4	–	–	
	1,9	–	10	8				8	–	–	
	1.5, 13.5	–	15	12.5				12.5	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0, 18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	μA

▲Classifications of RCA COS/MOS B-Series Types are shown in Table VII.

General Operating and Application Considerations

Table VII — Classification of RCA B-series COS/MOS Integrated Circuits According to Circuit Complexity

Gates/ Inverters		Buffers/Flip-Flop/ Latches/Multi-Level Gates (MSI-1)		Complex Logic (MSI-2)		
CD4000B	CD4023UB	CD4009UB■	CD4070B	CD4006B	CD4051B■	CD4527B
CD4000UB	CD4025B	CD4010B■	CD4077B	CD4008B	CD4052B■	CD4532B
CD4001B	CD4025UB	CD4013B	CD4085B	CD4014B	CD4053B■	CD4536B
CD4001UB	CD4048B	CD4019B	CD4086B	CD4015B	CD4054B■	CD4538B
CD4002B	CD4066B■	CD4027B	CD4093B	CD4017B	CD4055B■	CD4555B
CD4002UB	CD4068B	CD4030B	CD4095B	CD4018B	CD4056B■	CD4556B
CD4007UB	CD4069UB	CD4041UB■	CD4096B	CD4020B	CD4060B	CD4585B
CD4011B	CD4071B	CD4042B	CD4098B	CD4021B	CD4063B	CD4724B
CD4011UB	CD4072B	CD4043B	CD4502B■	CD4022B	CD4067B■	CD40100B
CD4012B	CD4073B	CD4044B	CD4503B	CD4024B	CD4076B	CD40101B
CD4012UB	CD4075B	CD4047B	CD40106B	CD4026B	CD4089B	CD40102B
CD4016B■	CD4078B	CD4049UB■	CD40107B■	CD4028B	CD4094B	CD40103B
CD4023B	CD4081B	CD4050B■	CD40109B■	CD4029B	CD4097B■	CD40104B
	CD4082B		CD40174B	CD4031B	CD4099B	CD40105B
			CD40257B	CD4032B	CD4508B	CD40108B
				CD4033B	CD4510B	CD40110B■
				CD4034B	CD4511B■	CD40147B
				CD4035B	CD4512B	CD40160B
				CD4038B	CD4514B	CD40161B
				CD4040B	CD4515B	CD40162B
				CD4045B■	CD4516B	CD40163B
				CD4046B■	CD4517B	CD40181B
					CD4518B	CD40182B
					CD4520B	CD40192B
						CD40193B
						CD40194B
						CD40208B

■Indicates types for which, because of special design requirements, one or more static characteristics differ from the standardized data. Refer to RCA data pages on these types for specific differences.

RCA will supply both buffered ("B") and unbuffered ("UB") versions of the popular NOR and NAND gates to make available to designers the advantages of both. The chart below briefly compares the features of the two versions (a more detailed coverage of the special features of B- and UB-series COS/MOS gates is provided by ICAN-6558 in the Application-Notes section):

Characteristic	Buffered Version ("B")	Unbuffered Version ("UB")
Propagation Delay (Speed)	Moderate	Fast
Noise Immunity/Margin	Excellent	Good
Output Impedance and Output Transition Time	Constant	Variable
AC Gain	High	Medium
Output Oscillation for Slow Inputs	Yes	No
Input Capacitance	Low	High

8. Reliability

RCA B-series COS/MOS integrated circuits incorporate the latest improvements in processing technology and plastic and ceramic packaging techniques. Product quality is real-time controlled using accelerated-temperature group quality screening in which measured dc parameters are criticized against tight B-series limits.

Figs. 7 through 10 show the standardized n- and p-channel drain characteristics for B-series COS/MOS devices, and Figs. 11 through 14 show the normalized variation of output source and sink currents with respect to temperature and voltage in these devices.

B-Series Dynamic Electrical Characteristics

B-series dynamic electrical characteristics are specified for individual types under the following conditions: $V_{DD} = 5V$; 10V, and 15V; $T_A = 25° C$; $C_L = 50$ pF; $R_L = 200$ kΩ; t_r and $t_f = 20$ ns. Table VIII lists dynamic characteristics specified for RCA B-series COS/MOS integrated circuits. Fig. 13 shows the variation of B-series dynamic parameters with temperature. Fig. 14 shows the variation of output transition time with supply voltage. Fig. 15 shows the variation of the standardized output transition time with load capacitance.

Maximum propagation delay or transition times for values of C_L other than the specified 50 picofarads can be determined by use of the multiplication factor (usually 2) between the typical and maximum values given in the dynamic characteristics chart included in the technical data for each device applied to the typical curves, and also shown in the device technical data.

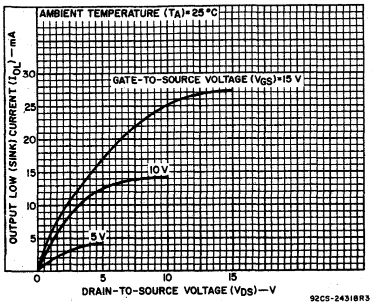


Fig. 7 — Typical output low (sink) current characteristics.

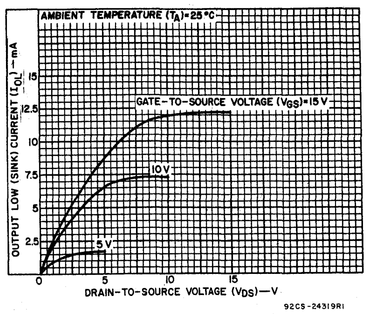


Fig. 8 — Minimum output low (sink) current characteristics.

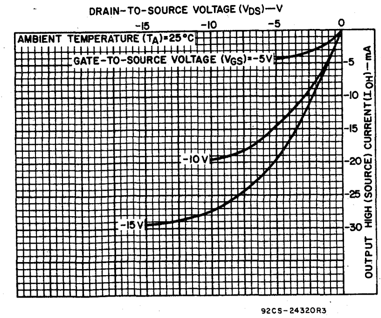


Fig. 9 — Typical output high (source) current characteristics.

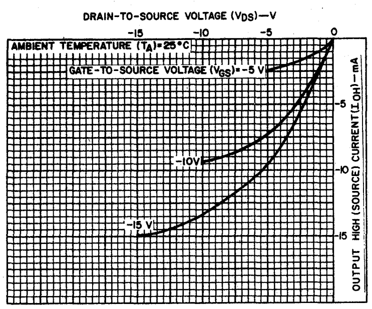


Fig. 10 — Minimum output high (source) current characteristics.

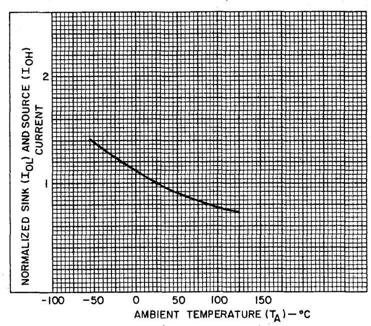


Fig. 11—Variation of normalized output low (sink) current I_{OL} and output high (source) current I_{OH} with temperature.

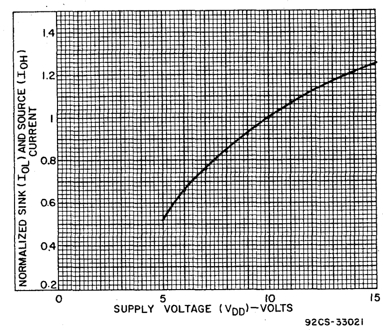


Fig. 12—Variation of normalized output low (sink) current I_{OL} and output high (source) current I_{OH} with supply voltage.

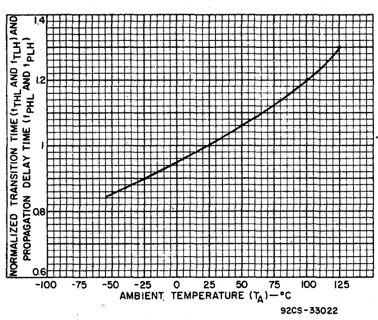


Fig. 13—Variation of low-to-high (t_{TLH}) and high to low (t_{THL}) transition time, and low-to-high (t_{PLH}) and high-to-low (t_{PHL}) propagation delay time with temperature.

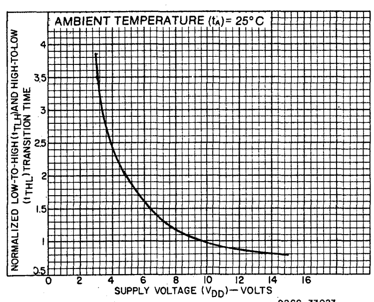


Fig. 14—Variation of low-to-high (t_{TLH}) and high-to-low (t_{THL}) transition time with supply voltage.

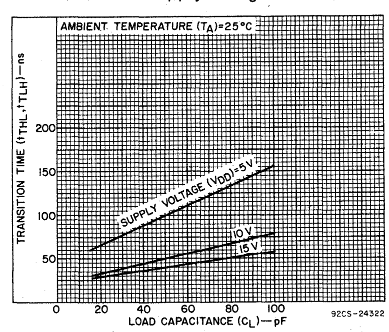


Fig. 15—Variation of transition time (t_{THL}, t_{TLH}) with load capacitance.

B-Series Dynamic (AC) Switching Parameters

Table VIII defines the major COS/MOS ac characteristics, with reference to the waveforms shown in Figs. 16 through 19. Test conditions of V_{DD}, low capacitance (C_L), and input conditions are given for individual types in the published data.

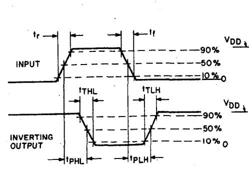
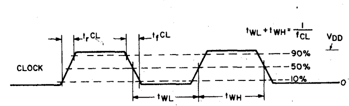


Fig. 16 — Transition times and propagation delay times, combination logic.



Outputs should be switching from 10% V_{DD} to 90% V_{DD} in accordance with device truth table.

Fig. 17 — Clock-pulse rise and fall times and pulse width.

General Operating and Application Considerations

Table VIII - Dynamic Electrical Characteristics - Definitions

Characteristic	Symbol	Limits		Notes
		Max.	Min.	
Propagation Delay:				
Outputs going high to low	t_{PHL}	X		
Outputs going low to high	t_{PLH}	X		
Output Transition Time:				
Outputs going high to low	t_{THL}	X		
Outputs going low to high	t_{TLH}	X		
Pulse Width-Set, Reset, Preset Enable, Disable, Strobe, Clock	t_{WL} or t_{WH}		X	1
Clock Input Frequency	f_{CL}	X		1,2
Clock Input Rise and Fall Time	t_{rCL}, t_{fCL}	X		
Set-Up Time	t_{SU}		X	1
Hold Time	t_H		X	1
Removal Time - Set, Reset, Preset-Enable	t_{REM}		X	1
Three State Disable Delay Times:				
High level to high impedance	t_{PHZ}	X		
High impedance to low level	t_{PZL}	X		
Low level to high impedance	t_{PLZ}	X		
High impedance to high level	t_{PZH}	X		

NOTE: (1) By placing a defining min. or max. in front of definition, the limits can change from min. to max., or vice versa.

(2) Clock input waveform should have a 50% duty cycle and be such as to cause the outputs to be switching from 10% V_{DD} to 90% V_{DD} in accordance with the device truth table.

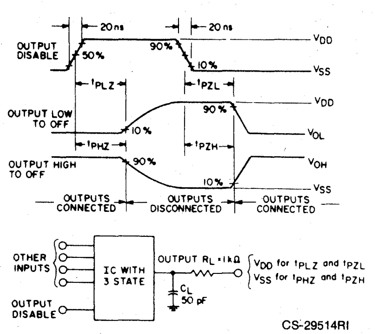


Fig. 18 — Three-state propagation delay wave shapes and test circuit.

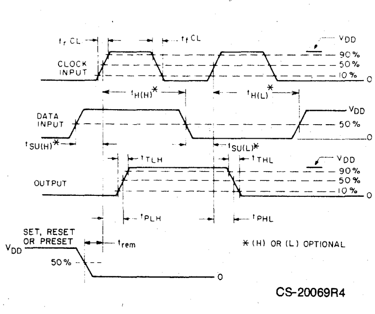


Fig. 19 — Setup times, hold times, removal time, and propagation delay times for positive-edge triggered sequential logic circuits.

COS/MOS Special Products

RCA supplies a variety of special COS/MOS products that have operating supply-voltage ranges and other characteristics that differ from the standardized data specified for A- and B-series COS/MOS integrated circuits.

These special applications types include **crosspoint switches** for use in telephone and PBX systems, in studio audio switching applications, and as multisystem bus interconnects; **tone generators** for use in dual-tone telephone dialing systems; **interface circuits** for level-shifting applications to interface CMOS logic levels with different logic types; and **display drivers** non-multiplexed, 4-digit, 7-segment LCD types containing all the circuitry necessary for driving conventional LCD displays without the need for external components.

COS/MOS High-Voltage B-Series Integrated Circuits

Technical Data

CD4000B, CD4001B, CD4002B, CD4025B Types

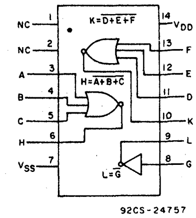
COS/MOS NOR Gates

High-Voltage Types (20-Volt Rating)
Dual 3 Input
plus Inverter – CD4000B
Quad 2 Input – CD4001B
Dual 4 Input – CD4002B
Triple 3 Input – CD4025B

RCA-CD4000B, CD4001B, CD4002B, and CD4025B NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of COS/MOS gates. All inputs and outputs are buffered.
The CD4000B, CD4001B, CD4002B, and CD4025B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

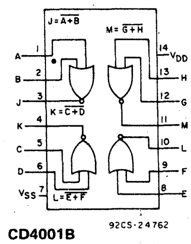
Features:

- **Propagation delay time = 60 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V**
- **Buffered inputs and outputs**
- **Standardized symmetrical output characteristics**
- **100% tested for maximum quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package temperature range):**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of "B" Series CMOS Devices"**



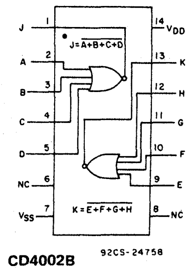
92CS-24757

CD4000B FUNCTIONAL DIAGRAM



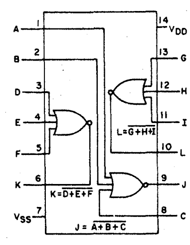
92CS-24762

CD4001B FUNCTIONAL DIAGRAM



92CS-24758

CD4002B FUNCTIONAL DIAGRAM



92CS-24760

CD4025B FUNCTIONAL DIAGRAM

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages Values at –40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				—	—	1.5	V
	1,9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5	–	5	3.5				3.5	—	—	
	1	–	10	7				7	—	—	
	1.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200kΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

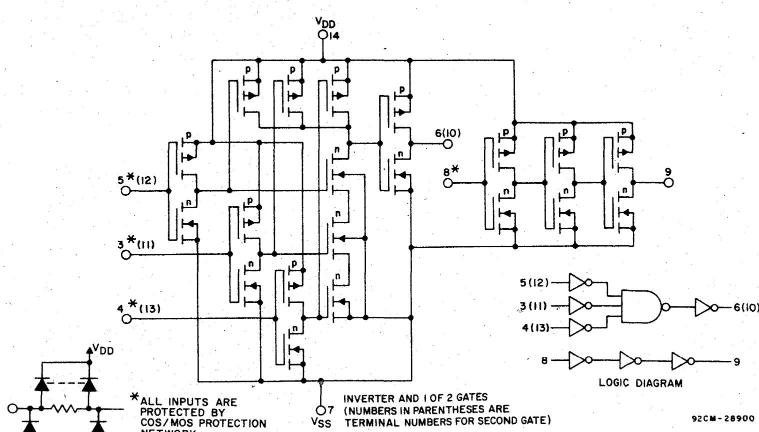


Fig.4 — Schematic and logic diagrams for CD4000B.

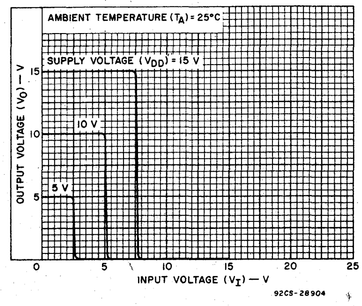


Fig.1 — Typical voltage transfer characteristics.

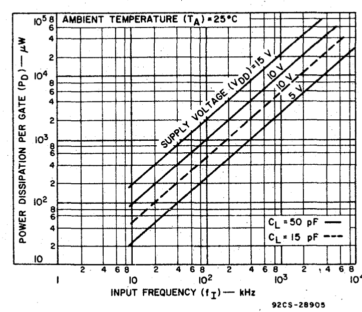


Fig.2 — Typical power dissipation vs. frequency.

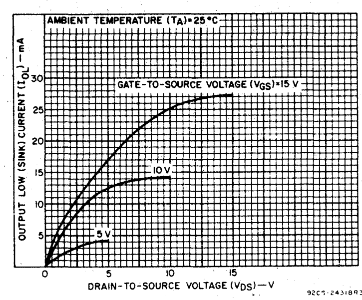


Fig.3 — Typical output low (sink) current characteristics.

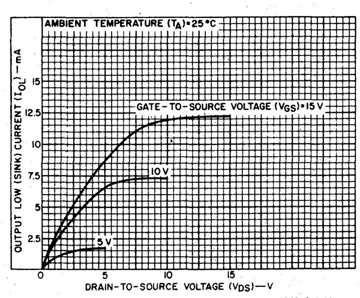


Fig.5 — Minimum output low (sink) current characteristics.

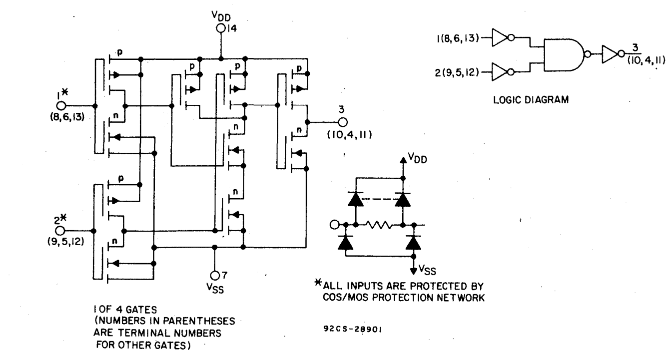


Fig.6 – Schematic and logic diagrams for CD4001B.

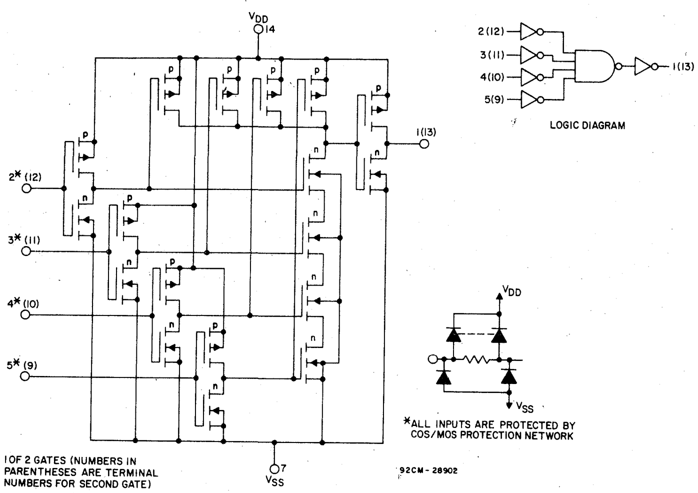


Fig.7 – Schematic and logic diagrams for CD4002B.

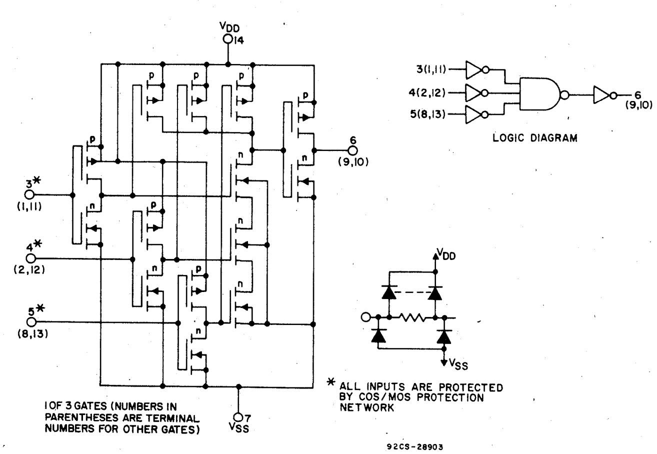


Fig.8 – Schematic and logic diagrams for CD4025B.

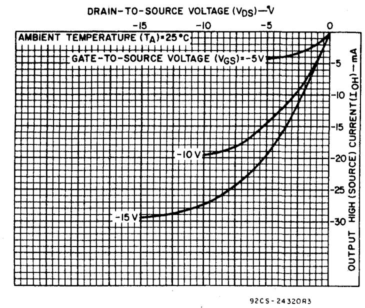


Fig.9 – Typical output high (source) current characteristics.

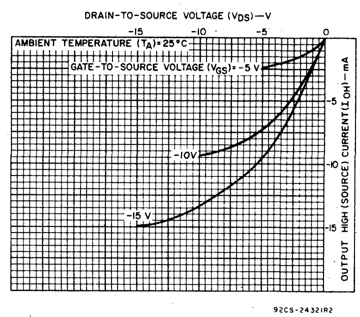


Fig.10 – Minimum output high (source) current characteristics.

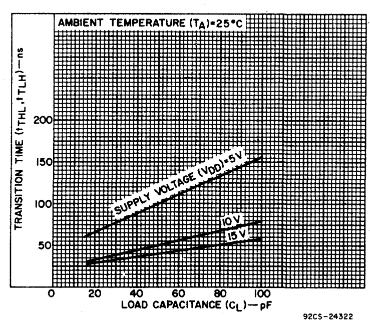


Fig.11 – Typical transition time vs. load capacitance.

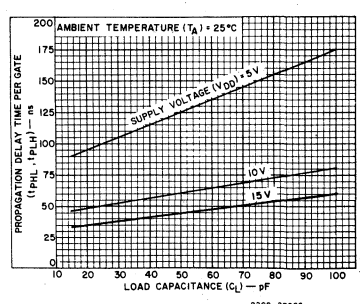


Fig.12 – Typical propagation delay time vs. load capacitance.

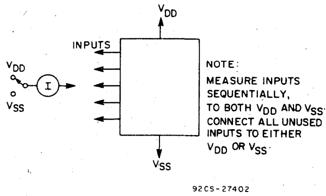


Fig. 13 – Input leakage current test circuit.

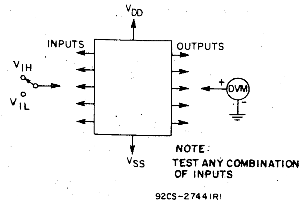


Fig. 14 – Input-voltage test circuit.

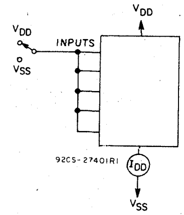
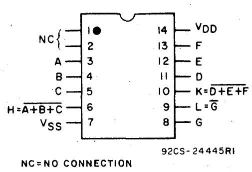
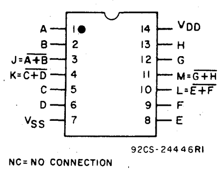


Fig. 15 – Quiescent-device current test circuit.

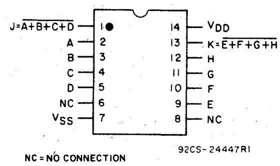
TERMINAL ASSIGNMENTS (TOP VIEW)



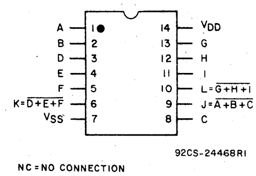
CD4000B



CD4001B



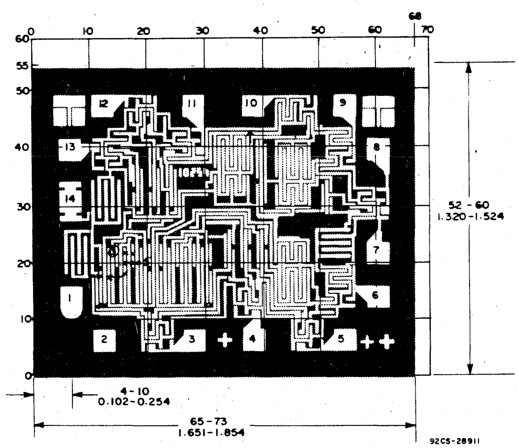
CD4002B



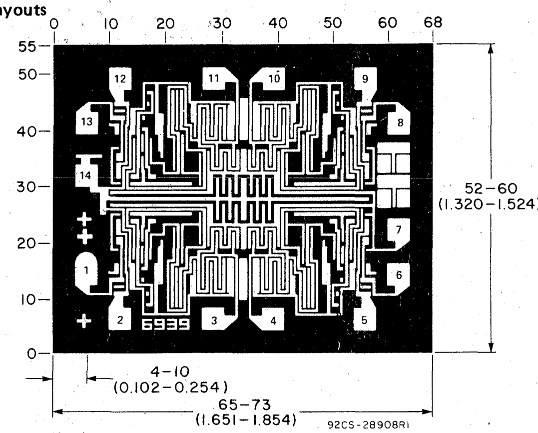
CD4025B

CHIP PHOTOGRAPHS

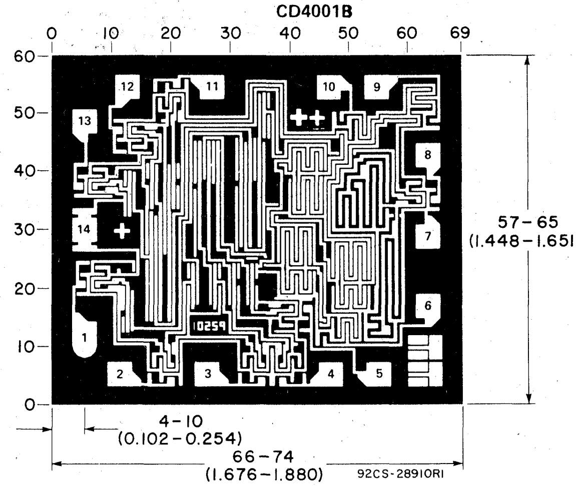
Dimensions and Pad Layouts



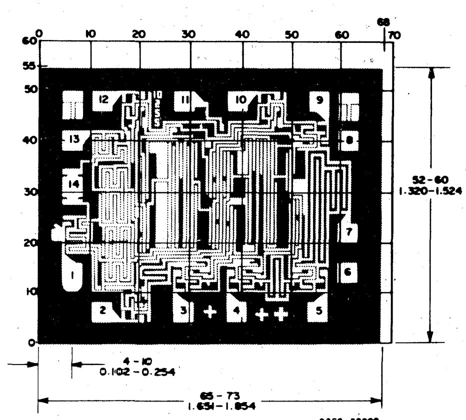
CD4000B



CD4001B



CD4025B



CD4002B

CD4000UB, CD4001UB, CD4002UB, CD4025UB Types

COS/MOS NOR Gates

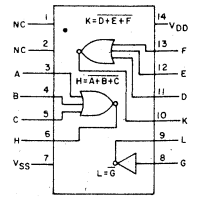
High-Voltage Types (20-Volt Rating)
Dual 3 Input
plus Inverter—CD4000UB
Quad 2 Input-CD4001UB
Dual 4 Input—CD4002UB
Triple 3 Input—CD4025UB

RCA-CD4000UB, CD4001UB, CD4002UB, and CD4025UB NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of COS/MOS gates.

The CD4000UB, CD4001UB, CD4002UB, and CD4025UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

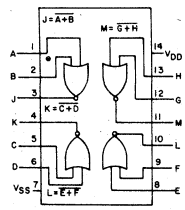
Features:

- Propagation delay time = 30 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V
- Standardized symmetrical output characteristics
- 100% tested for maximum quiescent current at 20 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings



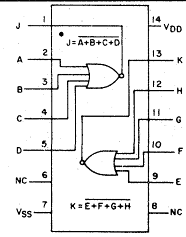
92CS-24757

CD4000UB FUNCTIONAL DIAGRAM



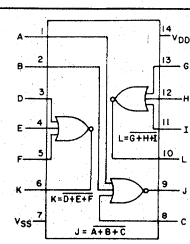
92CS-24762

CD4001UB FUNCTIONAL DIAGRAM



92CS-24758

CD4002UB FUNCTIONAL DIAGRAM



92CS-24760

CD4025UB FUNCTIONAL DIAGRAM

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1				–	–	1	V
	1, 9	–	10	2				–	–	2	
	1.5,13.5	–	15	2.5				–	–	2.5	
Input High Voltage, V_{IH} Min.	0.5	–	5	4				4	–	–	
	1	–	10	8				8	–	–	
	1.5	–	15	12.5				12.5	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

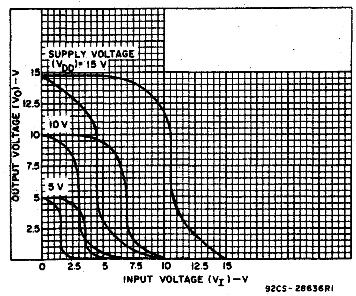


Fig. 1 – Minimum and maximum voltage transfer characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

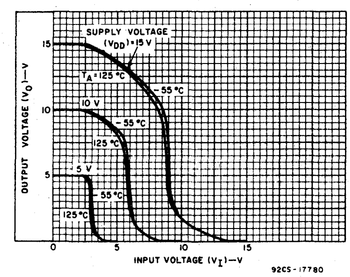


Fig. 2 – Typical voltage transfer characteristics as a function of temperature.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, and C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} Volts	ALL TYPES LIMITS TYP.	ALL TYPES LIMITS MAX.	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH}		5	60	120	ns
		10	30	60	
		15	25	50	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		10	15	pF

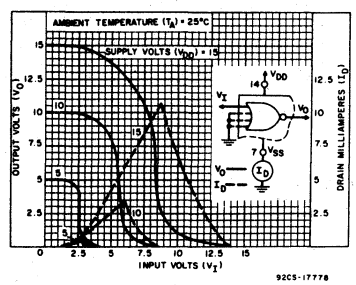


Fig. 3 – Typical current & voltage transfer characteristics.

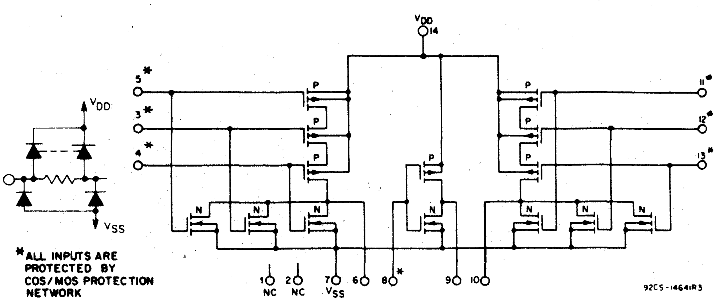


Fig. 4 – Schematic diagram for type CD4000UB.

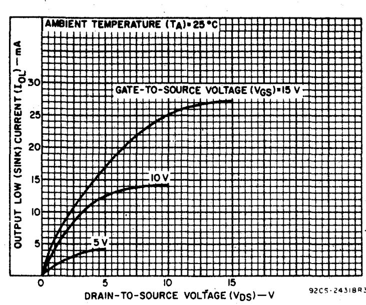


Fig. 5 – Typical output low (sink) current characteristics.

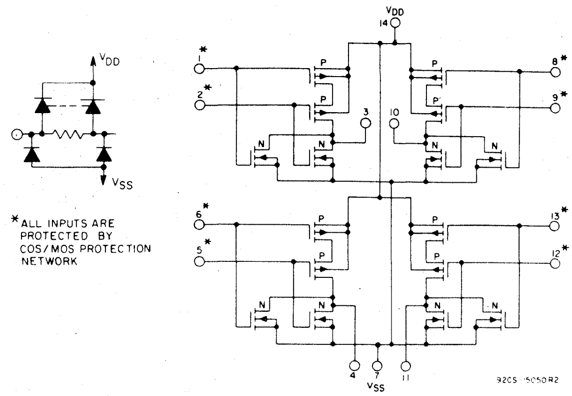


Fig. 6 – Schematic diagram for type CD4001UB.

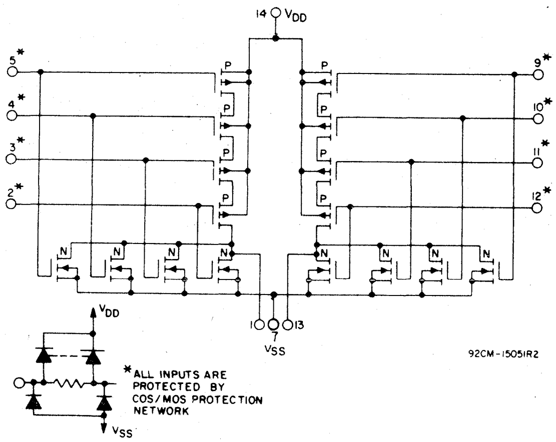


Fig. 7 – Schematic diagram for type CD4002UB.

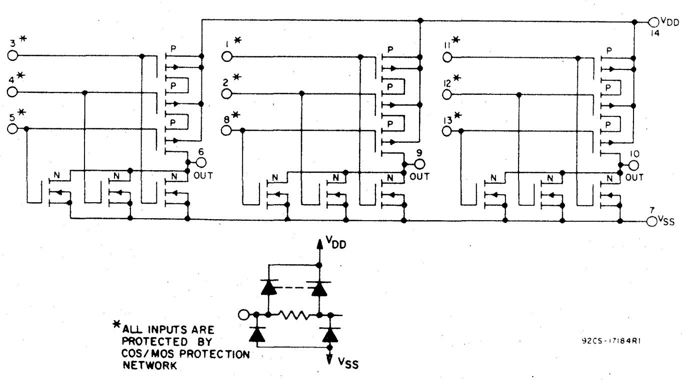


Fig. 8 – Schematic diagram for type CD4025UB.

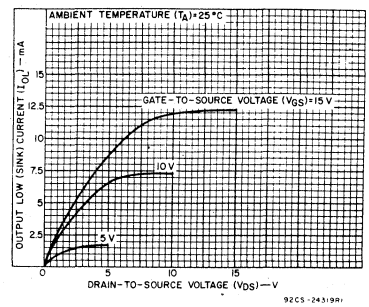


Fig. 9 – Minimum output low (sink) current characteristics.

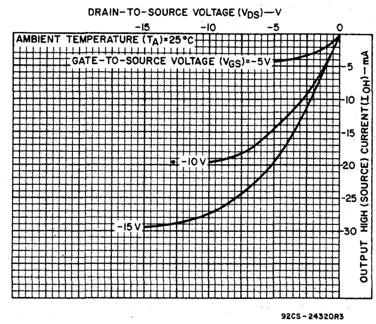


Fig. 10 – Typical output high (source) current characteristics.

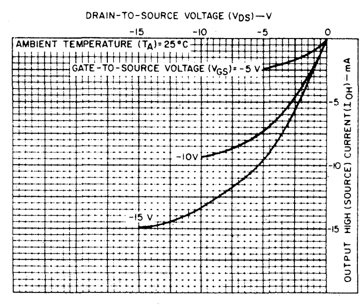


Fig. 11 – Minimum output high (source) current characteristics.

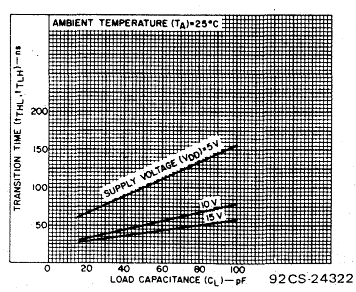


Fig. 12 – Typical transition time vs. load capacitance.

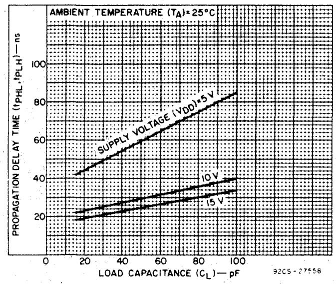


Fig. 13 – Typical propagation delay time vs. load capacitance.

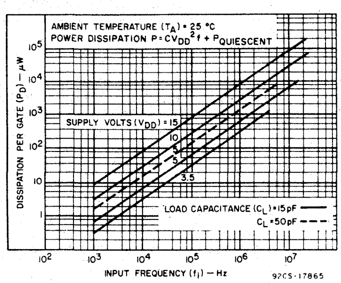


Fig. 14 – Typical power dissipation vs. frequency.

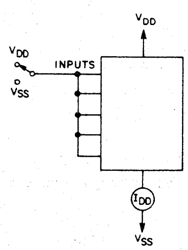


Fig. 15 – Quiescent-device-current test circuit.

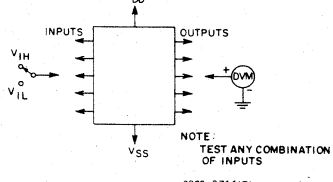


Fig. 16 – Input-voltage test circuit.

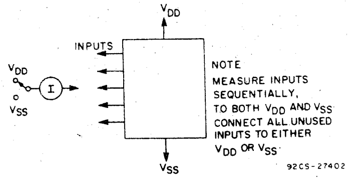
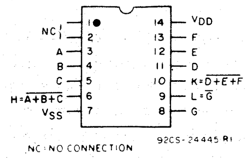
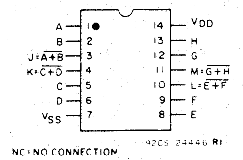


Fig. 17 – Input leakage current test circuit.

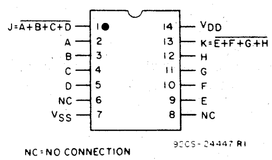
TERMINAL ASSIGNMENTS



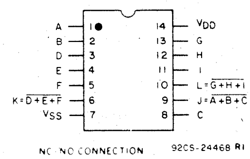
CD4000UB



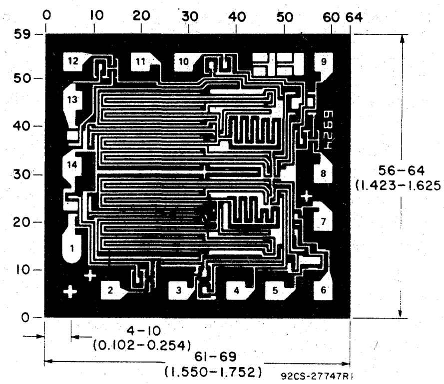
CD4001UB



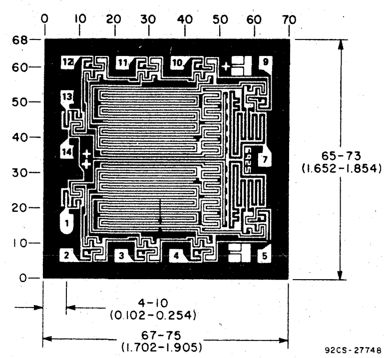
CD4002UB



CD4025UB

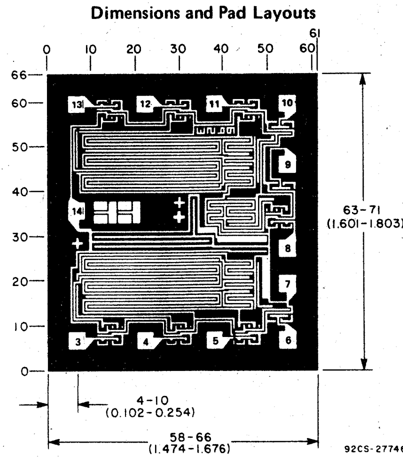


CD4001UB



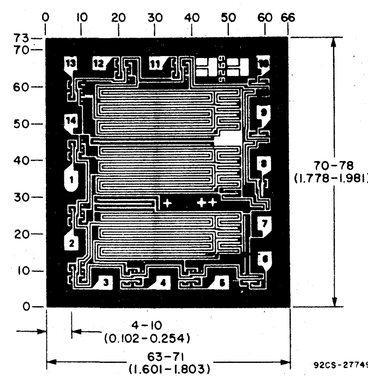
CD4002UB

CHIP PHOTOGRAPHS
Dimensions and Pad Layouts



CD4000UB

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).



CD4025UB

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4006B Types

COS/MOS 18-Stage Static Shift Register

High-Voltage Types (20-Volt Rating)

The RCA-CD4006B types are composed of 4 separate shift register sections: two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent single-rail data path.

A common clock signal is used for all stages. Data are shifted to the next stage on negative-going transitions of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17 and 18 stages can be implemented using one CD4006B package. Longer shift register sections can be assembled by using more than one CD4006B.

To facilitate cascading stages when clock rise and fall times are slow, an optional output (D_1+4') that is delayed one-half clock-cycle, is provided (see Truth Table for Output from Term. 2).

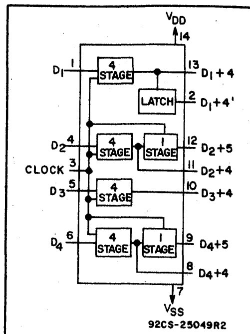
The CD4006B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

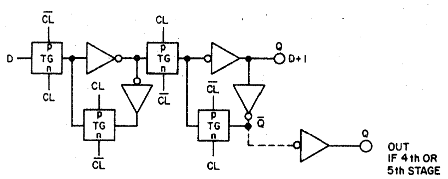
- Fully static operation
- Shifting rates up to 12 MHz @ 10 V (typ.)
- Permanent register storage with clock line high or low — no information recirculation required
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Serial shift registers
- F requency division
- Time delay circuits



FUNCTIONAL DIAGRAM



TRUTH TABLE FOR SHIFT REGISTER STAGE

D	CL▲	D + 1
0	⟍ (falling)	0
1	⟍ (falling)	1
X	⟋ (rising)	NC

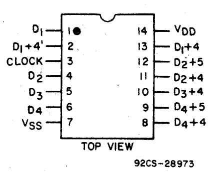
TRUTH TABLE FOR OUTPUT FROM TERM.2

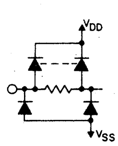
D_1+4	CL▲	D_1+4'
0	⟋ (rising)	0
1	⟋ (rising)	1
X	⟍ (falling)	NC

1 = HIGH X = DON'T CARE
0 = LOW ▲ = LEVEL CHANGE
NC = NO CHANGE

Fig. 1 – Logic diagram and truth table (one register stage).

TERMINAL ASSIGNMENT





ALL INPUTS (TERMINALS 1,3,4,5,6) PROTECTED BY COS/MOS PROTECTION NETWORK

92CS-28974

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	18	V
Clock Pulse Width, t_W	5	180	–	ns
	10	80	–	
	15	50	–	
Data Setup Time, t_S	5	100	–	ns
	10	50	–	
	15	40	–	
Data Hold Time, t_H	5	60	–	ns
	10	40	–	
	15	30	–	
Clock Rise or Fall Time: t_r, t_f	5,10, 15	–	15	μS
Clock Input Frequency, f_{CL}	5	–	2.5	MHz
	10	–	5	
	15	–	7	

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

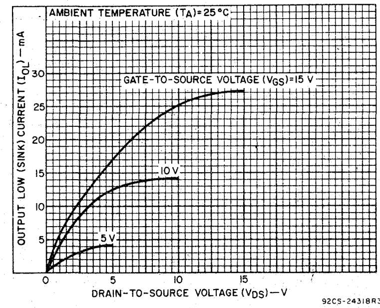


Fig. 2 – Typical output low (sink) current characteristics.

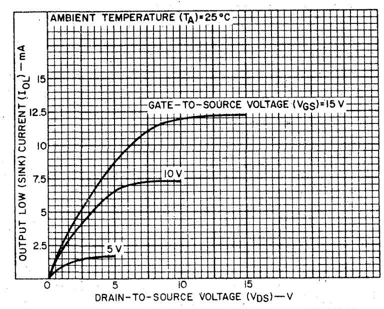


Fig. 3 – Minimum output low (sink) current characteristics.

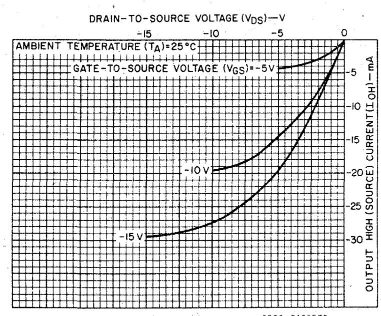


Fig. 4 – Typical output high (source) current characteristics.

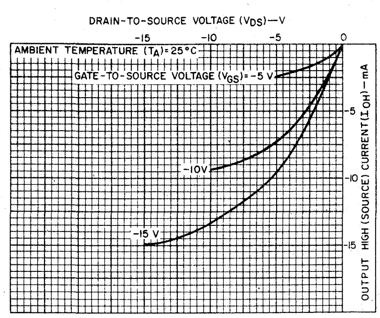


Fig. 5 – Minimum output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25^oC$; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ*

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH}	5 10 15	200 100 80	ns
Transition Time, t_{THL}, t_{TLH}	5 10 15	100 50 40	ns
Minimum Data Setup Time, t_S	5 10 15	50 25 20	ns
Minimum Clock Pulse Width, t_W	5 10 15	100 45 30	ns
Maximum Clock Input Frequency, f_{CL}	5 10 15	5 12 16	MHz
Maximum Clock Input Rise or Fall Time t_rCL, t_fCL*	5 10 15	15 15 15	μs
Input Capacitance, C_{IN}	Any Input	5	pF

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

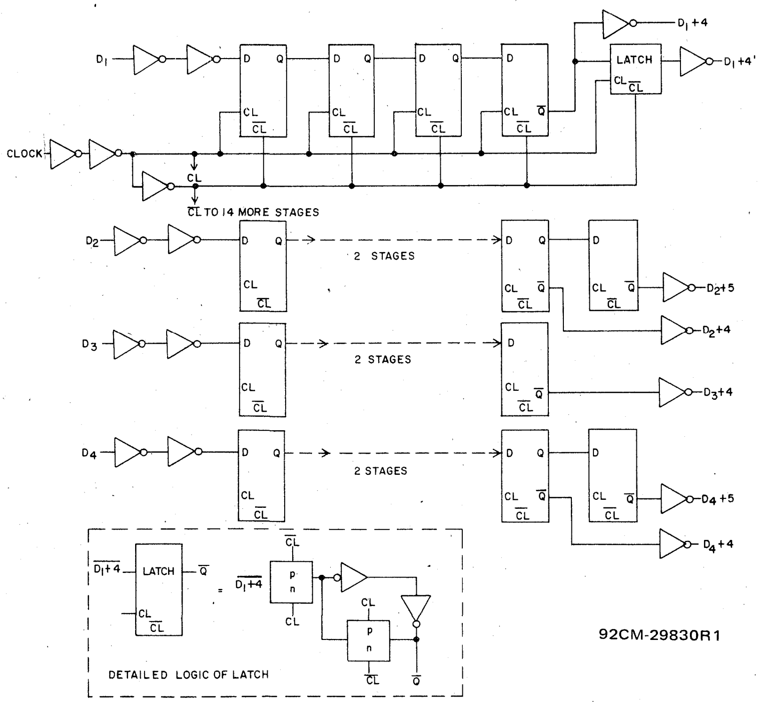


Fig. 6 – Logic diagram with detail of latch.

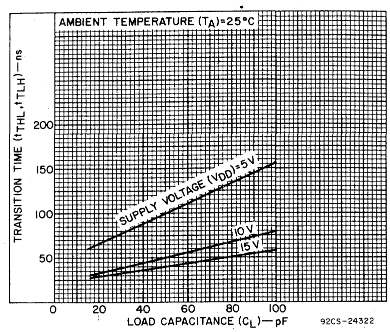


Fig. 7 – Typical transition time as a function of load capacitance.

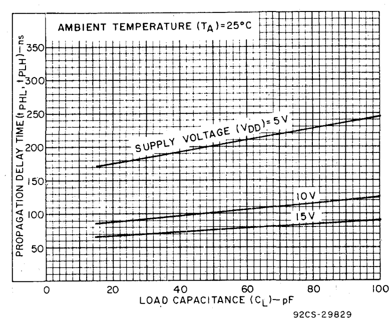


Fig. 8 – Typical propagation delay time as a function of load capacitance.

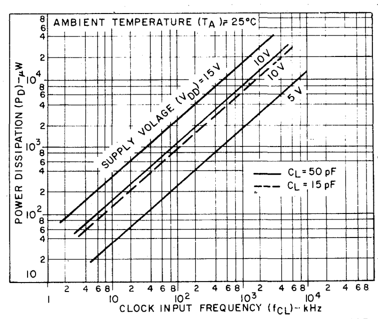


Fig. 9 – Typical dyanamic power dissipation as a function of clock frequency.

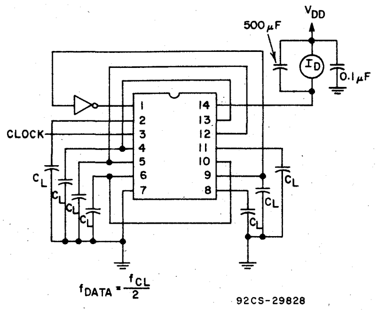


Fig. 10 — Dynamic power dissipation test circuit.

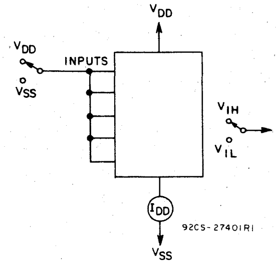


Fig. 11 — Quiescent device current test circuit.

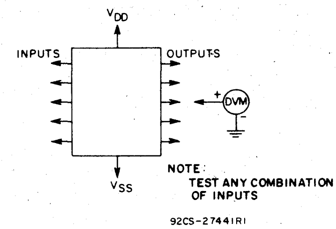


Fig. 12 — Input voltage test circuit.

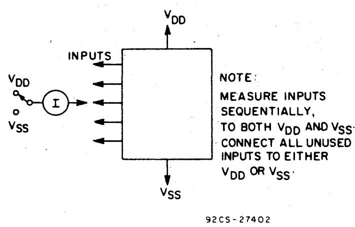
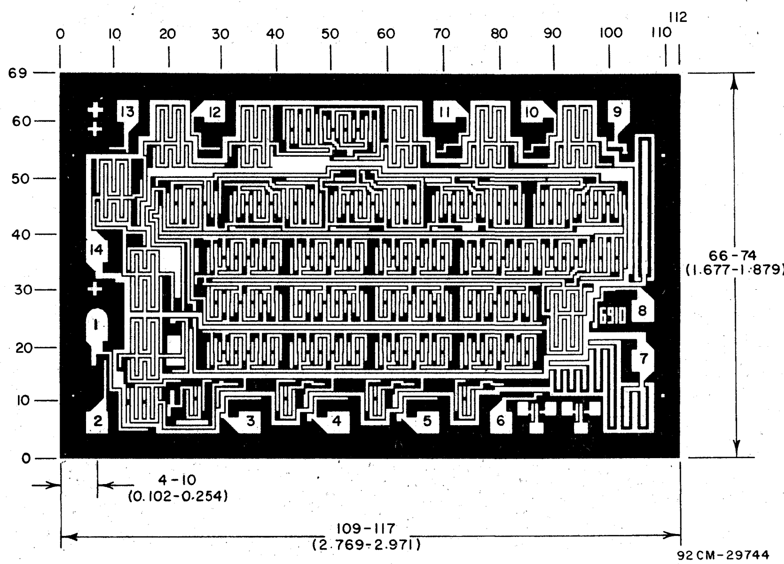


Fig. 13 — Input current test circuit.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for CD4006BH.

CD4007UB Types

COS/MOS Dual Complementary Pair Plus Inverter

High-Voltage Types (20-Volt Rating)

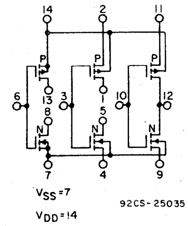
The RCA-CD4007UB types are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in Fig. 2.

More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed.

The CD4007UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Standardized symmetrical output characteristics**
- **Medium Speed Operation – t_{PHL}, t_{PLH} = 30 ns (typ.) at 10 V**
- **100% tested for quiescent current at 20 V**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**



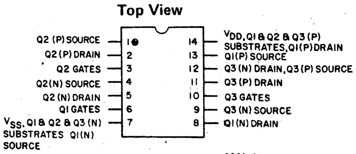
Terminal No.14 – V_{DD}
Terminal No. 7 – V_{SS}

FUNCTIONAL DIAGRAM

Applications:

- **Extremely high-input impedance amplifiers**
- **Shapers**
- **Inverters**
- **Threshold detector**
- **Linear amplifiers**
- **Crystal oscillators**

TERMINAL DIAGRAM
Top View



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages Values at –40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	4.5	–	5	1				–	–	1	V
	9	–	10	2				–	–	2	
	13.5	–	15	2.5				–	–	2.5	
Input High Voltage, V_{IH} Min.	0.5	–	5	4				4	–	–	
	1	–	10	8				8	–	–	
	1.5	–	15	12.5				12.5	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		CONDITIONS	ALL TYPES LIMITS		UNITS
		V_{DD} Volts	Typ.	Max.	
Propagation Delay Time:	t_{PHL}, t_{PLH}	5	55	110	ns
		10	30	60	
		15	25	50	
Transition Time	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance	C_{IN}	Any Input	10	15	pF

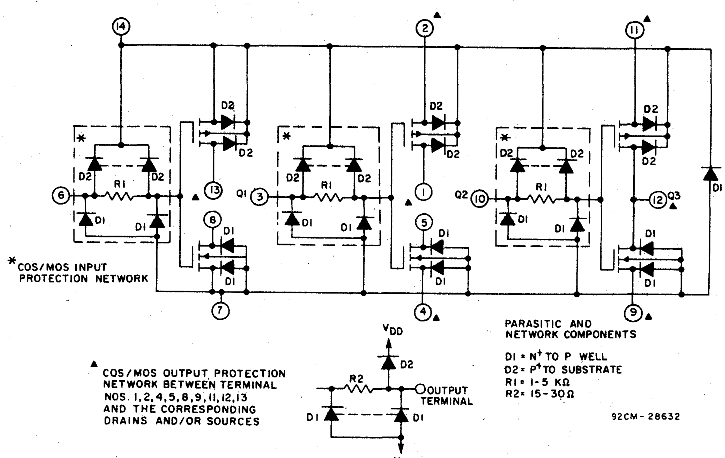
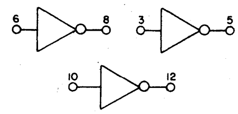


Fig. 1 – Detailed schematic diagram of CD4007UB showing input, output, and parasitic diodes.

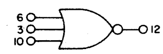
a) Triple Inverters



(14,2,11); (8,13); (1,5); (7,4,9)

92CS-15350

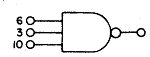
b) 3-Input NOR Gate



(13,2); (1,11); (12,5,8); (7,4,9)

92CS-15349

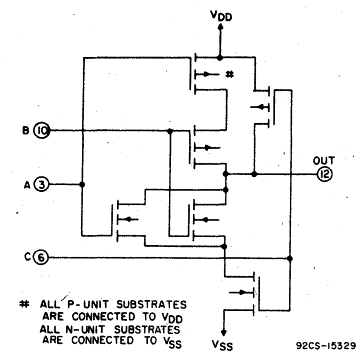
c) 3-Input NAND Gate



(1,12,13); (2,14,11); (4,8); (5,9)

92CS-15348

d) Tree (Relay) Logic



(13,12,5); (4,9,8); (14,2); (1,11)

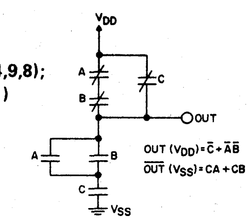
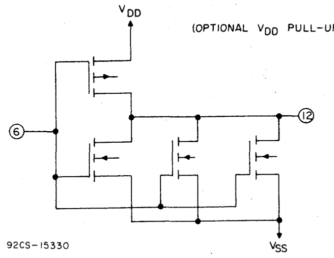


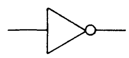
Fig. 2 – Sample COS/MOS logic circuit arrangements using type CD4007UB.

CD4007UB Types

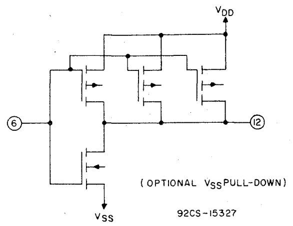
e) High Sink-Current Driver



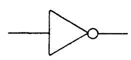
(6,3,10); (8.5, 12);
(11,14); 7,4,9)



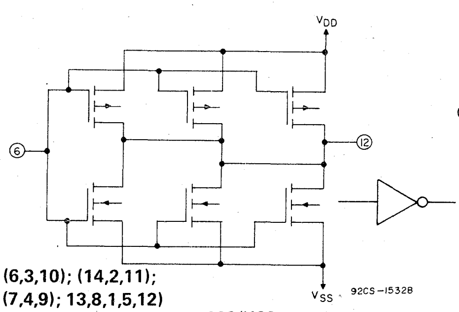
f) High Source-Current Driver



(6,3,10); (13,1,12);
(14,2,11); (7,9)

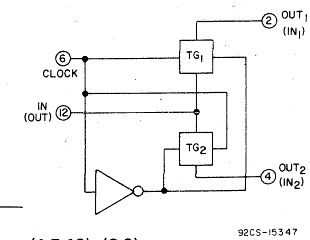


g) High Sink - and Source-Current Driver



(6,3,10); (14,2,11);
(7,4,9); 13,8,1,5,12)

h) Dual Bi-Directional Transmission Gating



(1,5,12); (2,9);
(11,4); (8,13,10);
(6,3)

Fig. 2 – Sample COS/MOS logic circuit arrangements using type CD4007UB (Cont'd).

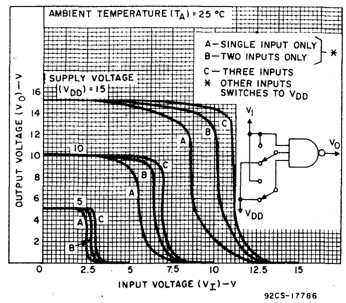


Fig. 3 – Typical voltage-transfer characteristics for NAND gate.

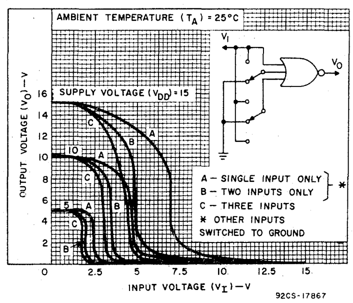


Fig. 4 – Typical voltage-transfer characteristics for NOR gate.

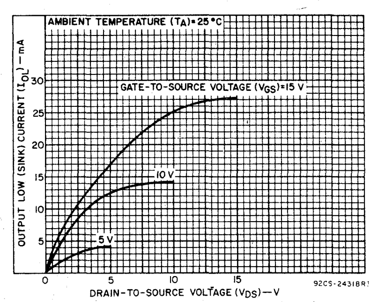


Fig. 5 – Typical output low (sink) current characteristics.

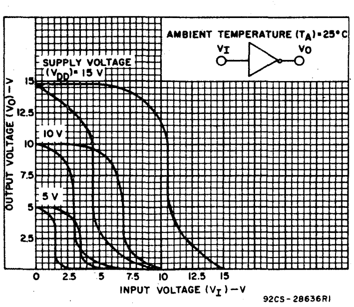


Fig. 6 – Minimum and maximum voltage-transfer characteristics for inverter.

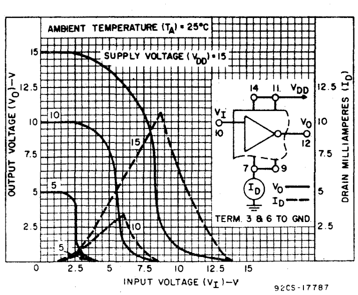


Fig. 7 – Typical current and voltage-transfer characteristics for inverter.

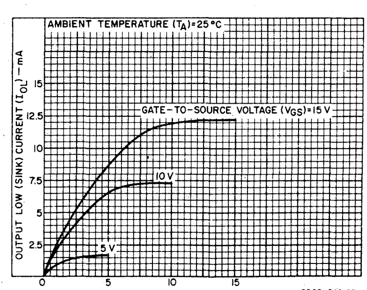


Fig. 8 – Minimum output low (sink) current characteristics.

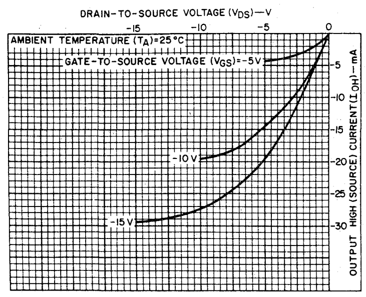


Fig. 9 – Typical output high (source) current characteristics.

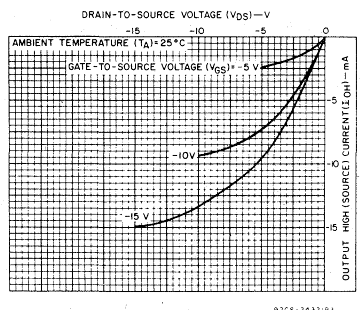


Fig. 10 – Minimum output high (source) current characteristics.

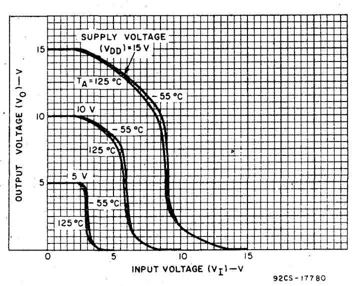


Fig. 11 – Typical voltage-transfer characteristics as a function of temperature.

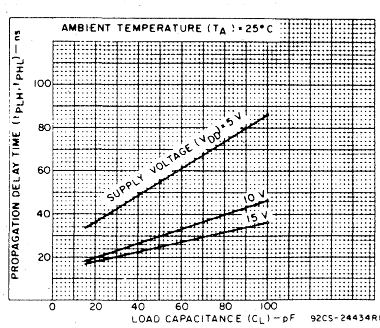


Fig. 12 – Typical propagation delay time vs. load capacitance.

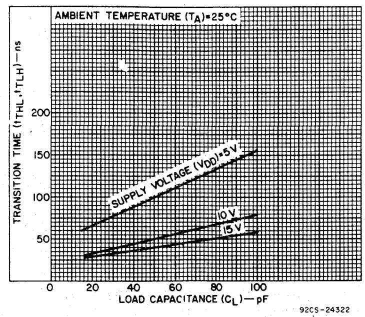


Fig. 13 – Typical transition time vs. load capacitance.

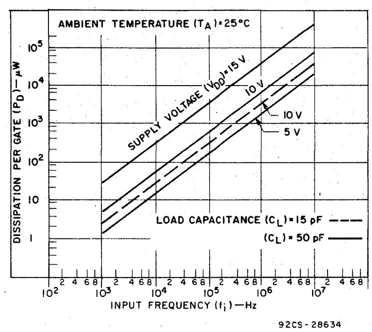


Fig. 14 – Typical dissipation vs. frequency characteristics.

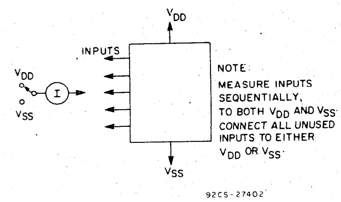


Fig. 15 – Input current test circuit.

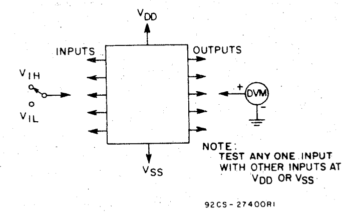


Fig. 16 – Input voltage test circuit.

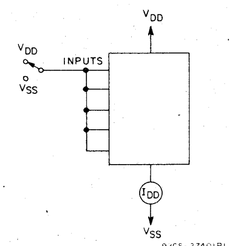
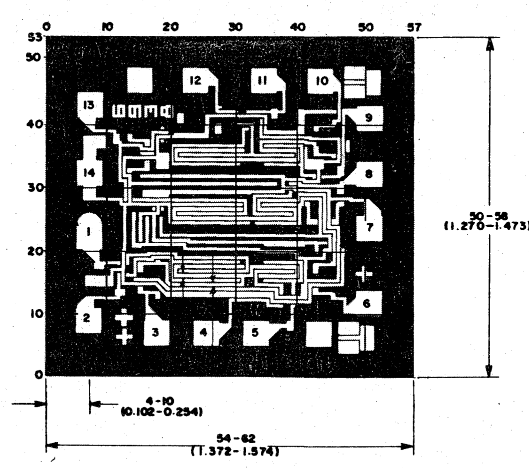


Fig. 17 – Quiescent device current test circuit.



DIMENSIONS AND PAD LAYOUT FOR CD4007UBH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4008B Types

COS/MOS 4-Bit Full Adder

With Parallel Carry Out

High-Voltage Types (20-Volt Rating)

The RCA-CD4008B types consist of four full adder stages with fast look ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" but to permit high-speed operation in arithmetic sections using several CD4008B's.

CD4008B inputs include the four sets of bits to be added, A_1 to A_4 and B_1 to B_4, in addition to the "Carry In" bit from a previous section. CD4008B outputs include the four sum bits, S_1 to S_4. In addition to the high speed "parallel-carry-out" which may be utilized at a succeeding CD4008B section.

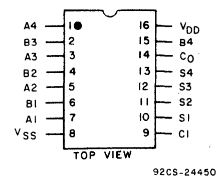
The CD4008B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **4 sum outputs plus parallel look-ahead carry-output**
- **High-speed operation — sum in-to-sum out, 160 ns typ; carry in-to-carry out, 50 ns typ. at V_{DD} = 10 V, C_L = 50 pF**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Binary addition/arithmetic units**



CD4008B
TERMINAL ASSIGNMENT

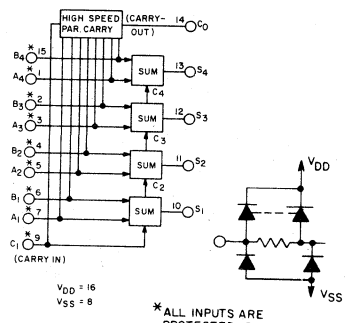


Fig.1 – CD4008B logic diagram.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages; Values at −40, +25, +85 Apply to E Package: −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

TRUTH TABLE

A_i	B_i	C_i	C_O	SUM
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:*

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . . +265°C

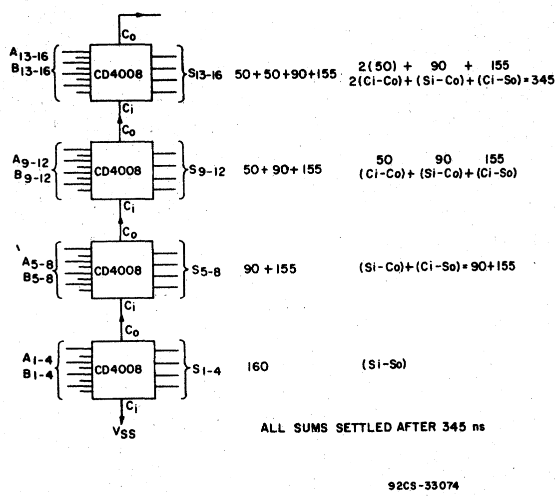


Fig.2 — Typical propagation delay for a 16-bit adder (10 V operation).

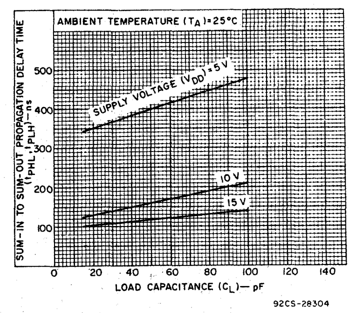


Fig.3 — Typical sum-in to sum-out propagation delay time vs. load capacitance.

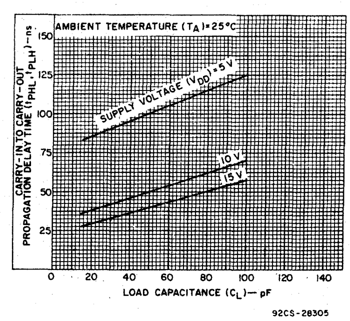


Fig.4 — Typical carry-in to carry-out propagation delay time vs. load capacitance.

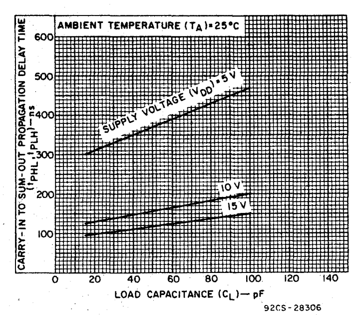


Fig.5 — Typical carry-in to sum-out propagation delay time vs. load capacitance.

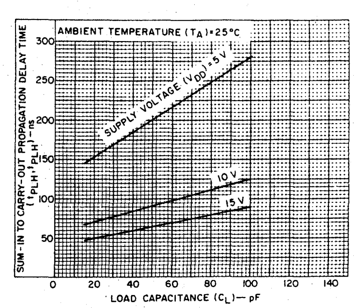


Fig.6 — Typical sum-in to carry-out propagation delay time vs. load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ C$; Input t_r, $t_f = 20\,ns$, $C_L = 50\,pF$, $R_L = 200k\Omega$

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL TYPES TYP.	LIMITS ALL TYPES MAX.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} Sum In to Sum Out	5	400	800	ns
	10	160	320	
	15	115	230	
Carry In to Sum Out	5	370	740	ns
	10	155	310	
	15	115	230	
Sum In to Carry Out	5	200	400	ns
	10	90	180	
	15	65	130	
Carry In to Carry Out	5	100	200	ns
	10	50	100	
	15	40	80	
Transition Time: t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN}	—	5	7.5	pF

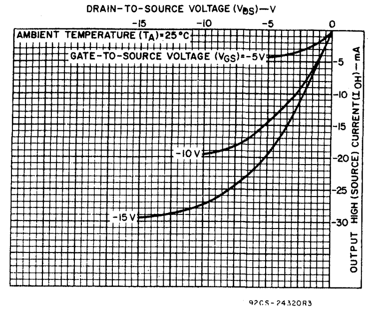


Fig.7 — Typical output high (source) current characteristics.

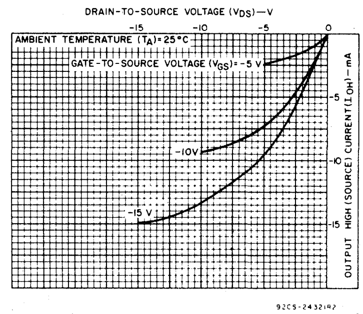


Fig.8 — Minimum output high (source) current characteristics.

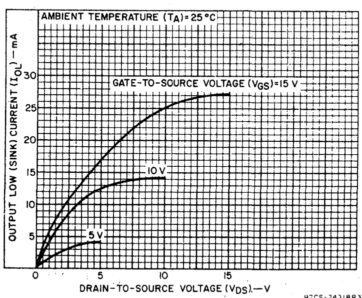


Fig.9 — Typical output low (sink) current characteristics.

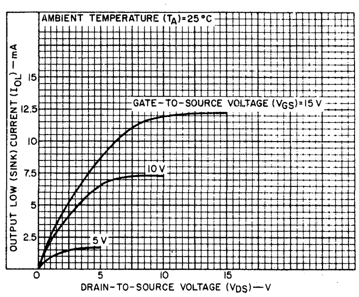


Fig.10 — Minimum output low (sink) current characteristics.

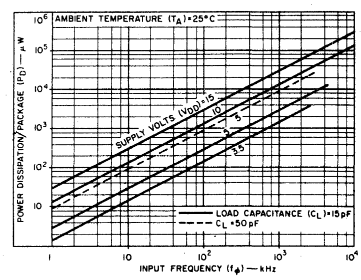


Fig.11 — Typical dissipation characteristics.

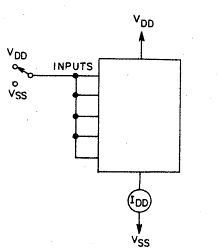


Fig.12 — Quiescent-device-current test circuit.

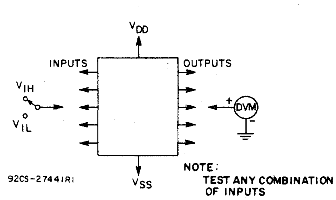


Fig.13 — Input-voltage test circuit.

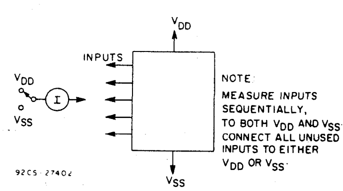
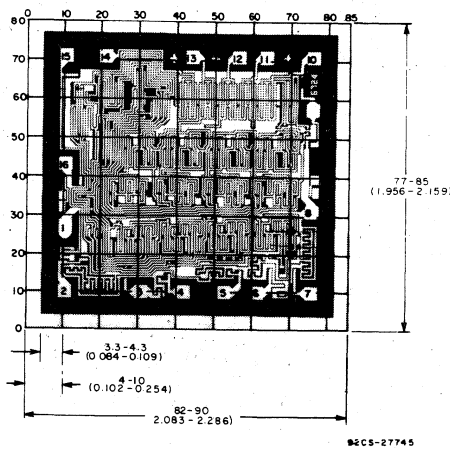


Fig.14 — Input current test circuit.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and Pad Layout for CD4008BH

CD4009UB, CD4010B Types

COS/MOS
Hex Buffers/Converters

High-Voltage Types (20-Volt Rating)

Inverting Type: CD4009UB

Non-Inverting Type: CD4010B

The RCA-CD4009UB and CD4010B Hex Buffer/Converters may be used as COS/MOS to TTL or DTL logic-level converters or COS/MOS high-sink-current drivers.

The CD4049UB and CD4050B are preferred hex buffer replacements for the CD4009UB and CD4010B, respectively, in all applications except multiplexers. For applications not requiring high sink current or voltage conversion, the CD4069UB Hex Inverter is recommended.

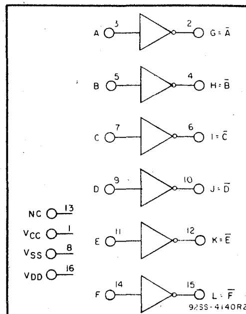
The CD4009UB and CD4010B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

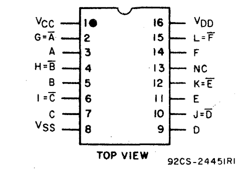
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings

Applications:

- **COS/MOS to DTL/TTL hex converter**
- **COS/MOS current "sink" or "source" driver**
- **COS/MOS high-to-low logic-level converter**
- **Multiplexer – 1 to 6 or 6 to 1**

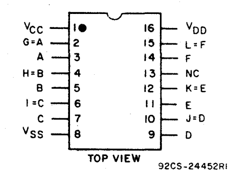


CD4009UB
FUNCTIONAL DIAGRAM



NC = NO CONNECTION

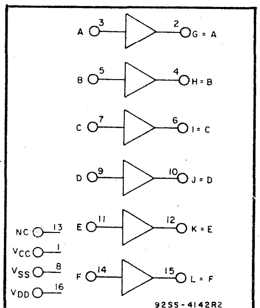
CD4009UB



NC = NO CONNECTION

CD4010B

TERMINAL ASSIGNMENTS



CD4010B
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}, V_{CC}) (Voltages referenced to V_{SS} Terminal)	–0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	–55 to +125°C
PACKAGE TYPE E	–40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	–65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

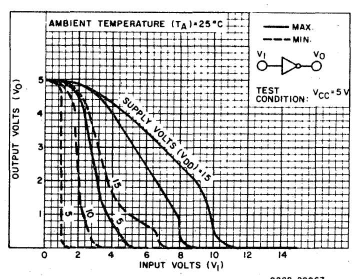


Fig. 3 – Minimum and maximum voltage transfer characteristics–CD4009UB.

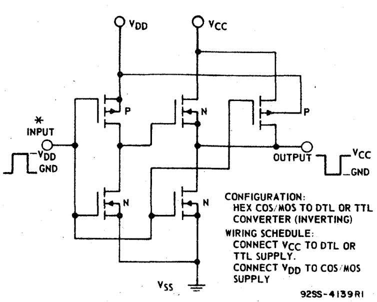


Fig. 1 – Schematic diagram of CD4009UB– 1 of 6 identical stages.

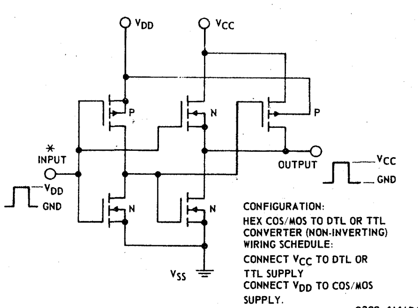
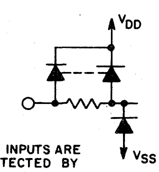


Fig. 2 – Schematic diagram of CD4010B– 1 of 6 identical stages.



*ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range), V_{DD}	3	18	V
V_{CC}*	3	V_{DD}	
Input Voltage Range (V_I)	V_{CC}*	V_{DD}	V

*The CD4009UB and CD4010B have high-to-low level voltage conversion capability but not low-to-high level, therefore it is recommended that $V_{DD} \geq V_I \geq V_{CC}$.

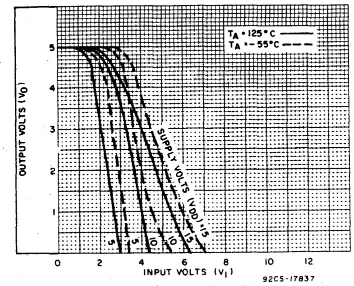


Fig. 4 — Typical voltage transfer characteristics as function of temp.—CD4009UB.

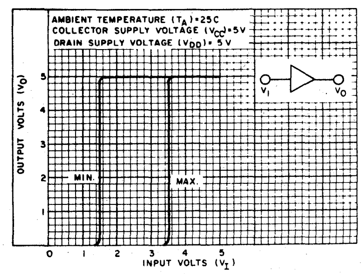


Fig. 5 — Minimum and maximum voltage transfer characteristics (V_{DD}=5)—CD4010B.

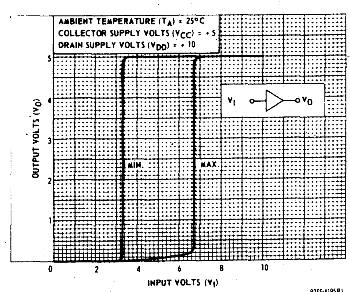


Fig. 6 — Minimum and maximum voltage transfer characteristics (V_{DD}=10)—CD4010B.

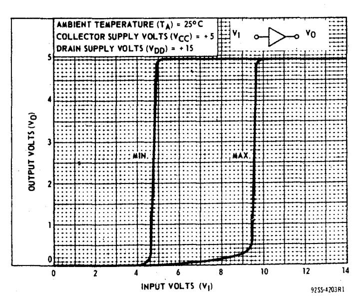


Fig. 7 — Minimum and maximum voltage transfer characteristics (V_{DD}=15)—CD4010B.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			Limits At Indicated Temperatures (°C) *Values at –55,+25,+125 Apply to D,F,H Pkgs. Values at –40,+25,+85 Apply to E Package*							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	3.75	3.6	2.4	2.1	3	4	–	mA
	0.5	0,10	10	10	9.6	6.4	5.6	8	10	–	
	1.5	0,15	15	30	40	19	16	24	36	–	
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	–0.25	–0.23	–0.18	–0.15	–0.2	–0.4	–	
	2.5	0,5	5	–1	–0.9	–0.65	–0.58	–0.8	–1.6	–	
	9.5	0,10	10	–0.55	–0.5	–0.38	–0.33	–0.45	–0.9	–	
	13.5	0,15	15	–1.65	–1.6	–1.25	–1.1	–1.5	–3	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05					0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage: V_{IL} Max. CD4009UB	4.5	–	5	1				–	–	1	V
	9	–	10	2				–	–	2	
	13.5	–	15	2.5				–	–	2.5	
Input Low Voltage: V_{IL} Max. CD4010B	0.5	–	5	1.5				–	–	1.5	
	1	–	10	3				–	–	3	
	1.5	–	15	4				–	–	4	
Input High Voltage: V_{IH} Min. CD4009UB	0.5	–	5	4				4	–	–	
	1	–	10	8				8	–	–	
	1.5	–	15	12.5				12.5	–	–	
Input High Voltage: V_{IH} Min. CD4010B	4.5	–	5	3.5				3.5	–	–	
	9	–	10	7				7	–	–	
	13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A=25°C; Input t_r, t_f=20 ns, C_L=50 pF, R_L=200 KΩ*

CHARACTERISTIC	CONDITIONS V_{DD} (V)	V_I (V)	V_{CC} (V)	LIMITS ALL PKGS TYP.	MAX.	UNIT
Propagation Delay Time: Low-to-High, t_{PLH}	5	5	5	70	140	ns
	10	10	10	40	80	
CD4009UB	10	10	5	35	70	
	15	15	15	30	60	
	15	15	5	30	60	
	5	5	5	100	200	ns
	10	10	10	50	100	
CD4010B	10	10	5	50	100	
	15	15	15	35	70	
	15	15	5	35	70	
High-to-Low, t_{PHL}	5	5	5	30	60	ns
	10	10	10	20	40	
CD4009UB	10	10	5	15	30	
	15	15	15	15	30	
	15	15	5	10	20	
	5	5	5	65	130	ns
	10	10	10	35	70	
CD4010B	10	10	5	30	70	
	15	15	15	25	50	
	15	15	5	20	40	
Transition Time: Low-to-High, t_{TLH}	5	5	5	150	350	ns
	10	10	10	75	150	
	15	15	15	55	110	
High-to-Low, t_{THL}	5	5	5	35	70	ns
	10	10	10	20	40	
	15	15	15	15	30	
Input Capacitance, C_{IN} CD4009UB	–	–	–	15	22.5	pF
CD4010B	–	–	–	5	7.5	

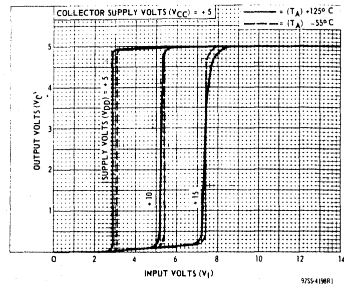


Fig. 8 — Typical voltage transfer characteristics as a function of temperature—CD4010B.

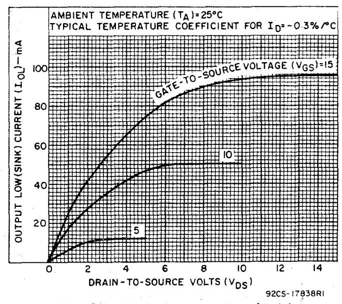


Fig. 9 — Typical output low (sink) current characteristics.

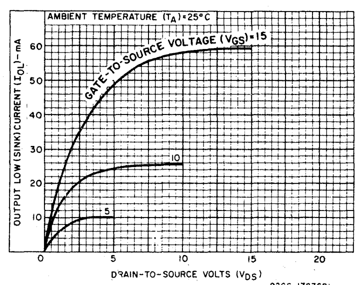


Fig. 10 — Minimum output low (sink) current characteristics.

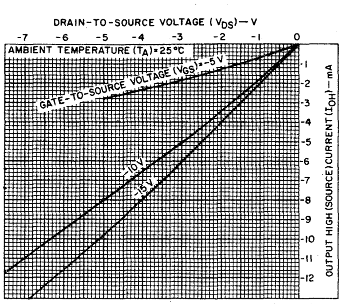


Fig. 11 — Typical output high (source) current characteristics.

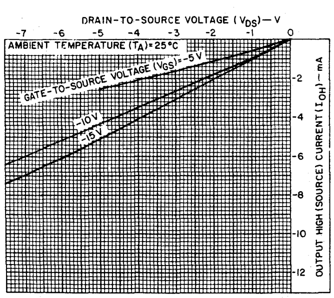


Fig. 12 — Minimum output high (source) current characteristics.

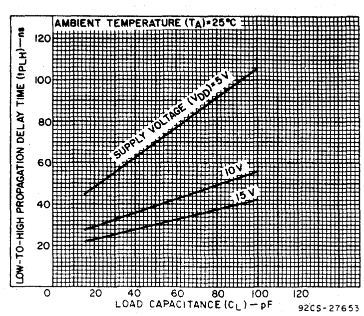


Fig. 13 — Typical low-to-high propagation delay time vs. load capacitance (CD4009UB).

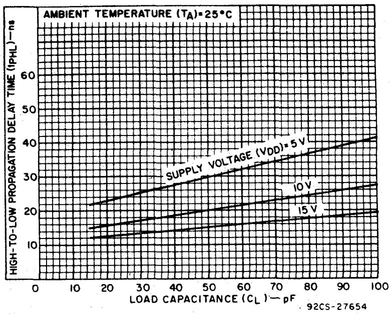


Fig. 14 – Typical high-to-low propagation delay time vs. load capacitance (CD4009UB).

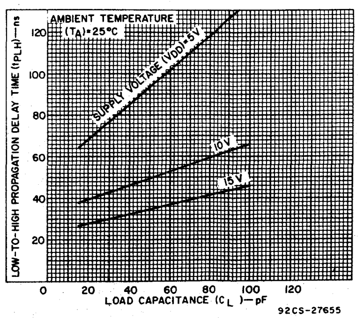


Fig. 15 – Typical low-to-high propagation delay time vs. load capacitance (CD4010B).

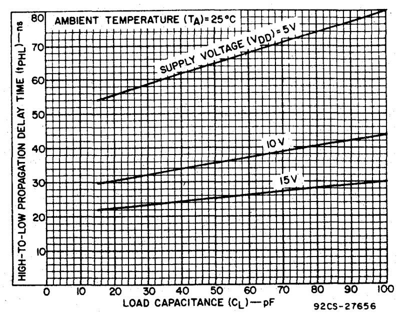


Fig. 16 – Typical high-to-low propagation delay time vs. load capacitance (CD4010B).

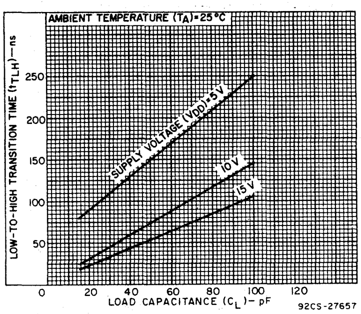


Fig. 17 – Typical low-to-high transition time vs. load capacitance.

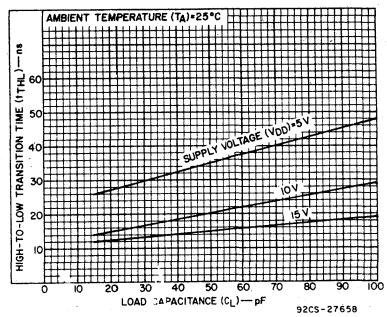


Fig. 18 – Typical high-to-low transition time vs. load capacitance.

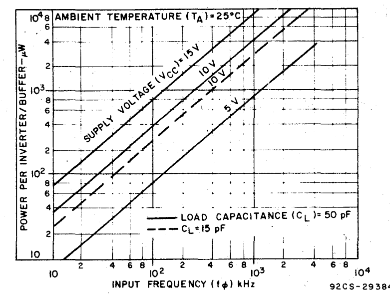


Fig. 19 – Typical dissipation characteristics.

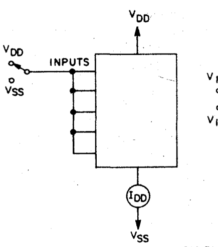


Fig. 20 – Quiescent device current test circuit.

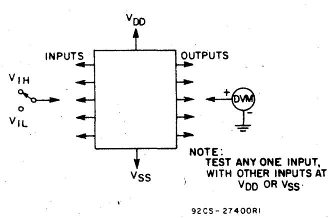


Fig. 21 – Noise immunity test circuit.

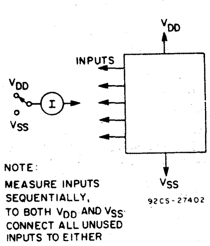
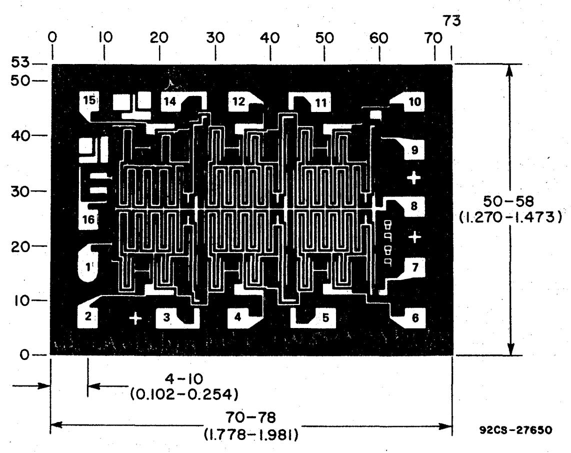


Fig. 22 – Input current test circuit.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid Graduations Are In Mils (10^{-3} Inch)

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Photograph of chip for CD4009UB. Dimensions and pad layout for CD4010B are identical.

CD4011B, CD4012B, CD4023B Types

COS/MOS NAND Gates

High-Voltage Types (20-Volt Rating)

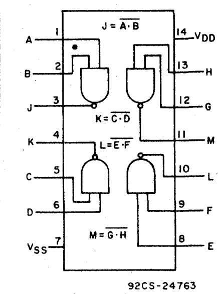
Quad 2 Input – CD4011B
Dual 4 Input – CD4012B
Triple 3 Input – CD4023B

RCA-CD4011B, CD4012B, and CD4023B NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of COS/MOS gates. All inputs and outputs are buffered.

The CD4011B, CD4012B, and CD4023B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

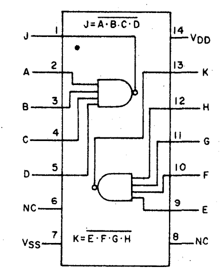
- **Propagation delay time = 60 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V**
- **Buffered inputs and outputs**
- **Standardized symmetrical output characteristics**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Noise margin (over full package temperature range:**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of "B" Series CMOS Devices"**



CD4011B
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

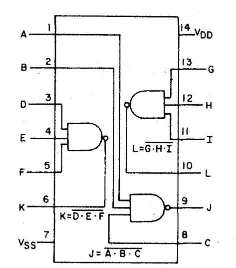


CD4012B
FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

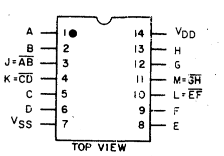
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

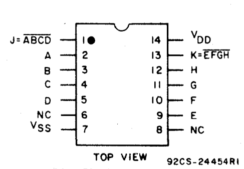


CD4023B
FUNCTIONAL DIAGRAM

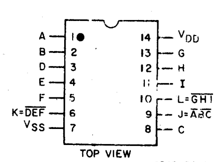
TERMINAL ASSIGNMENTS



CD4011B



CD4012B



CD4023B

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages Values at –40, +25, +85 Apply to E Package –55	–40	+85	+125	+25 Min.	Typ.	Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	4.5	–	5	1.5				–	–	1.5	V
	9	–	10	3				–	–	3	
	13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	'–	$\pm10^{-5}$	±0.1	μA

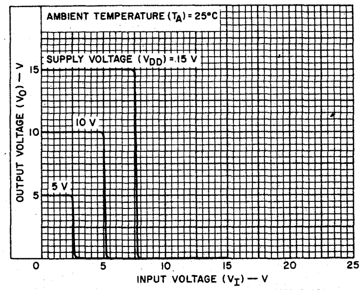


Fig.1 — Typical voltage transfer characteristics.

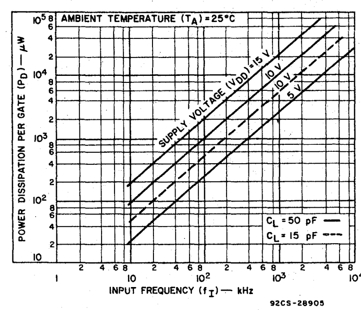


Fig.2 — Typical power dissipation characteristics.

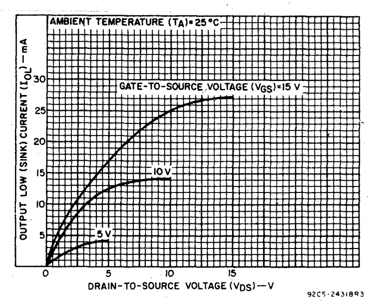


Fig.3 — Typical output low (sink) current characteristics.

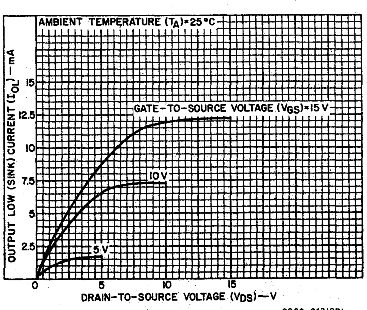


Fig.4 — Minimum output low (sink) current characteristics.

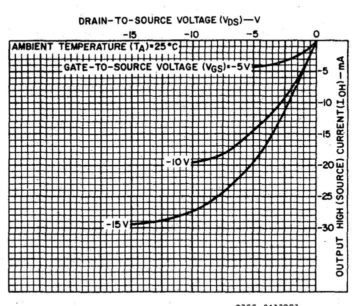


Fig.5 — Typical output high (source) current characteristics.

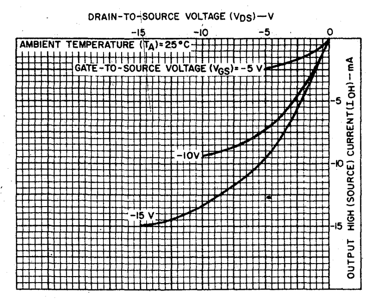


Fig.6 — Minimum output high (source) current characteristics.

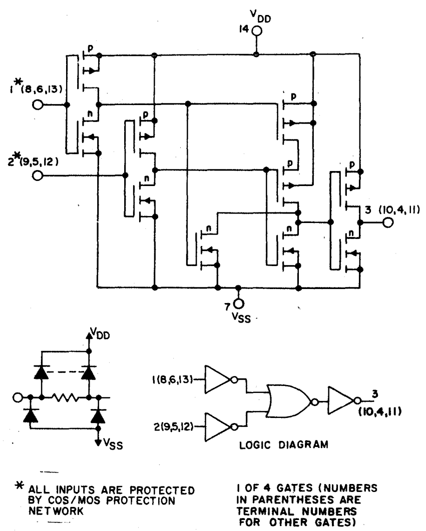


Fig.7 – Schematic and logic diagrams for CD4011B.

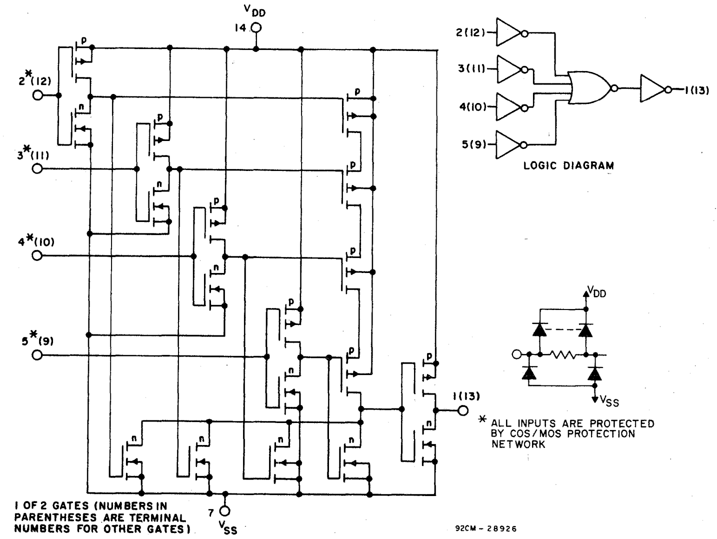


Fig.8 – Schematic and logic diagrams for CD4012B.

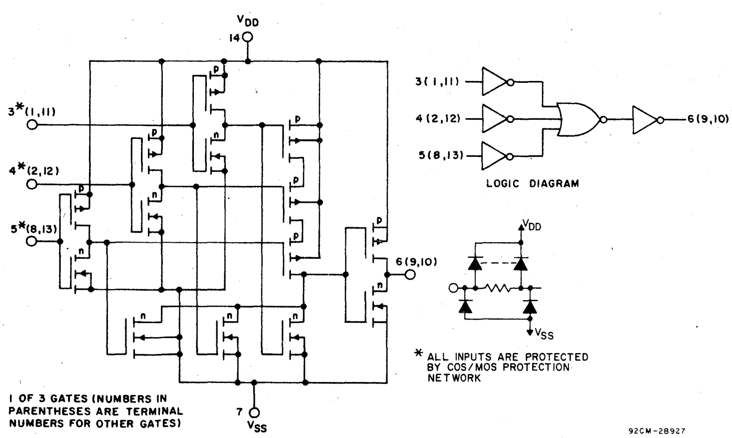


Fig. 9 – Schematic and logic diagrams for CD4023B.

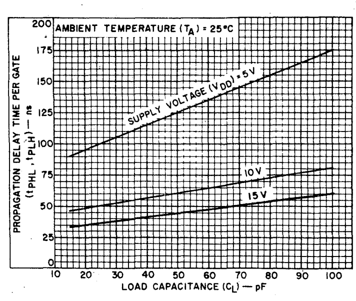


Fig.10 – Typical propagation delay time per gate as a function of load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$; Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200k\Omega$

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5 10 15	125 60 45	250 120 90	ns
Transition Time, t_{THL}, t_{TLH}		5 10 15	100 50 40	200 100 80	ns
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

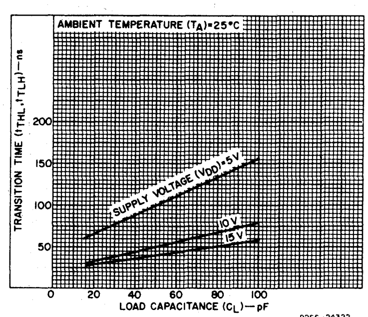


Fig.11 – Typical transition time as a function of load capacitance.

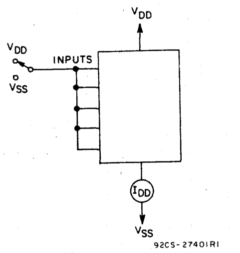


Fig. 12 – Quiescent-device-current test circuit.

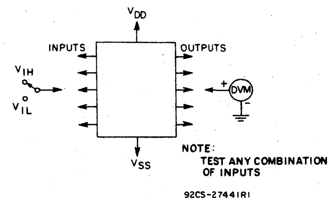


Fig. 13 – Input-voltage test circuit.

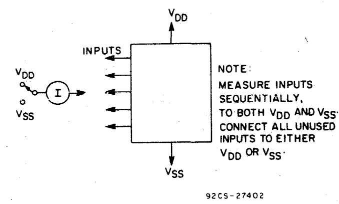
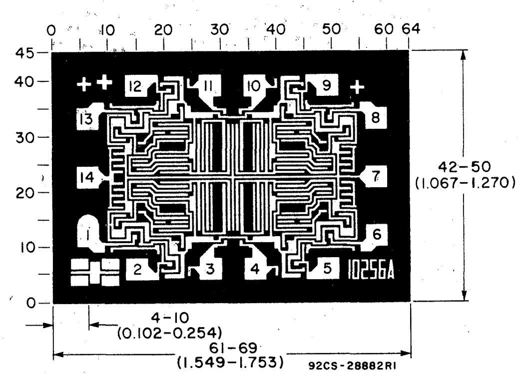
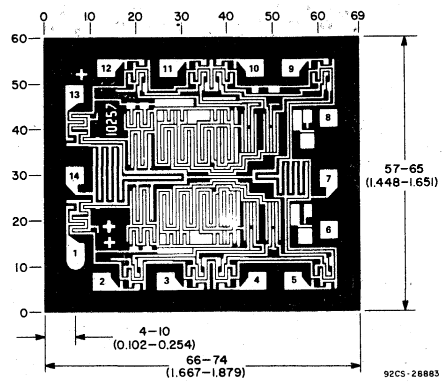


Fig. 14 – Input-current test circuit.

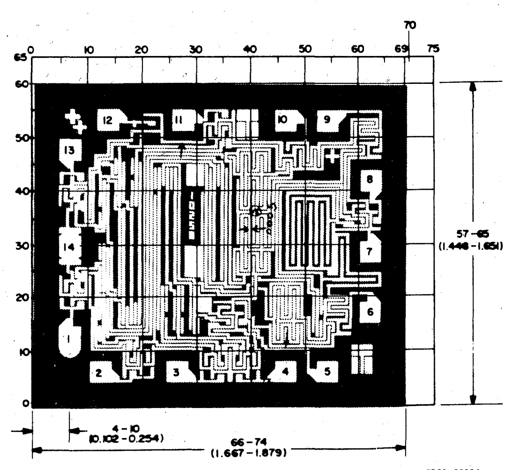
CHIP PHOTOGRAPHS
Dimensions and Pad Layouts



CD4011BH



CD4012BH



CD4023BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

CD4011UB, CD4012UB, CD4023UB Types

COS/MOS NAND Gates

High-Voltage Types (20-Volt Rating)

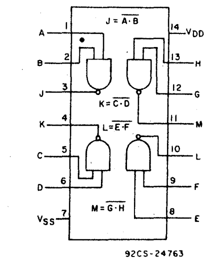
Quad 2 Input – CD4011UB
Dual 4 Input – CD4012UB
Triple 3 Input – CD4023UB

The RCA-CD4011UB, CD4012UB, and CD4023UB NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of COS/MOS gates.

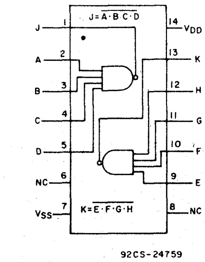
The CD4011UB, CD4012UB, and CD4023UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

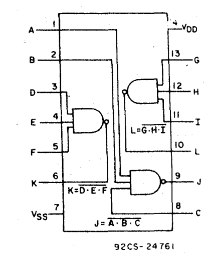
- **Propagation delay time = 30 ns (typ). at C_L = 50 pF, V_{DD} = 10 V**
- **Standardized symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



CD4011UB
FUNCTIONAL DIAGRAM



CD4012UB
FUNCTIONAL DIAGRAM



CD4023UB
FUNCTIONAL DIAGRAM

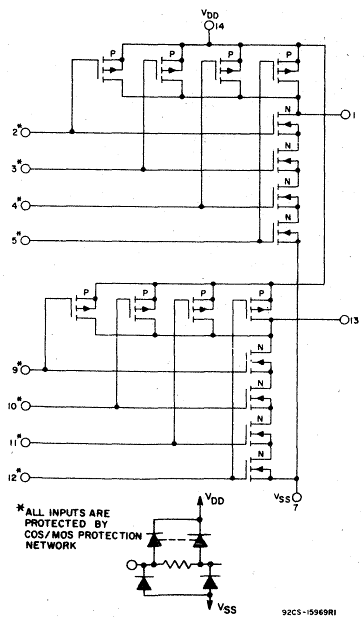


Fig. 1 – Schematic diagram for type CD4012UB.

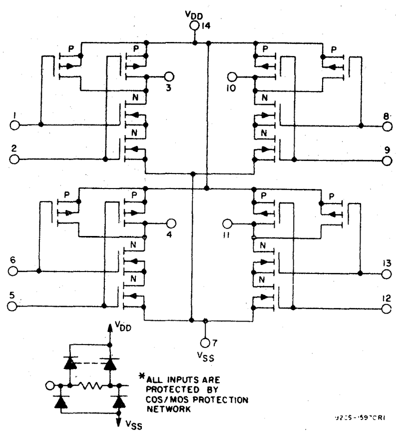


Fig. 2 – Schematic diagram for type CD4011UB.

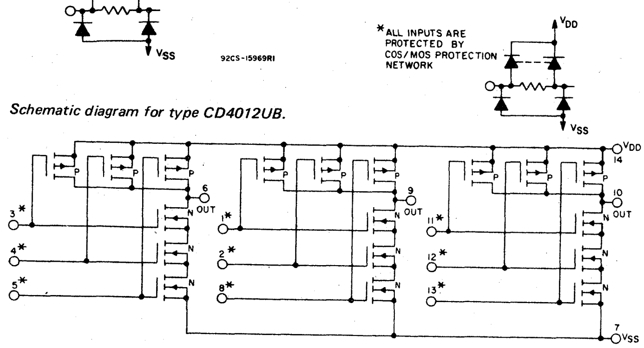


Fig. 3 – Schematic diagram for type CD4023UB. 92CS-17185R1

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	MIN.	MAX.	UNITS
Supply Voltage Range (For T_A= Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . –55 to +125°C
PACKAGE TYPE E . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

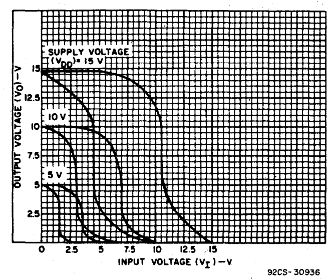


Fig. 4 — Minimum and maximum voltage transfer characteristics.

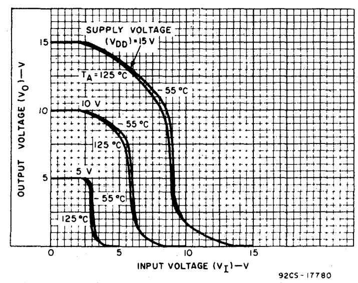


Fig. 5 — Typical voltage transfer characteristics as a function of temperature.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages Values at –40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	µA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	4.5	–	5	1				–	–	1	V
	9	–	10	2				–	–	2	
	13.5	–	15	2.5				–	–	2.5	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	4				4	–	–	
	1,9	–	10	8				8	–	–	
	1.5,13.5	–	15	12.5				12.5	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	µA

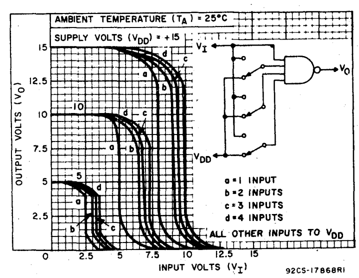


Fig. 6 — Typical multiple input switching transfer characteristics for CD4012UB.

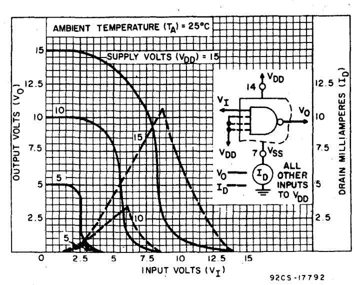


Fig. 7 — Typical current and voltage transfer characteristics.

CD4011UB, CD4012UB, CD4023UB Types

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^{\circ}C$, Input t_r, $t_f = 20$ ns, and $C_L = 50$ pF, $R_L = 200k\,\Omega$

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} VOLTS	TYP.	MAX	
Propagation Delay Time, t_{PHL}, t_{PLH}		5 10 15	60 30 25	120 60 50	ns
Transition Time, t_{THL}, t_{TLH}		5 10 15	100 50 40	200 100 80	ns
Input Capacitance, C_{IN}	Any Input		10	15	pF

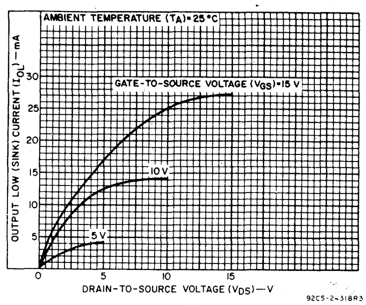


Fig.8 – Typical output low (sink) current characteristics.

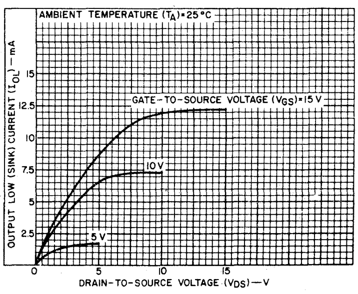


Fig. 9 – Minimum output low (sink) current characteristics.

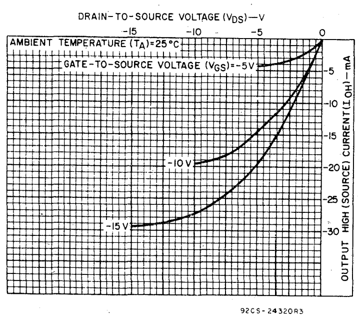


Fig. 10 – Typical output high (source) current characteristics.

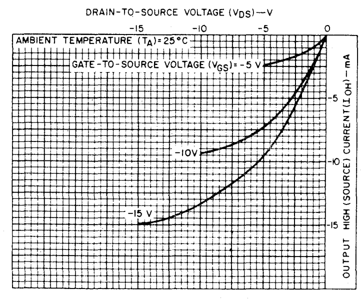


Fig. 11 – Minimum output high (source) current characteristics.

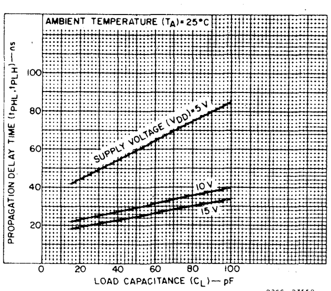


Fig.12 – Typical propagation delay time vs. load capacitance.

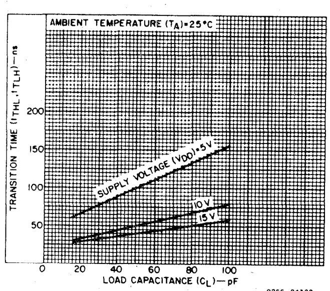


Fig.13 – Typical transition time vs. load capacitance.

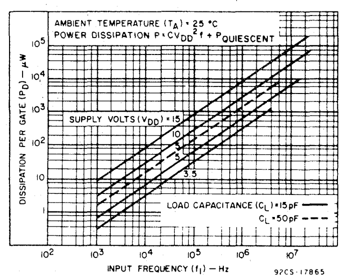


Fig.14 – Typical power dissipation vs. frequency characteristics.

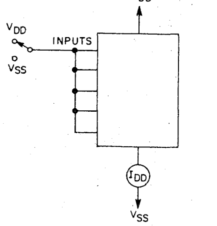


Fig.15 – Quiescent device current test circuit.

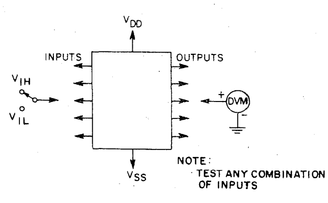


Fig.16 – Input voltage test circuit.

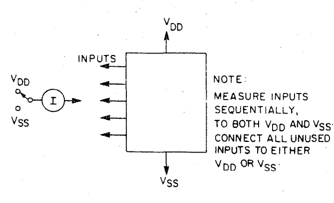
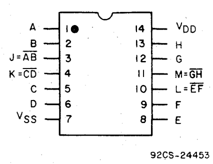


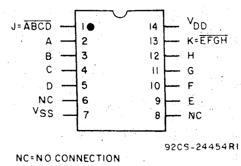
Fig.17 – Input current test circuit.

TERMINAL ASSIGNMENTS



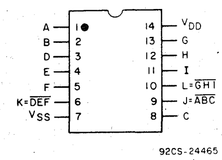
TOP VIEW

CD4011UB



TOP VIEW

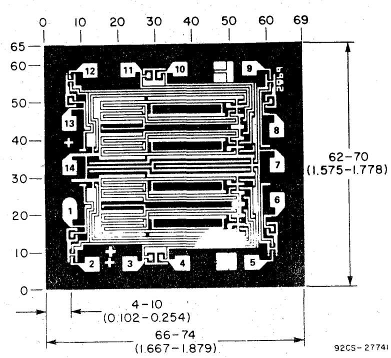
CD4012UB



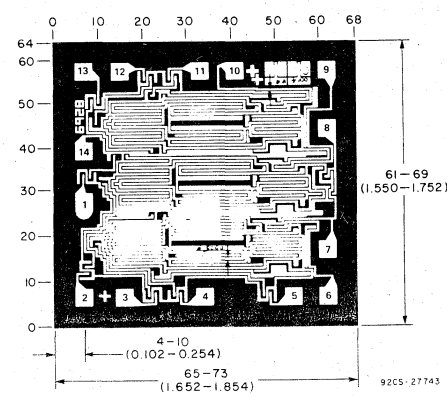
TOP VIEW

CD4023UB

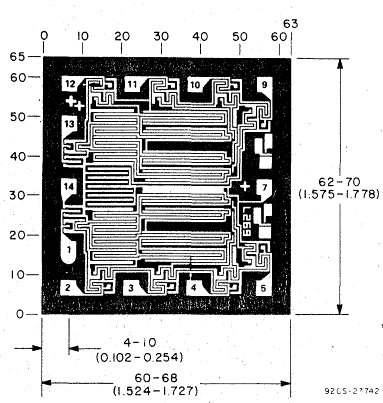
CHIP PHOTOGRAPHS
Dimensions and Pad Layouts



CD4011UBH



CD4023UBH



CD4012UBH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Dual 'D'-Type Flip-Flop

High-Voltage Types (20-Volt Rating)

The RCA-CD4013B consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

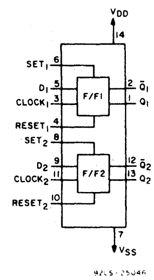
The CD4013B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Set-Reset capability**
- **Static flip-flop operation — retains state indefinitely with clock level either "high" or "low"**
- **Medium-speed operation — 16 MHz (typ.) clock toggle rate at 10V**
- **Standardized symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package temperature range): 1 V at V_{DD}=5 V, 2 V at V_{DD}=10 V, 2.5 V at V_{DD}=15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Registers, counters, control circuits**



CD4013B
FUNCTIONAL DIAGRAM

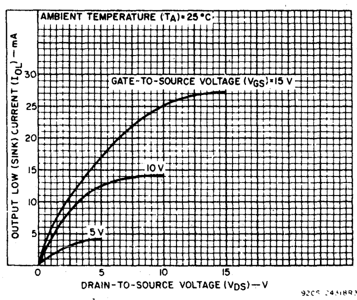


Fig. 1 — Typical output low (sink) current characteristics.

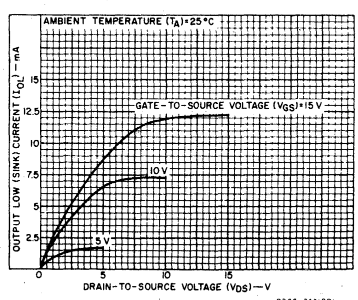


Fig. 2 — Minimum output low (sink) current characteristics.

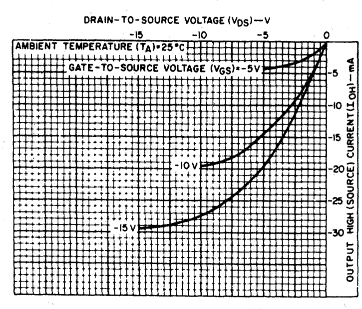


Fig. 3 — Typical output high (source) current characteristics.

RECOMMENDED OPERATING CONDITIONS

At T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	—	3	18	V
Data Setup Time t_S	5	40	—	ns
	10	20	—	
	15	15	—	
Clock Pulse Width t_W	5	140	—	ns
	10	60	—	
	15	40	—	
Clock Input Frequency f_{CL}	5	dc	3.5	MHz
	10		8	
	15		12	
Clock Rise or Fall Time t_rCL,* t_fCL	5	—	15	μs
	10	—	4	
	15	—	1	
Set or Reset Pulse Width t_W	5	180	—	ns
	10	80	—	
	15	50	—	

*If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

STATIC ELECTRICAL CHARACTERISTICS

CHARAC-TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Pkgs. Values at −40,+25,+85 Apply to E Pkgs.							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	Typ.	Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

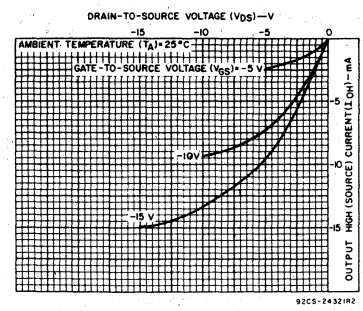


Fig. 4 — Minimum output high (source) current characteristics.

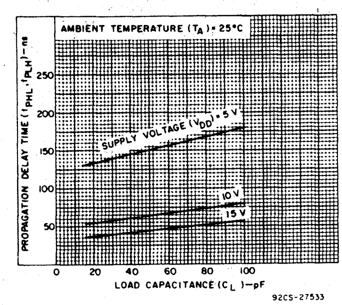


Fig. 5 — Typical propagation delay time vs. load capacitance (CLOCK or SET to Q,CLOCK or RESET to $\overline{Q}$).

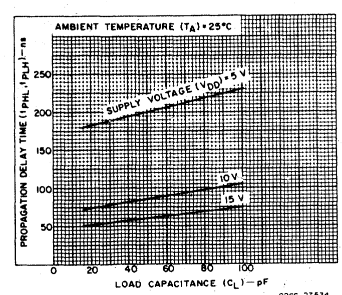


Fig. 6 — Typical propagation delay time vs. load capacitance (SET to $\overline{Q}$ or RESET to Q).

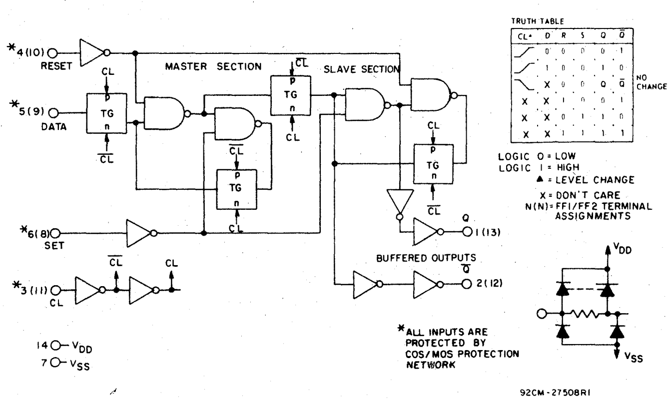


Fig. 7 — Logic diagram and truth table for CD4013B (one of two identical flip-flops).

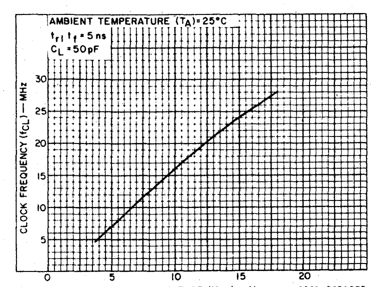


Fig. 8 — Typical maximum clock frequency vs. supply voltage.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Propagation Delay Time: Clock to Q or $\overline{Q}$ Outputs t_{PHL}, t_{PLH}		5	–	150	300	ns
		10	–	65	130	
		15	–	45	90	
Set to Q or Reset to $\overline{Q}$ t_{PLH}		5	–	150	300	ns
		10	–	65	130	
		15	–	45	90	
Set to $\overline{Q}$ or Reset to Q t_{PHL}		5	–	200	400	ns
		10	–	85	170	
		15	–	60	120	
Transition Time t_{THL}, t_{TLH}		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Maximum Clock Input Frequency Frequency # f_{CL}		5	3.5	7	–	MHz
		10	8	16	–	
		15	12	24	–	
Minimum Clock Pulse Width t_W		5	–	70	140	ns
		10	–	30	60	
		15	–	20	40	
Minimum Set or Reset Pulse Width t_W		5	–	90	180	ns
		10	–	40	80	
		15	–	25	50	
Minimum Data Setup Time t_S		5	–	20	40	ns
		10	–	10	20	
		15	–	7	15	
Clock Input Rise or Fall Time t_{rCL}, t_{fCL}		5	–	–	15	µs
		10	–	–	4	
		15	–	–	1	
Input Capacitance C_{IN}	Any Input		–	5	7.5	pF

#Input t_r, t_f = 5 ns.

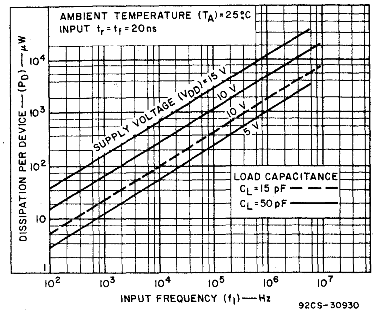


Fig. 9 — Typical power dissipation vs. frequency.

TEST CIRCUITS

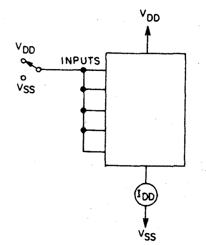


Fig. 10 — Quiescent device current.

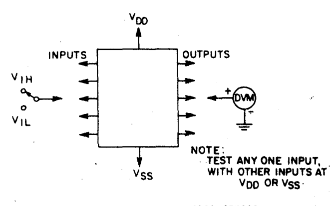


Fig. 11 — Input voltage.

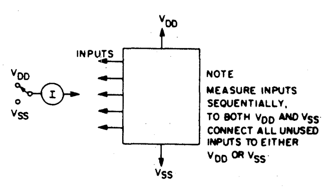
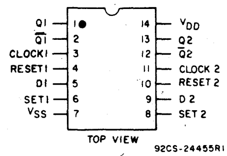
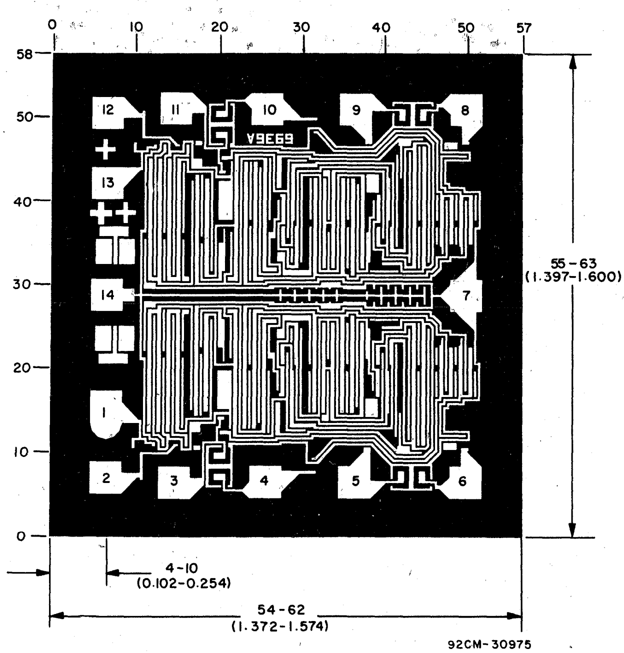


Fig. 12 — Input current.



TERMINAL ASSIGNMENT

DIMENSIONS AND PAD LAYOUT FOR CD4013BH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4014B, CD4021B Types

COS/MOS 8-Stage Static Shift Registers

High-Voltage Types (20-Volt Rating)

CD4014B:

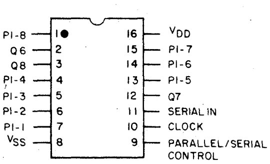
Synchronous Parallel or Serial Input/Serial Output

CD4021B:

Asynchronous Parallel Input or Synchronous Serial Input/Serial Output

The RCA-CD4014B and CD4021B series types are 8-stage parallel- or serial-input/serial output registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL data input, and individual parallel "JAM" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7. Parallel as well as serial entry is made into the register synchronously with the positive clock line transition in the CD4014B. In the CD4021B serial entry is synchronous with the clock but parallel entry is asynchronous. In both types, entry is controlled by the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. In the CD4021B, the CLOCK input of the internal stage is "forced" when asynchronous parallel entry is made. Register expansion using multiple packages is permitted.

The CD4014B and CD4021B series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

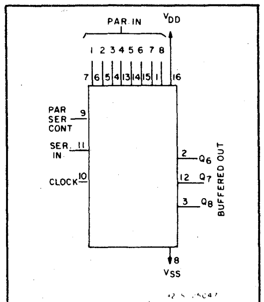


TOP VIEW 92CS-24456

TERMINAL DIAGRAM CD4014B, CD4021B

Features:

- **Medium-speed operation . . . 12 MHz (typ.) clock rate at $V_{DD}-V_{SS}$ = 10 V**
- **Fully static operation**
- **8 master-slave flip-flops plus output buffering and control gating**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) = 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V**
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



CD4014B, CD4021B FUNCTIONAL DIAGRAM

Applications:

- **Parallel input/serial output data queueing**
- **Parallel to serial data conversion**
- **General-purpose register**

RECOMMENDED OPERATING CONDITIONS AT T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (T_A = Full Package-Temperature Range)	–	3	18	V
Clock Pulse Width, t_W	5	180	–	ns
	10	80	–	
	15	50	–	
Clock Frequency, f_{CL}	5	–	3	MHz
	10	–	6	
	15	–	8.5	
Clock Rise and Fall Time, t_rCL, t_fCL	5	–	15	μs
	10	–	15	
	15	–	15	
Set-up Time, t_s: Serial Input (ref. to CL)	5	120	–	ns
	10	80	–	
	15	60	–	
Parallel Inputs CD4014B (ref. to CL)	5	80	–	ns
	10	50	–	
	15	40	–	
Parallel Inputs CD4021B (ref. to P/S)	5	50	–	ns
	10	30	–	
	15	20	–	
Parallel/Serial Control CD4014B (ref. to CL)	5	180	–	ns
	10	80	–	
	15	60	–	
Parallel/Serial Pulse Width, t_W (CD4021B)	5	160	–	ns
	10	80	–	
	15	50	–	
Parallel/Serial Removal Time, t_{REM} (CD4021B)	5	280	–	ns
	10	140	–	
	15	100	–	

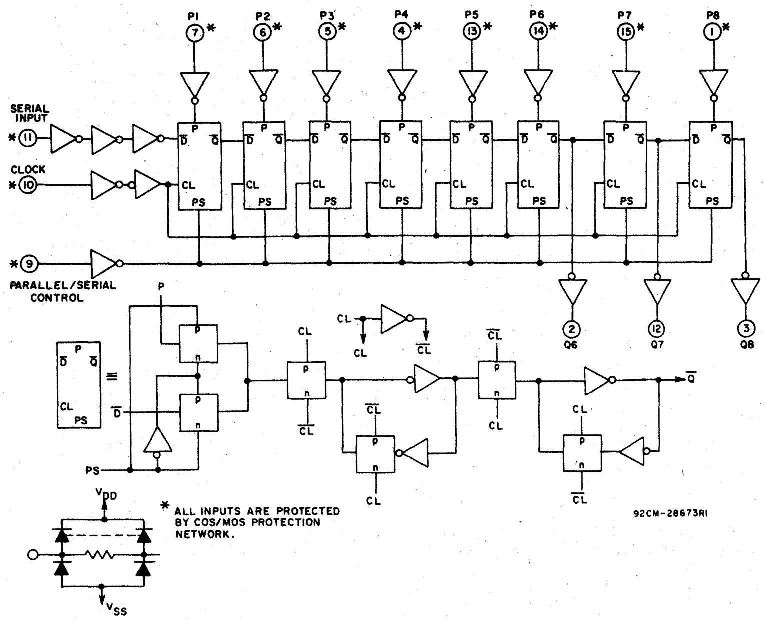


Fig. 1 – Logic diagram for CD4014B.

TRUTH TABLE – CD4014B

CL	SER. IN	PAR SER CONTROL	PI-1	PI-n	Q_1 (INTERNAL)	Q_n	
_/‾	X	1	0	0	0	0	
_/‾	X	1	1	0	1	0	
_/‾	X	1	0	1	0	1	
_/‾	X	1	1	1	1	1	
_/‾	0	0	X	X	0	Q_{n-1}	
_/‾	1	0	X	X	1	Q_{n-1}	
‾_	X	X	X	X	Q_1	Q_n	NC

X = DON'T CARE CASE
NC = NO CHANGE

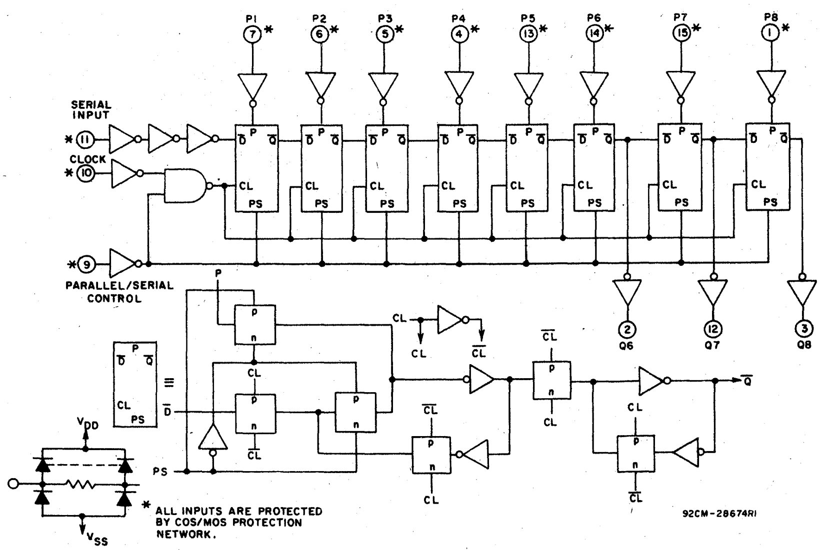


Fig. 2 – Logic diagram for CD4021B.

TRUTH TABLE – CD4021B

CL	Serial Input	Parallel/ Serial Control	PI-1	PI-n	Q_1 (Internal)	Q_n	
X	X	1	0	0	0	0	
X	X	1	0	1	0	1	
X	X	1	1	0	1	0	
X	X	1	1	1	1	1	
_/‾	0	0	X	X	0	Q_{n-1}	
_/‾	1	0	X	X	1	Q_{n-1}	
‾_	X	0	X	X	Q_1	Q_n	NC

X = DON'T CARE CASE

CD4014B, CD4021B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

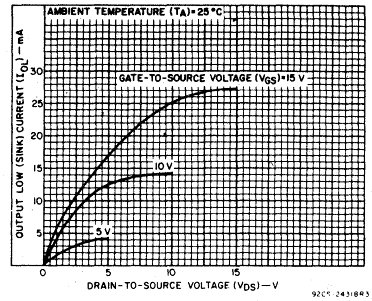


Fig. 3 — Typical output low (sink) current characteristics.

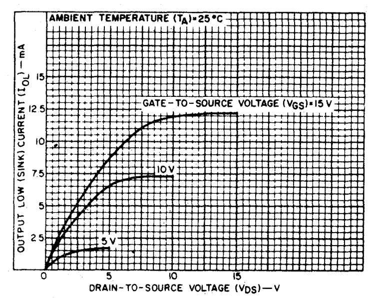


Fig. 4 — Minimum output low (sink) current characteristics.

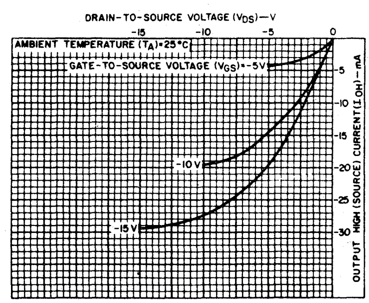


Fig. 5 — Typical output high (source) current characteristics.

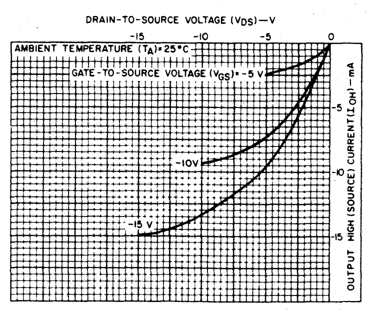


Fig. 6 — Minimum output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARAC-TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	µA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	µA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, Input t_r,t_f=20 ns, C_L=50 pF, R_L=200 KΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time, t_{PLH}, t_{PHL}	5	–	160	320	ns
	10	–	80	160	
	15	–	60	120	
Transition Time, t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Maximum Clock Input Frequency, f_{CL}	5	3	6	–	MHz
	10	6	12	–	
	15	8.5	17	–	
Minimum Clock Pulse Width, t_W	5	–	90	180	ns
	10	–	40	80	
	15	–	25	50	
Clock Rise and Fall Time, t_rCL, t_fCL*	5	–	–	15	µs
	10	–	–	15	
	15	–	–	15	
Minimum Set-up Time, t_s: Serial Input (ref. to CL)	5	–	60	120	ns
	10	–	40	80	
	15	–	30	60	
Parallel Inputs CD4014B (ref. to CL)	5	–	40	80	ns
	10	–	25	50	
	15	–	20	40	
Parallel Inputs CD4021B (ref. to P/S)	5	–	25	50	ns
	10	–	15	30	
	15	–	10	20	
Parallel/Serial Control CD4014B (ref. to CL)	5	–	90	180	ns
	10	–	40	80	
	15	–	30	60	
Minimum Hold Time, t_H: Serial In, Parallel In, Parallel/Serial Control	5	–	–	0	ns
	10	–	–	0	
	15	–	–	0	
Minimum P/S Pulse Width, t_{WH} (CD4021B)	5	–	80	160	ns
	10	–	40	80	
	15	–	25	50	
Minimum P/S Removal Time, t_{REM} CD4021B (ref. to CL)	5	–	140	280	ns
	10	–	70	140	
	15	–	50	100	
Average Input Capacitance, C_I	Any Input	–	5	7.5	pF

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

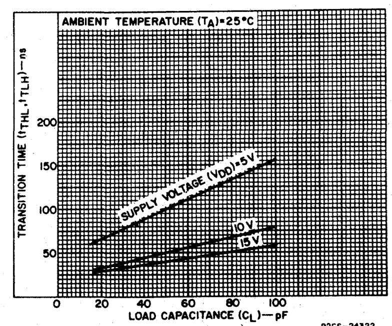


Fig. 7 – Typical transition time as a function of load capacitance.

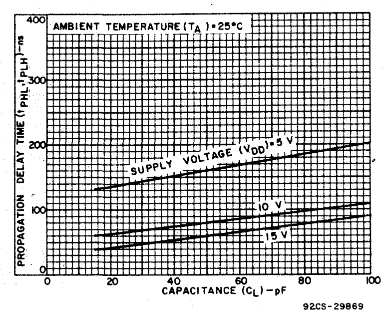


Fig. 8 – Typical propagation delay time as a function of load capacitance.

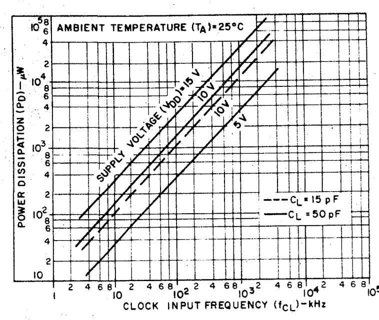


Fig. 9 – Typical dynamic power dissipation as a function of clock input frequency.

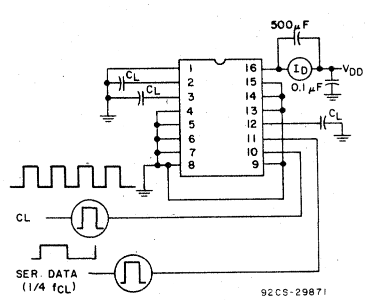


Fig. 10 – Dynamic power dissipation test circuit.

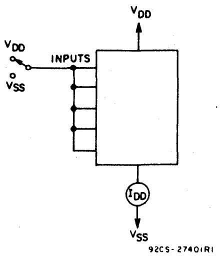


Fig. 11 – Quiescent device current test circuit.

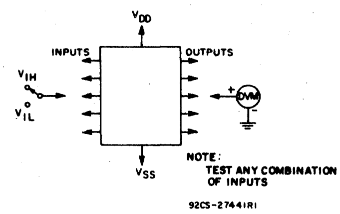


Fig. 12 – Input voltage test circuit.

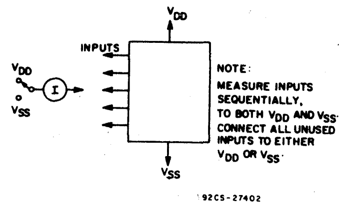
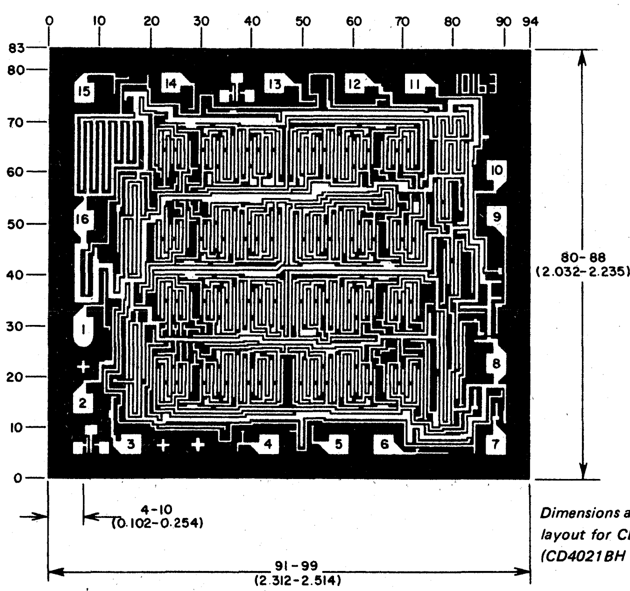


Fig. 13 – Input current test circuit.



Dimensions and pad layout for CD4014BH (CD4021BH is identical)

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

COS/MOS Dual 4-Stage Static Shift Register

With Serial Input/Parallel Output

High-Voltage Types (20-Volt Rating)

The RCA-CD4015B consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the DATA input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one CD4015B package, or to more than 8 stages using additional CD4015B's is possible.

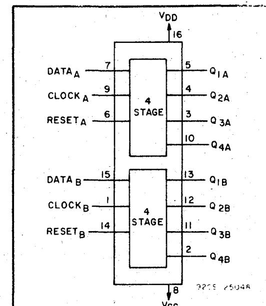
The CD4015B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **Medium speed operation . . . .**
  12 MHz (typ.) clock rate at $V_{DD} - V_{SS}$ = 10 V
- **Fully static operation**
- **8 master-slave flip-flops plus input and output buffering**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) =**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

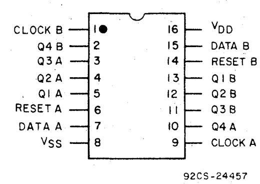
Applications:

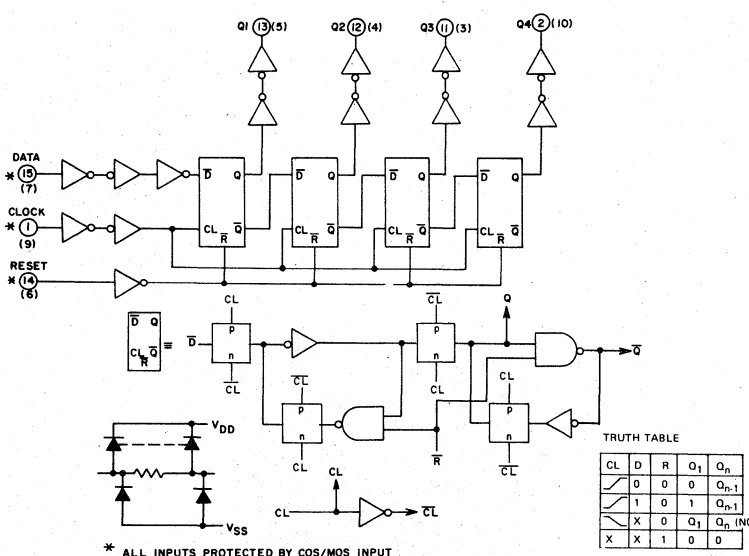
- **Serial-input/parallel-output data queueing**
- **Serial to parallel data conversion**
- **General-purpose register**



CD4015B FUNCTIONAL DIAGRAM

TERMINAL DIAGRAM





* ALL INPUTS PROTECTED BY COS/MOS INPUT PROTECTION NETWORK

TRUTH TABLE

CL	D	R	Q_1	Q_n
⟋ (positive edge)	0	0	0	Q_{n-1}
⟋ (positive edge)	1	0	1	Q_{n-1}
⟍ (negative edge)	X	0	Q_1	Q_n (NO CHANGE)
X	X	1	0	0

X = DON'T CARE CASE

Fig. 1 – Logic diagram (1 register).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)			3	18	V
Clock Pulse Width,	t_WCL	5	180	—	ns
		10	80	—	
		15	50	—	
Clock Rise and Fall Time,	t_rCL, t_fCL	5	—	15	µs
		10	—		
		15	—		
Clock Input Frequency,	f_{CL}	5	DC	3	MHz
		10		6	
		15		8.5	
Data Setup Time,	t_{SU}	5	70	—	ns
		10	40	—	
		15	30	—	
Reset Pulse Width,	t_WR	5	200	—	ns
		10	80	—	
		15	60	—	

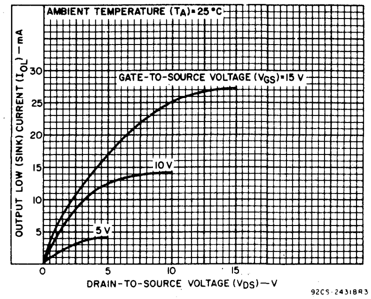


Fig. 2 — Typical output low (sink) current characteristics.

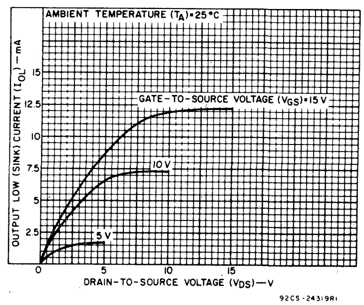


Fig. 3 — Minimum output low (sink) current characteristics.

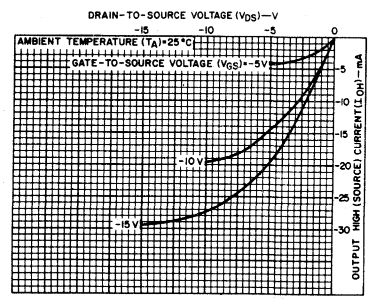


Fig. 4 — Typical output high (source) current characteristics.

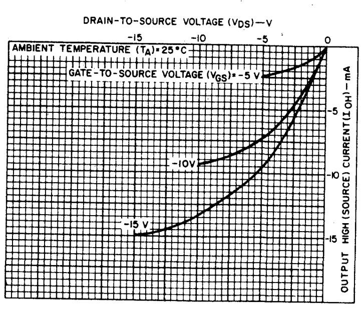


Fig. 5 — Minimum output high (source) current characteristics.

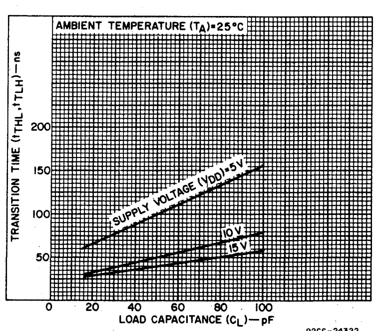


Fig. 6 — Typical transition time as a function of load capacitance.

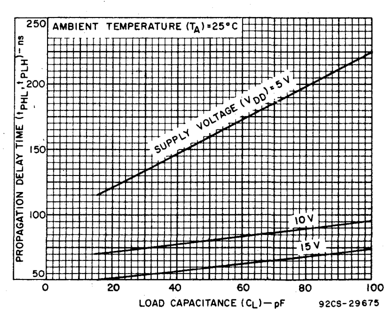
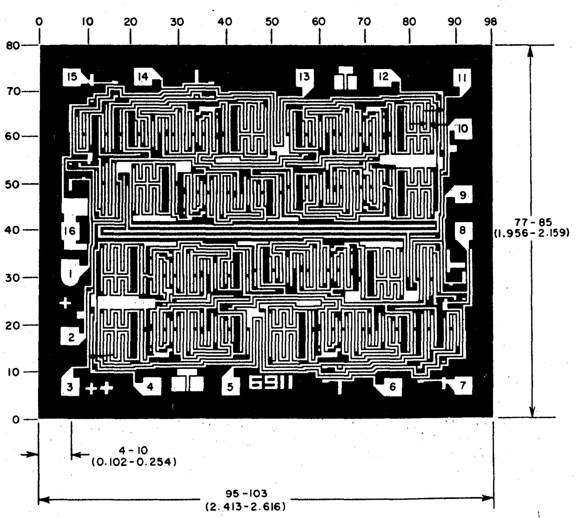


Fig. 7 — Typical propagation delay time as a function of load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA



Photograph of Chip Layout for CD4015B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4015B Types

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25°C$, Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200\ k\Omega$*

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
		V_{DD}(V)	Min.	Typ.	Max.	
CLOCKED OPERATION						
Propagation Delay Time; t_{PHL}, t_{PLH}		5	–	160	320	ns
		10	–	80	160	
		15	–	60	120	
Transition Time; t_{THL}, t_{TLH}		5	–	100	200	
		10	–	50	100	
		15	–	40	80	
Minimum Clock Pulse Width, t_WCL		5	–	90	180	
		10	–	40	80	
		15	–	25	50	
Clock Rise & Fall Time; t_rCL, t_fCL*		5	–	–	15	µs
		10	–	–	15	
		15	–	–	15	
Minimum Data Setup Time, t_{SU}		5	–	35	70	ns
		10	–	20	40	
		15	–	15	30	
Maximum Clock Input Frequency, f_{CL}		5	3	6	–	MHz
		10	6	12	–	
		15	8.5	17	–	
Input Capacitance, C_{IN}	Any Input		–	5	7.5	pF
RESET OPERATION						
Propagation Delay Time, t_{PHL}		5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
Minimum Reset Pulse Width t_WR		5	–	100	200	
		10	–	40	80	
		15	–	30	60	

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

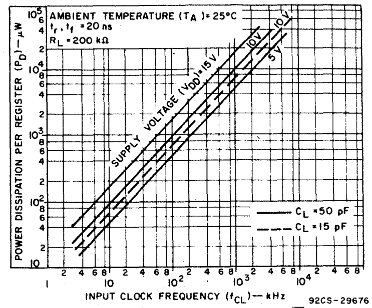


Fig. 8 – Typical power dissipation as a function of frequency.

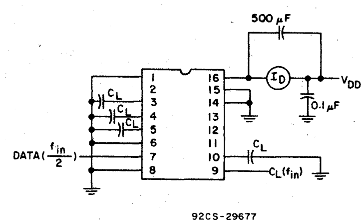


Fig. 9 – Power dissipation test circuit.

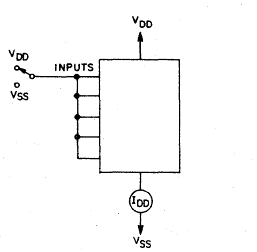


Fig. 10 – Quiescent device current test circuit.

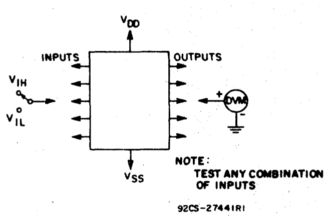


Fig. 11 – Input voltage test circuit.

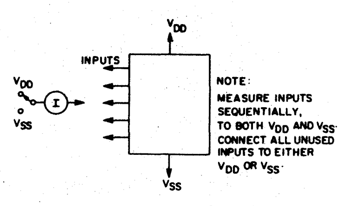


Fig. 12 – Input current test circuit.

COS/MOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

High-Voltage Types (20-Volt Rating)

The RCA-CD4016B Series types are quad bilateral switches intended for the transmission or multiplexing of analog or digital signals. Each of the four independent bilateral switches has a single control signal input which simultaneously biases both the p and n device in a given switch on or off.

The CD4016 "B" Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

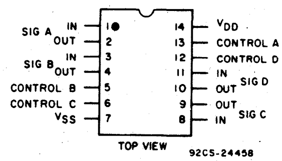
Features:

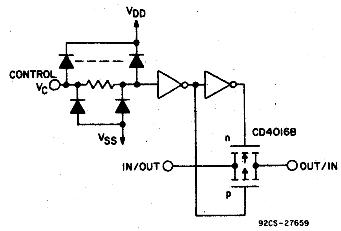
- **20-V digital or ± 10-V peak-to-peak switching**
- **280-Ω typical on-state resistance for 15-V operation**
- **Switch on-state resistance matched to within 10 Ω typ. over 15-V signal-input range**
- **High on/off output-voltage ratio: 65 dB typ. @ f_{is} = 10 kHz, R_L = 10 kΩ**
- **High degree of linearity: <0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 V_{p-p}, $V_{DD}-V_{SS} \geq$ 10 V, R_L = 10 kΩ**
- **Extremely low off-state switch leakage resulting in very low offset current and high effective off-state resistance: 100 pA typ. @ $V_{DD}-V_{SS}$=18 V, T_A=25°C**
- **Extremely high control input impedance (control circuit isolated from signal circuit: 10^{12} Ω typ.**
- **Low crosstalk between switches: –50 dB typ. @ f_{is} = 0.9 MHz, R_L = 1 kΩ**
- **Matched control-input to signal-output capacitance: Reduces output signal transients**
- **Frequency response, switch on = 40 MHz (typ.)**
- **100% tested for quiescent current at 20 V**
- **Maximum control input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V at 25°C**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

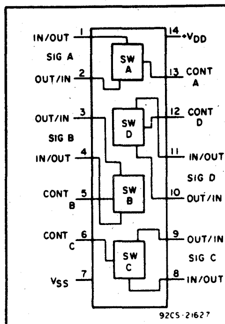
- **Analog signal switching/multiplexing**
  - **Signal gating**
  - **Squelch control**
  - **Chopper**
  - **Modulator**
  - **Demodulator**
  - **Commutating switch**
- **Digital signal switching/multiplexing**
- **COS/MOS logic implementation**
- **Analog-to-digital & digital-to-analog conversion**
- **Digital control of frequency, impedance, phase, and analog-signal gain**

Terminal Assignment





Schematic diagram - 1 of 4 identical sections.



Functional Diagram

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT (INCLUDING TRANSMISSION GATE) . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D, F) . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER TRANSMISSION GATE
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . –55 to +125°C
PACKAGE TYPE E . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . +265°C

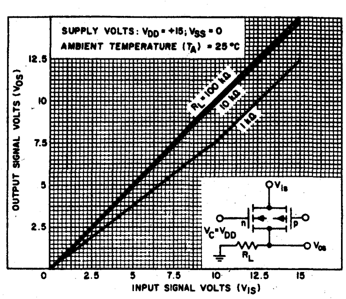


Fig. 1– Typ. on-state characteristics for 1 of 4 switches with V_{DD} = +15 V, V_{SS} = 0 V.

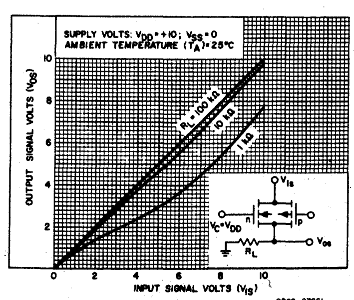


Fig. 2– Typ. on-state characteristics for 1 of 4 switches with V_{DD} = +10 V, V_{SS} = 0 V.

CD4016B Types

ELECTRICAL CHARACTERISTICS

Characteristic	Test Conditions		V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURE (°C) Values at −55, +25, +125 Apply to D, F, H Packages Values at −40, +25, +85 Apply to E Package −55	−40	+85	+125	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD}			0,5	5	0.25	0.25	7.5	7.5	0.01	0.25	µA
			0,10	10	0.5	0.5	15	15	0.01	0.5	
			0,15	15	1	1	30	30	0.01	1	
			0,20	20	5	5	150	150	0.02	5	
Signal Inputs (V_{is}) and Output (V_{os})											
On-State Resistance, r_{on} Max.	$V_C = V_{DD}$, $R_L = 10 k\Omega$ Returned to $\frac{V_{DD}-V_{SS}}{2}$	$V_{is}=V_{DD}$ or V_{SS}		10	600	610	840	960	–	660	Ω
		V_{is}=4.75 to 5.75 V		10	1870	1900	2380	2600	–	2000	
		$V_{is}=V_{DD}$ or V_{SS}		15	360	370	520	600	–	400	
		V_{is}=7.25 to 7.75 V		15	775	790	1080	1230	–	850	
ΔOn-State Resistance Between Any 2 Switches, Δr_{on}	$R_L = 10 k\Omega$, $V_C = V_{DD}$			5	–	–	–	–	15	–	Ω
				10	–	–	–	–	10	–	
				15	–	–	–	–	5	–	
Total Harmonic Distortion, THD	$V_C=V_{DD}$ = 5 V, V_{SS} = −5 V, $V_{is(p\text{-}p)}$ = 5 V (Sine wave centered on 0 V) R_L=10 kΩ, f_{is}=1 kHz sine wave				–	–	–	–	0.4	–	%
−3dB Cutoff Frequency (Switch on)	$V_C=V_{DD}$=5 V, V_{SS}= −5 V, $V_{is(p\text{-}p)}$ =5 V (Sine wave centered on 0 V) R_L = 1 kΩ,				–	–	–	–	40	–	MHz
−50dB Feed-through Frequency (Switch off)	$V_C=V_{SS}$= −5 V, $V_{is(p\text{-}p)}$=5 V (Sine wave centered on 0 V) R_L = 1 kΩ				–	–	–	–	1.25	–	MHz
Input/Output Leakage Current (Switch off) I_{is} Max.	V_C = 0 V, V_{is} = 18 V, V_{os} = 0 V; V_{is} = 0 V, V_{os} = 18 V			18	±0.1	±0.1	±1	±1	10^{-4}	±0.1	µA
−50 dB Crosstalk Frequency	$V_C(A) = V_{DD}$ = +5 V, $V_C(B) = V_{SS}$ = −5 V, $V_{is}(A)$ = 5 $V_{p\text{-}p}$, 50 Ω source R_L = 1 kΩ				–	–	–	–	0.9	–	MHz
Propagation Delay (Signal Input to Signal Output) t_{pd}	R_L = 200 kΩ, $V_C = V_{DD}$, V_{SS} = GND, C_L = 50 pF, V_{is} = 10 V (Square wave centered on 5 V t_r, t_f = 20 ns			5	–	–	–	–	40	100	ns
				10	–	–	–	–	20	40	
				15	–	–	–	–	15	30	
Capacitance: Input, C_{is}	V_{DD} = +5 V, $V_C = V_{SS}$ = −5 V				–	–	–	–	4	–	pF
Output, C_{os}					–	–	–	–	4	–	
Feedthrough, C_{ios}					–	–	–	–	0.2	–	

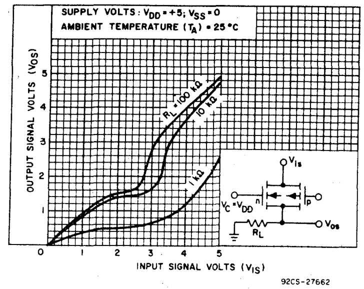


Fig. 3—Typ. on-state characteristics for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = 0 V.

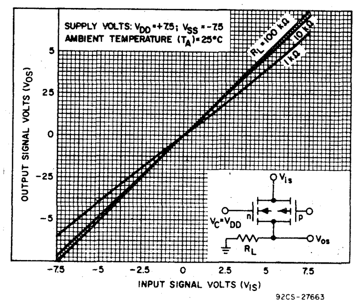


Fig. 4—Typ. on-state characteristics for 1 of 4 switches with V_{DD} = +7.5 V, V_{SS} = −7.5 V.

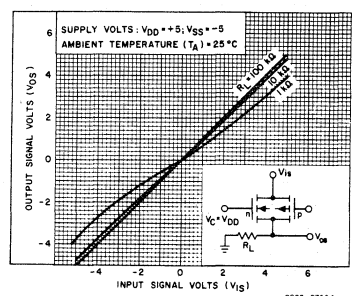


Fig. 5— Typ. on-state characteristics for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = −5 V.

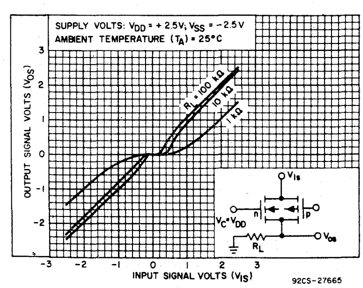


Fig. 6— Typ. on-state characteristics for 1 of 4 switches with V_{DD} = +2.5 V, V_{SS} = −2.5 V.

ELECTRICAL CHARACTERISTICS (cont'd)

Characteristic	Test Conditions	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURE (°C) Values at −55, +25, +125 Apply to D, F, H Packages Values at −40, +25, +85 Apply to E Package −55	−40	+85	+125	+25 Typ.	+25 Max.	UNITS
Control (V_C)									
Control Input Low Voltage, V_{ILC} (Max.)	$\lvert I_{is}\rvert < 10\,\mu A$ $V_{is} = V_{SS}, V_{OS} = V_{DD}$ and $V_{is} = V_{DD}, V_{OS} = V_{SS}$	5,10, 15	0.9	0.9	0.4	0.4	–	0.7	V
Control Input High Voltage, V_{IHC}	See Fig. 1	5	3.5 (Min.)						V
		10	7 (Min.)						
		15	11 (Min.)						
Input Current, I_{IN} (Max.)	$V_{is} \leq V_{DD}$ $V_{DD} - V_{SS} = 18\,V$ $V_{CC} \leq V_{DD} - V_{SS}$	18	±0.1	±0.1	±1	±1	$\pm 10^{-5}$	±0.1	µA
Crosstalk (Control Input to Signal Output)	$V_C = 10\,V$ (Sq. Wave) $t_r, t_f = 20\,ns$ $R_L = 10\,k\Omega$	10	–	–	–	–	50	–	mV
Turn-On Propagation Delay	$t_r, t_f = 20\,ns$ $C_L = 50\,pF$ $R_L = 1\,k\Omega$	5	–	–	–	–	35	70	ns
		10	–	–	–	–	20	40	
		15	–	–	–	–	15	30	
Maximum Control Input Repetition Rate	$V_{is} = V_{DD}, V_{SS} = GND$, $R_L = 1\,k\Omega$ to gnd, $C_L = 50\,pF$, $V_C = 10\,V$ (Square wave centered on 5 V) $t_r, t_f = 20\,ns$, $V_{os} = ½\,V_{os}$ @ 1 kHz	10	–	–	–	–	10	–	MHz
Input Capacitance, C_{IN}			–	–	–	–	5	7.5	µF

V_{DD} (V)	V_{is} (V)	Switch Input I_{is} (mA) −55°C	−40°C	25°C*	25°C▲	+85°C	+125°C	Switch Output V_{os} (V) Min.	Max.
5	0	0.25	0.2	0.2	0.16	0.12	0.14	–	0.4
5	5	−0.25	−0.2	−0.2	−0.16	−0.12	−0.14	4.6	–
10	0	0.62	0.5	0.5	0.4	0.3	0.35	–	0.5
10	10	−0.62	−0.5	−0.5	−0.4	−0.3	−0.35	9.5	–
15	0	1.8	1.4	1.5	1.2	1	1.1	–	1.5
15	15	−1.8	−1.4	−1.5	−1.2	−1	−1.1	13.5	–

* Plastic package ▲ Ceramic package

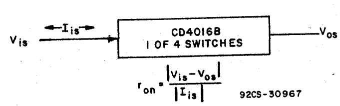


Fig. 10— Determination of r_{on} as a test condition for control input high voltage (V_{IHC}) specification.

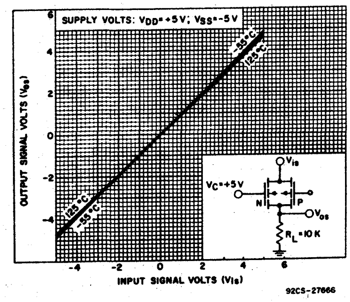


Fig. 7— Typ. on-state characteristics as a function of temp. for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = −5 V.

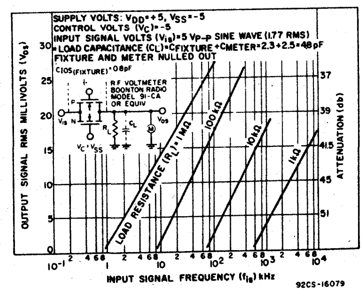


Fig. 8 – Typ. feedthru vs. frequency – switch off.

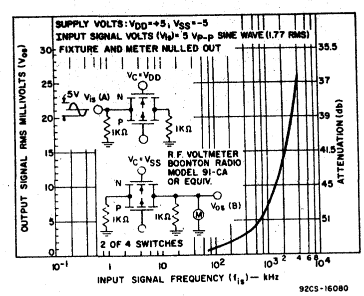


Fig. 9— Typical crosstalk between switch circuits in the same package.

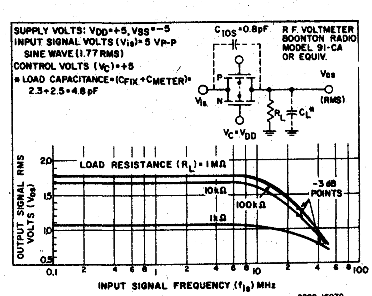


Fig. 11 – Typical frequency response – switch on.

TYPICAL ON-STATE RESISTANCE CHARACTERISTICS, $T_A = 25^oC$

CHARAC-TERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			R_L = 1kΩ		R_L = 10kΩ		R_L = 100kΩ	
	V_{DD} (V)	V_{SS} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)
r_{on}	+15	0	200	+15	200	+15	180	+15
			200	0	200	0	200	0
r_{on} (max.)	+15	0	300	+11	300	+9.3	320	+9.2
r_{on}	+10	0	290	+10	250	+10	240	+10
			290	0	250	0	300	0
r_{on} (max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
r_{on}	+ 5	0	860	+ 5	470	+ 5	450	+ 5
			600	0	580	0	800	0
r_{on} (max.)	+ 5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
r_{on}	+7.5	−7.5	200	+7.5	200	+7.5	180	+7.5
			200	−7.5	200	−7.5	180	−7.5
r_{on} (max.)	+7.5	−7.5	290	±0.25	280	±25	400	±0.25
r_{on}	+ 5	− 5	260	+ 5	250	+ 5	240	+ 5
			310	− 5	250	− 5	240	− 5
r_{on} (max.)	+ 5	− 5	600	±0.25	580	±0.25	760	±0.25
r_{on}	+2.5	−2.5	590	+2.5	450	+2.5	490	+2.5
			720	−2.5	520	−2.5	520	−2.5
r_{on} (max.)	+2.5	−2.5	232k	±0.25	300k	±0.25	870k	±0.25

* Variation from aperfect switch, r_{on} = 0 Ω.

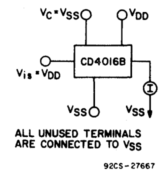


Fig. 12 — Off-state switch input or output leakage current test circuit.

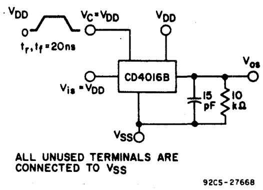
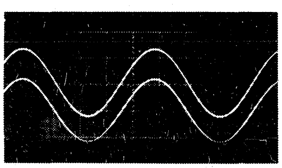


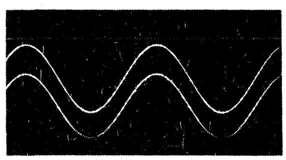
Fig. 13 — Test circuit for square-wave response.



SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV
VDD = VC = +7.5V, VSS = -7.5V, RL = 10KΩ
CL = 15 pF
fIS = 1 KHz VIS = 5V p-p
DISTORTION = 0.2 %

92CS-27612

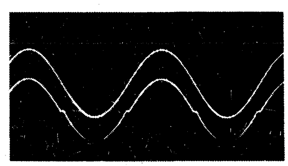
Fig. 14 — Typical sine wave response of V_{DD} = +7.5 V, V_{SS} = −7.5 V.



SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV
VDD = VC = +5 V, VSS = -5 V, RL = 10KΩ
CL = 15 pF
fIS = 1 KHz VIS = 5 V p-p
DISTORTION = 0.4 %

92CS-27613

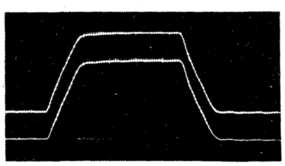
Fig. 15 — Typical sine wave response of V_{DD} = +5 V, V_{SS} = −5 V.



SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV
VDD = VC = +2.5V, VSS = -2.5V, RL = 10KΩ
CL = 15 pF
fIS = 1 KHz VIS = 5V p-p
DISTORTION = 3 %

92CS-27614

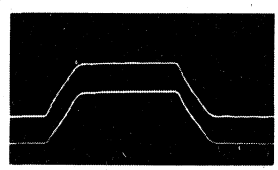
Fig. 16 — Typical sine wave response of V_{DD} = +2.5 V, V_{SS} = −2.5 V.



SCALE: X = 100 ns/DIV
Y = 5.0 V/DIV

92CS-27615

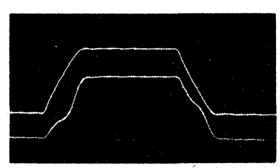
Fig. 17 — Typical square wave response at V_{DD} = V_C = +15 V, V_{SS} = Gnd.



SCALE: X = 100 ns/DIV
Y = 5.0 V/DIV

92CS-27616

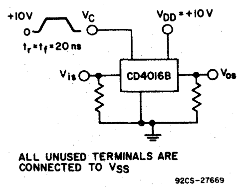
Fig. 18 — Typical square wave response at V_{DD} = V_C = +10 V, V_{SS} = Gnd.



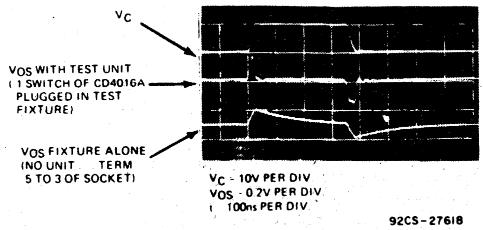
SCALE: X = 100 ns/DIV
Y = 2 V/DIV

92CS-27617

Fig. 19 — Typical square wave response at V_{DD} = V_C = +5 V, V_{SS} = Gnd.



(a)



(b)

Fig.20 – Crosstalk-control input to signal output.

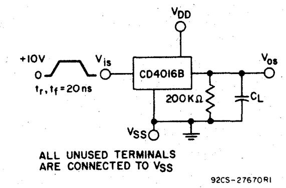


Fig.21 – Propagation delay time signal input (V_{IS}) to signal output (V_{OS}).

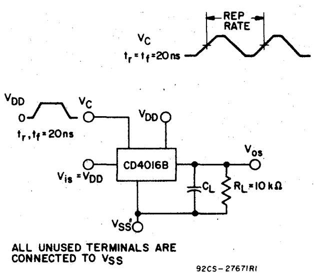


Fig. 22 – Max. control-input repetition rate.

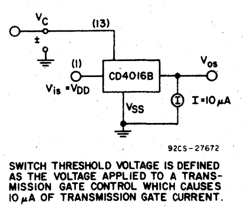


Fig.23 – Switch threshold voltage.

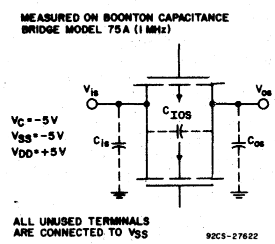
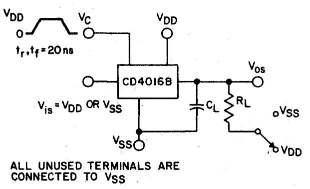


Fig.24 – Capacitance C_{IOS} and C_{OS}.



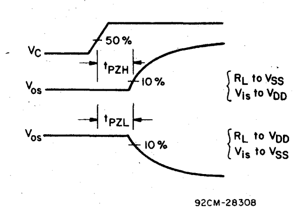
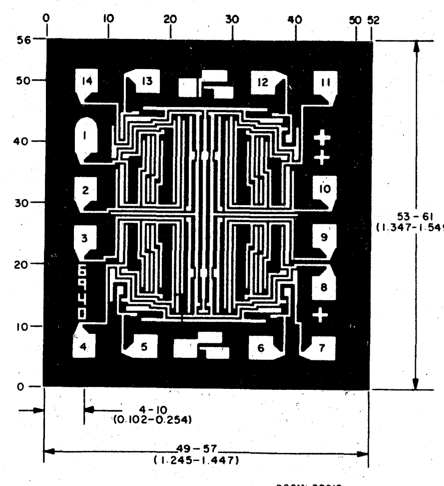


Fig.25 – Turn-On propagation delay-control input.

Dimensions and pad layout for CD4016BH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4017B, CD4022B Types

COS/MOS Counter/Dividers

High-Voltage Types (20-Volt Rating)

CD4017B—Decade Counter with 10 Decoded Outputs

CD4022B—Octal Counter with 8 Decoded Outputs

The RCA-CD4017B and CD4022B are 5-stage and 4-stage Johnson counters having 10 and 8 decoded outputs, respectively. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal. Schmitt trigger action in the CLOCK input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times.

These counters are advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson counter configuration permits high-speed operation, 2-input decode-gating and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A CARRY-OUT signal completes one cycle every 10 clock input cycles in the CD4017B or every 8 clock input cycles in the CD4022B and is used to ripple-clock the succeeding device in a multi-device counting chain.

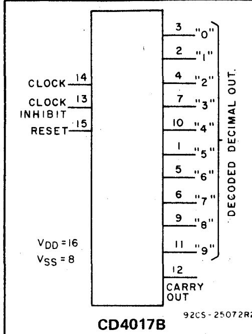
The CD4017B and CD4022B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

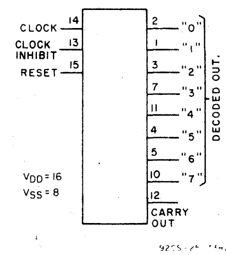
- **Fully static operation**
- **Medium-speed operation . . . 10 MHz (typ.) at V_{DD} = 10 V**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Decade counter/decimal decode display (CD4017B)**
- **Binary counter/decoder**
- **Frequency division**
- **Counter control/timers**
- **Divide-by-N counting**
- **For further application information, see ICAN-6166 "COS/MOS MSI Counter and Register Design and Applications"**



CD4017B Functional Diagram

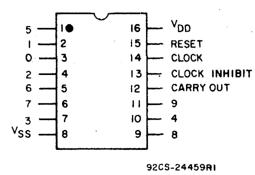


CD4022B Functional Diagram

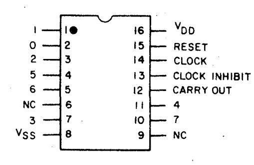
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

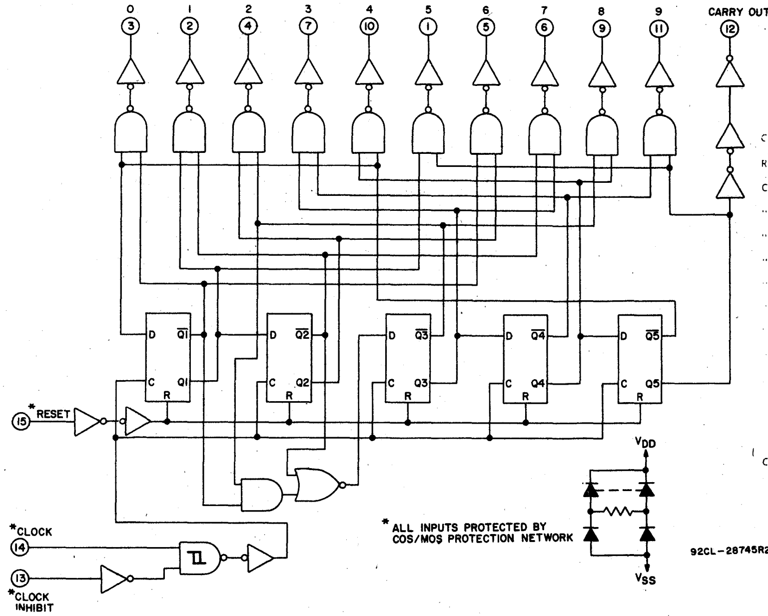
CHARACTERISTICS	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Clock Input Frequency, f_{CL}	5	–	2.5	MHz
	10	–	5	
	15	–	5.5	
Clock Pulse Width, t_W	5	200	–	ns
	10	90	–	
	16	60	–	
Clock Rise & Fall Time, t_{rCL}, t_{fCL}	5	UNLIMITED		
	10			
	15			
Clock Inhibit Setup Time, t_s	5	230	–	ns
	10	100	–	
	15	70	–	
Reset Pulse Width, t_{RW}	5	260	–	ns
	10	110	–	
	15	60	–	
Reset Removal Time, t_{rem}	5	400	–	ns
	10	280	–	
	15	150	–	



TOP VIEW
CD4017B
TERMINAL DIAGRAM



TOP VIEW
NC - no connection
CD4022B
TERMINAL DIAGRAM



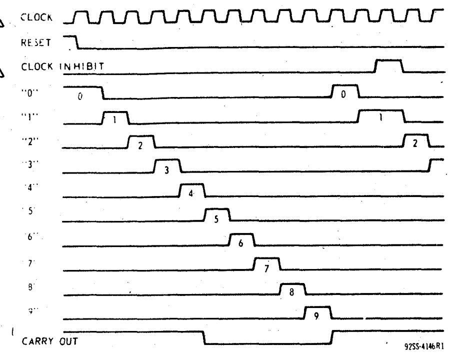


Fig. 2 – Timing diagram for CD4017B.

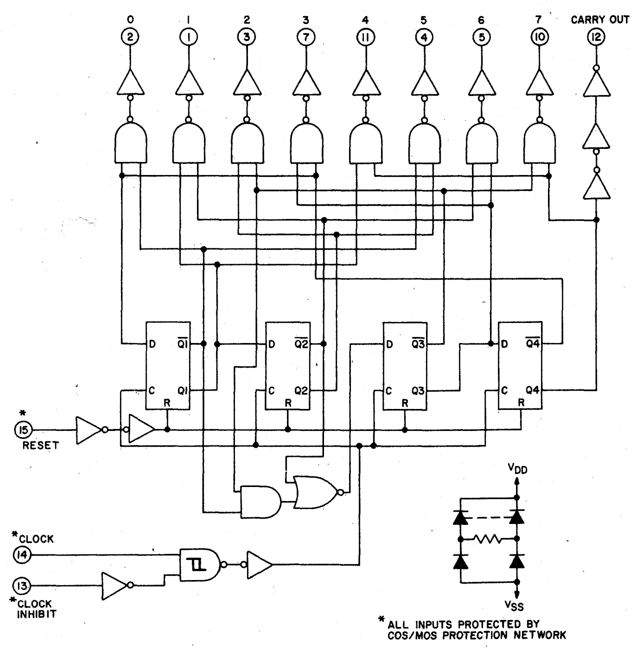


Fig. 3 – Logic diagram for CD4022B.

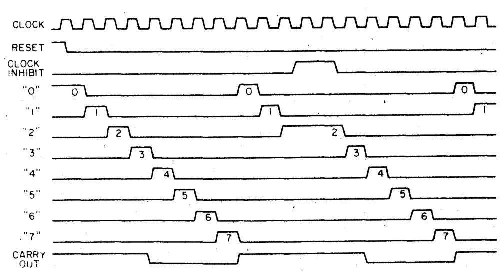


Fig. 4 – Timing diagram for CD4022B.

CD4017B, CD4022B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . −55 to +125°C
PACKAGE TYPE E . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . +265°C

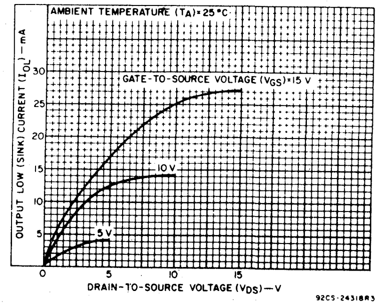


Fig. 5— Typical output low (sink) current characteristics.

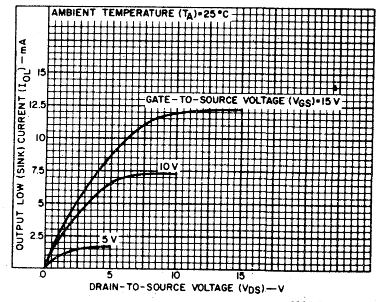


Fig. 6— Minimum output low (sink) current characteristics.

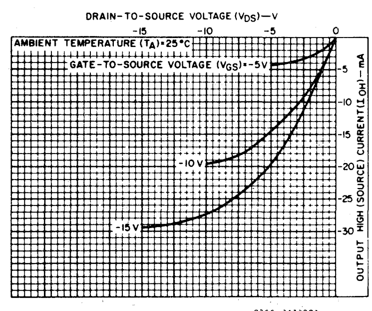


Fig. 7— Typical output high (source) current characteristics.

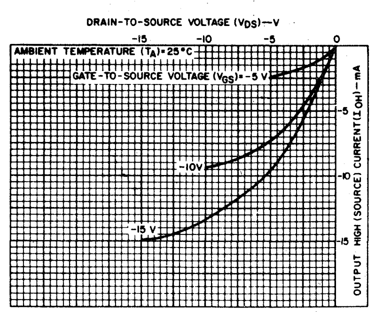


Fig. 8— Minimum output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages; Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage High-Level V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^oC$, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
CLOCKED OPERATION					
Propagation Delay Time, t_{PHL}, t_{PLH} Decode Out	5	–	325	650	ns
	10	–	135	270	
	15	–	85	170	
Carry Out	5	–	300	600	
	10	–	125	250	
	15	–	80	160	
Transition Time, t_{THL}, t_{TLH} Carry Out or Decode Out Line	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Maximum Clock Input Frequency, f_{CL}*	5	2.5	5	–	MHz
	10	5	10	–	
	15	5.5	11	–	
Minimum Clock Pulse Width, t_W	5	–	100	200	ns
	10	–	45	90	
	15	–	30	60	
Clock Rise or Fall Time, t_rCL, t_fCL	5, 10, 15	UNLIMITED			
Minimum Clock Inhibit to Clock Setup Time, t_s	5	–	115	230	ns
	10	–	50	100	
	15	–	35	70	
Input Capacitance, C_{IN}	Any Input	–	5	–	pF
RESET OPERATION					
Propagation Delay Time, t_{PHL}, t_{PLH} Carry Out or Decode Out Lines	5	–	265	530	ns
	10	–	115	230	
	15	–	85	170	
Minimum Reset Pulse Width, t_W	5	–	130	260	ns
	10	–	55	110	
	15	–	30	60	
Minimum Reset Removal Time	5	–	200	400	ns
	10	–	140	280	
	15	–	75	150	

* Measured with respect to carry output line.

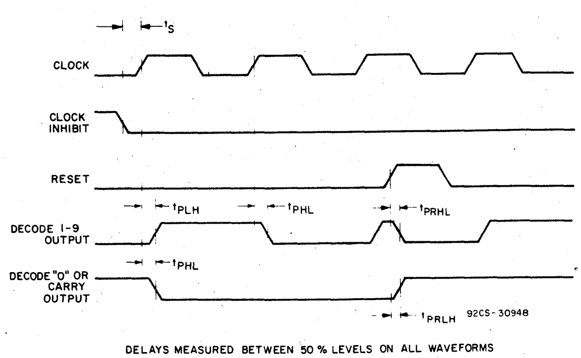


Fig. 9— Propagation delay, setup, and hold time waveforms.

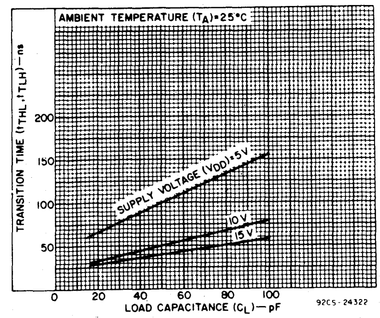


Fig. 10 – Typical transition time as a function of load capacitance.

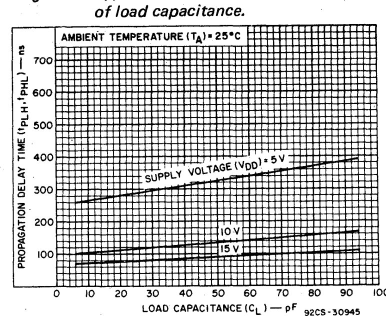


Fig. 11 – Typical propagation delay time as a function of load capacitance (clock to decode output).

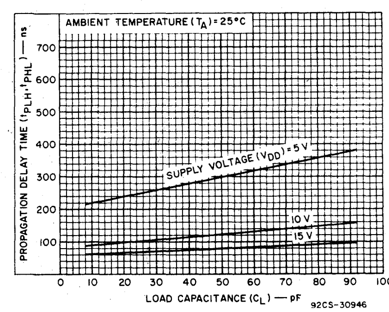


Fig. 12 – Typical propagation delay time as a function of load capacitance (clock to carry-out).

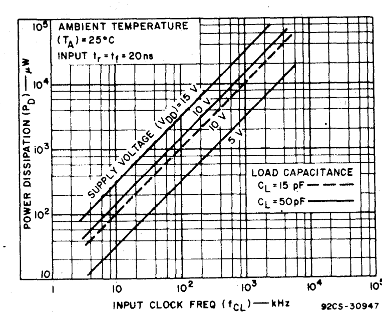


Fig. 13 – Typical dyanamic power dissipation as a function of clock input frequency.

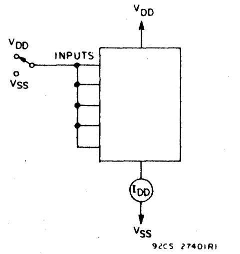


Fig. 14 – Quiescent-device-current test circuit.

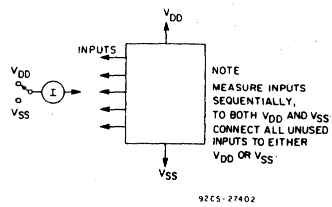


Fig. 15 – input-leakage current.

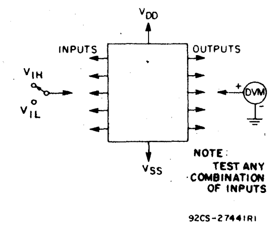


Fig. 16 – Input-voltage test circuit.

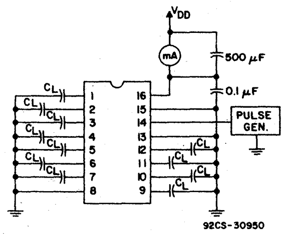


Fig. 17 – Dynamic power dissipation test circuit.

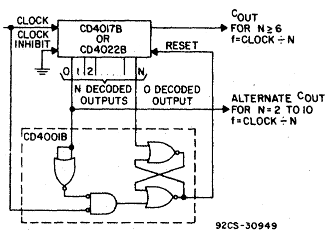
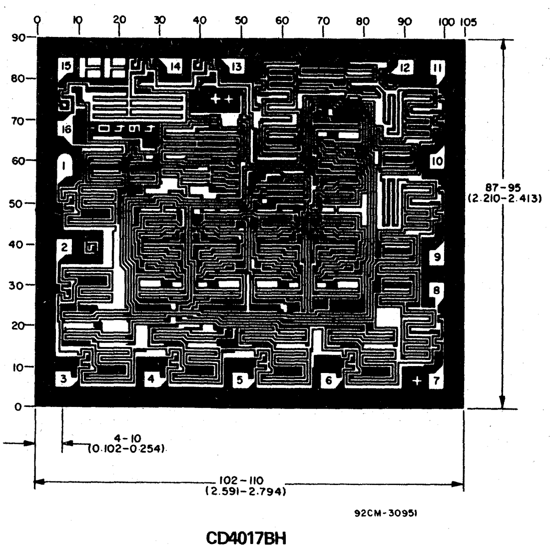
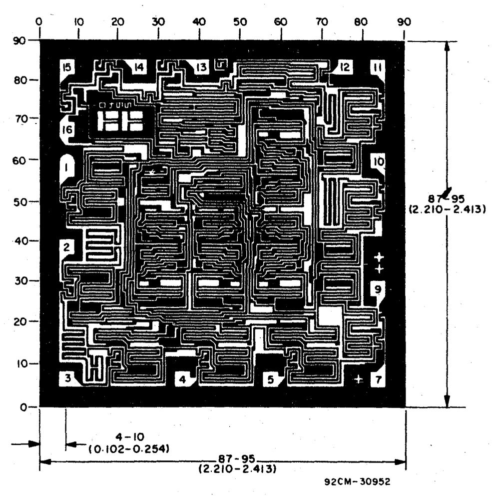


Fig. 18 – Divide by N counter (N ⩽ 10) with N decoded outputs.

When the N^{th} decoded output is reached (N^{th} clock pulse) the S-R flip flop (constructed from two NOR gates of the CD4001B) generates a reset pulse which clears the CD4017B or CD4022B to its zero count. At this time, if the N^{th} decoded output is greater than or equal to 6 in the CD-4017B or 5 in the CD4022B, the C_{OUT} line goes high to clock the next CD4017B or CD-4022B counter section. The "0" decoded output also goes high at this time. Coincidence of the clock low and decoded "0" output low resets the S-R flip flop to enable the CD4017B or CD4022B. If the N^{th} decoded output is less than 6 (CD4017B) or 5 (CD4022B), the C_{OUT} line will not go high and, therefore, cannot be used. In this case "0" decoded output may be used to perform the clocking function for the next counter.



CD4017BH



CD4022BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

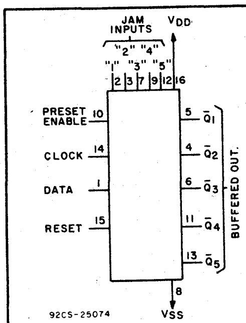
COS/MOS Presettable Divide-By-'N' Counter

High-Voltage Types (20-Volt Rating)

The RCA-CD4018B types consist of 5 Johnson-Counter stages, buffered Q outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\overline{Q}5$, $\overline{Q}4$, $\overline{Q}3$, $\overline{Q}2$, $\overline{Q}1$ signals, respectively, back to the DATA input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a CD4011B to gate the feedback connection to the DATA input. Divide-by functions greater than 10 can be achieved by use of multiple CD4018B units. The counter is advanced one count at the positive clock-signal transition. Schmitt Trigger action on the clock line permits unlimited clock rise and fall times. A high RESET signal clears the counter to an all-zero condition. A high PRESET-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

The CD4018B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

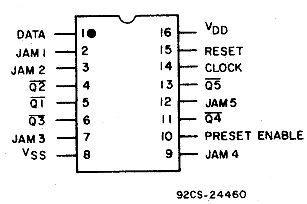
Features:
- Medium speed operation . . . . . . 10 MHz (typ.) at $V_{DD} - V_{SS} = 10$ V
- Fully static operation
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



FUNCTIONAL DIAGRAM

Applications:
- Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counters
- Fixed and programmable counters greater than 10
- Programmable decade counters
- Divide-by-"N" counters/frequency synthesizers
- Frequency division
- Counter control/timers

TERMINAL DIAGRAM
Top View



92CS-24460

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC		V_{DD}	Min.	Max.	UNITS
Supply Voltage Range (at T_A = Full Package-Temperature Range)			3	18	V
Clock Input Frequency,	f_{CL}	5 10 15	– – –	3 7 8.5	MHz
Clock Pulse Width,	t_W	5 10 15	160 70 50	– – –	ns
Clock Rise & Fall Time,	t_rCL, t_fCL	5 10 15	Unlimited		μs
Data Input Set-Up Time,	t_S	5 10 15	40 12 16	– – –	ns
Data Input Hold Time,	t_H	5 10 15	140 80 60	– – –	ns
Preset or Reset Pulse Width,	t_W	5 10 15	160 70 50	– – –	ns
Preset or Reset Removal Time		5 10 15	80 30 20	– – –	ns

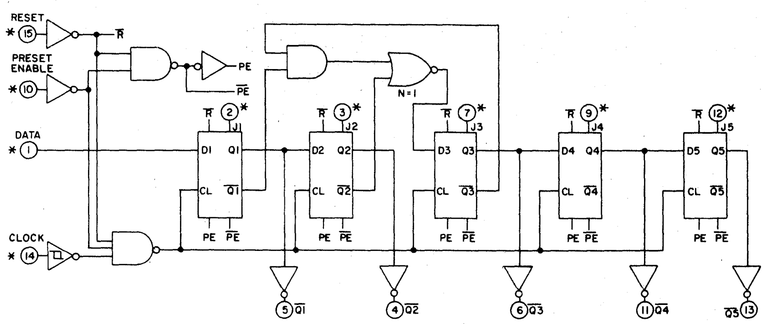


Fig. 1 – Logic diagram.

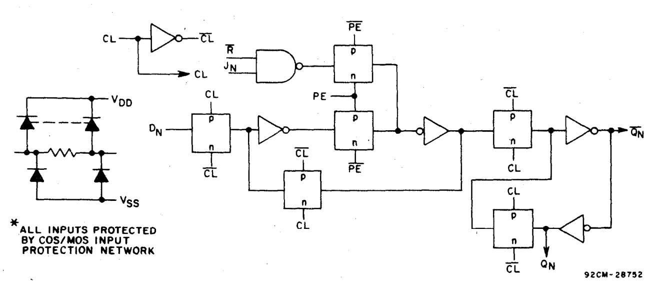


Fig. 2 – Detail of a typical stage.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages; Values at −40, +25, +85 Apply to E Package: −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

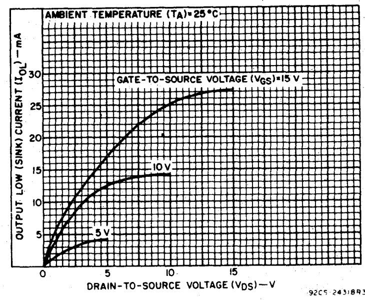


Fig. 3 – Typical output low (sink) current characteristics.

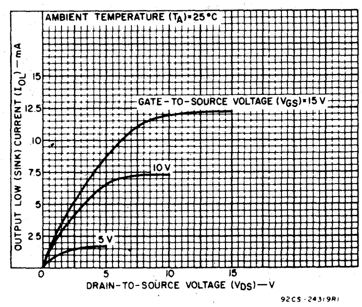


Fig. 4 – Minimum output low (sink) current characteristics.

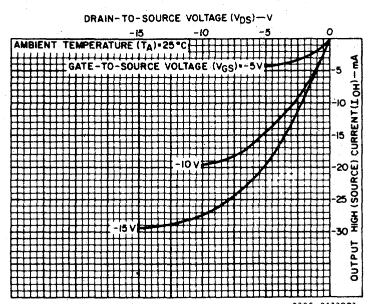


Fig. 5 – Typical output high (source) current characteristics.

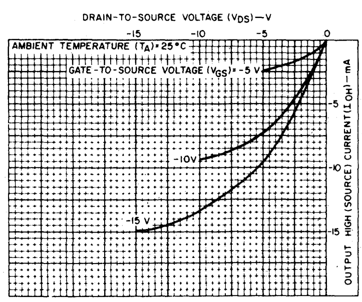


Fig. 6 – Minimum output high (source) current characteristics.

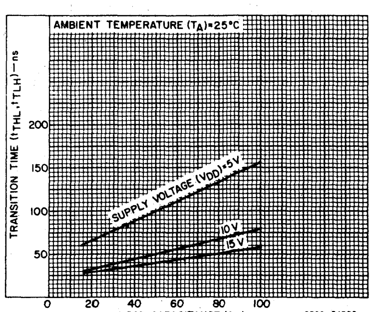


Fig. 7 – Typical transition time as a function of load capacitance.

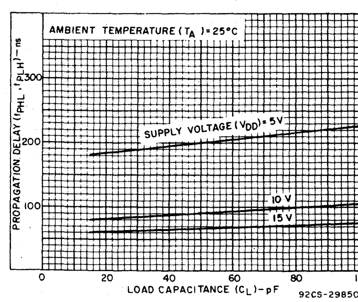


Fig. 8 – Typical propagation delay time as a function of load capacitance (CLOCK to Q).

DYNAMIC ELECTRICAL CHARATERISTICS at T_A = 25°C, Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
		V_{DD} (V)	Min.	Typ.	Max.	
CLOCKED OPERATION						
Propagation Delay Time; t_{PLH}, t_{PHL}		5	–	200	400	ns
		10	–	90	180	
		15	–	65	130	
Transition Time; t_{THL}, t_{TLH}		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Maximum Clock Input Frequency, f_{CL}		5	3	6	–	MHz
		10	7	14	–	
		15	8.5	17	–	
Minimum Clock Pulse Width, t_W		5	–	80	160	ns
		10	–	35	70	
		15	–	25	50	
Clock Rise & Fall Time; t_rCL, t_fCL		5	Unlimited			μs
		10				
		15				
Minimum Data Input Set-Up Time, t_S		5	–	20	40	ns
		10	–	6	12	
		15	–	3	6	
Minimum Data Input Hold Time, t_H		5	–	70	140	ns
		10	–	40	80	
		15	–	30	60	
Average Input Capacitance, C_I	Any Input		–	5	7.5	pF
PRESET* OR RESET OPERATION						
Propagation Delay Time; Preset or Reset to $\overline{Q}$ t_{PLH}, t_{PHL}		5	–	275	550	ns
		10	–	125	250	
		15	–	90	180	
Minimum Preset or Reset Pulse Width, t_W		5	–	80	160	ns
		10	–	35	70	
		15	–	25	50	
Minimum Preset or Reset Removal Time		5	–	40	80	ns
		10	–	15	30	
		15	–	10	20	

* At PRESET ENABLE or JAM Inputs.

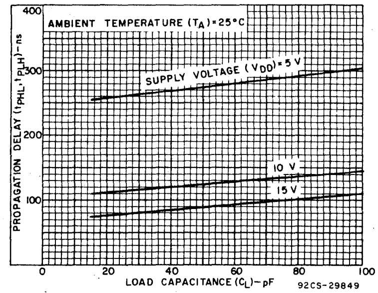


Fig. 9 – Typical propagation delay time as a function of load capacitance (RESET to Q).

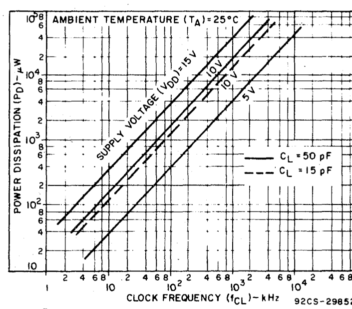


Fig. 10 – Typical dynamic power dissipation as a function of clock input frequency.

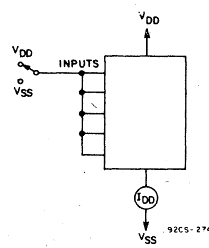


Fig. 11 – Quiescent device current test circuit.

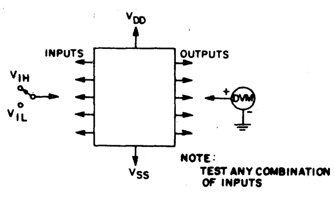


Fig. 12 – Input voltage test circuit.

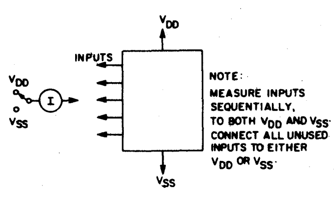


Fig. 13 – Input current test circuit.

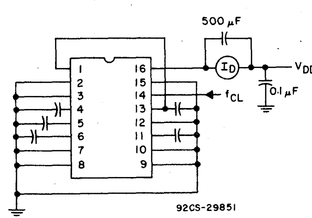


Fig. 14 – Dynamic power dissipation test circuit.

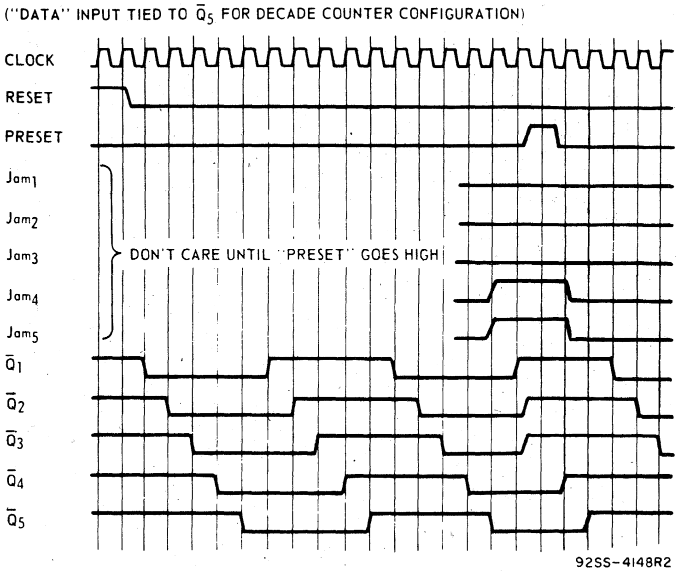


Fig. 15 — Timing diagram.

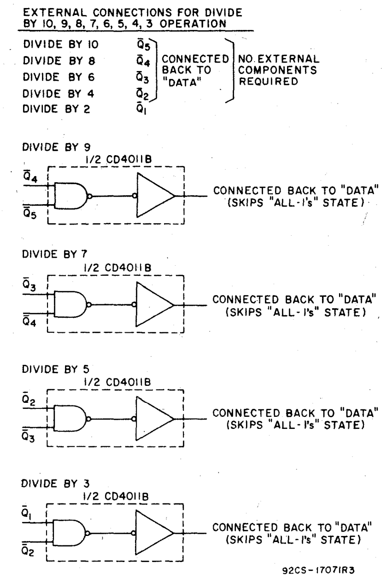
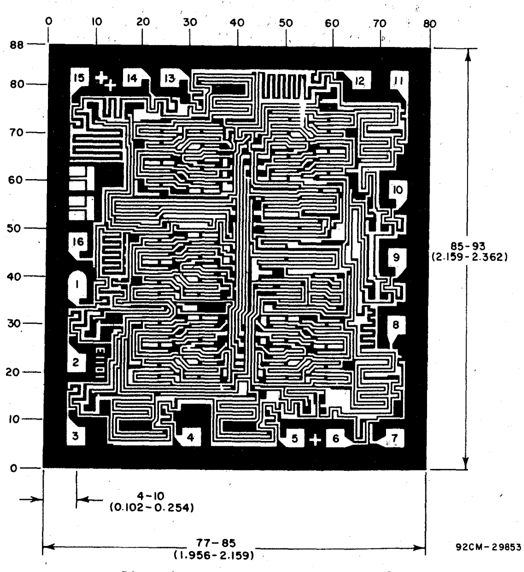


Fig. 16 — External connections for divide by 10, 9, 8, 7, 5, 4, 3, 2 operation.



Dimensions and pad layout for CD4018B,

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4019B Types

COS/MOS Quad AND/OR Select Gate

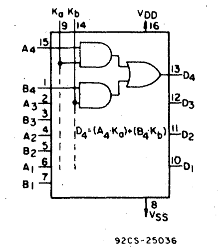
High-Voltage Types (20-Volt Rating)

The RCA-CD4019B types consist of four AND/OR select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_a and K_b. In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical A + B function.

The CD4019B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Medium-speed operation . . . . .**
  . . . $t_{PHL} = t_{PLH}$ = 60 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) = 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V**



CD4019B FUNCTIONAL DIAGRAM

Applications:

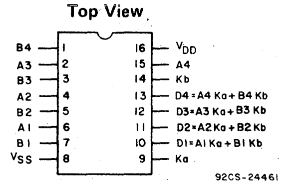
- **AND-OR select gating**
- **Shift-right/shift-left registers**
- **True/complement selection**
- **AND/OR/Exclusive-OR selection**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . . +265°C

TERMINAL DIAGRAM

Top View



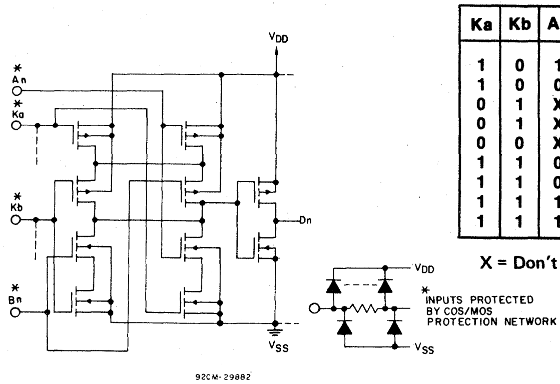


Fig. 1 — Schematic diagram for 1 of 4 identical stages.

TRUTH TABLE

Ka	Kb	An	Bn	Dn
1	0	1	X	1
1	0	0	X	0
0	1	X	1	1
0	1	X	0	0
0	0	X	X	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

X = Don't Care

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	Min.	Max.	Units
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6		
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8		
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–		0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

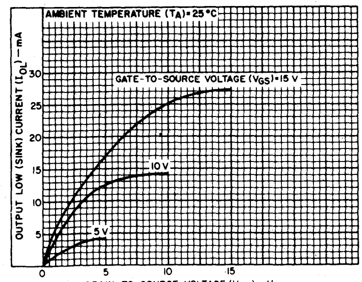


Fig. 2 – Typical output low (sink) current characteristics.

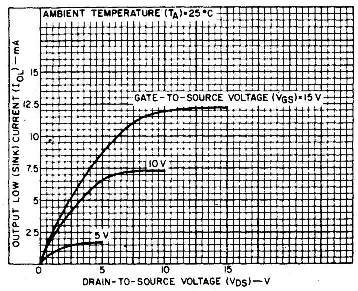


Fig. 3 – Minimum output low (sink) current characteristics.

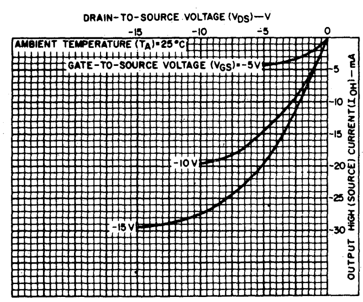


Fig. 4 – Typical output high (source) current characteristics.

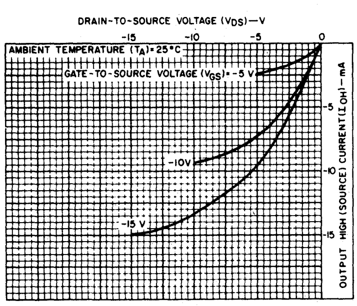


Fig. 5 – Minimum output high (source) current characteristics.

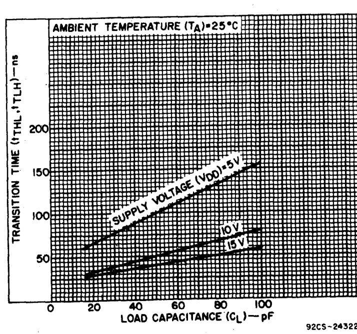


Fig. 6 – Typical transition time as a function of load capacitance.

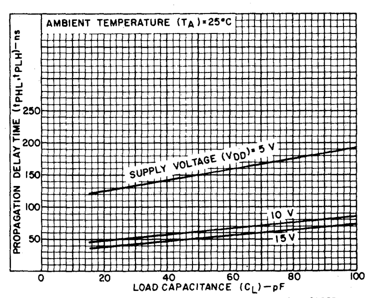


Fig. 7 – Propagation delay time as a function of load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
		V_{DD} (V)	Min.	Typ.	Max.	
Propagation Delay Time; t_{PLH}, t_{PHL}		5	–	150	300	ns
		10	–	60	120	
		15	–	50	100	
Transition Time; t_{THL}, t_{TLH}		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Input Capacitance, C_{IN}	All A and B Inputs		–	5	7.5	pF
	K_a and K_b Inputs		–	10	15	pF

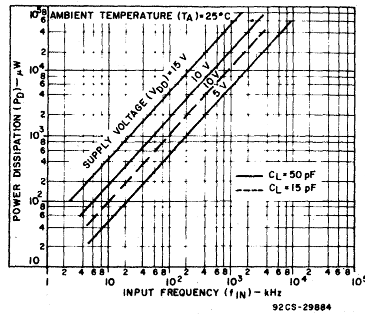


Fig. 8 — Typical dynamic power dissipation as a function of input frequency.

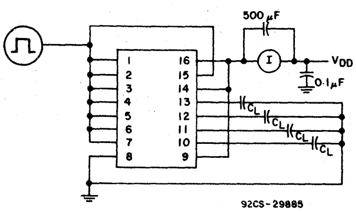


Fig. 9 — Dynamic power dissipation test circuit.

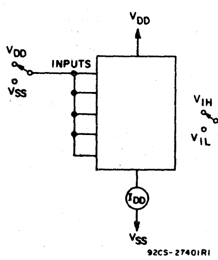


Fig. 10 — Quiescent device current test circuit.

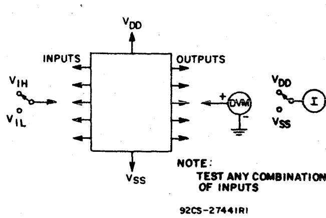


Fig. 11 — Input voltage test circuit.

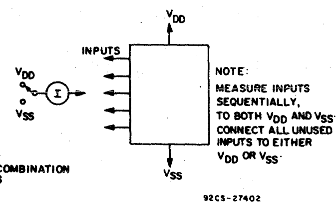


Fig. 12 — Input current test circuit.

TYPICAL APPLICATIONS

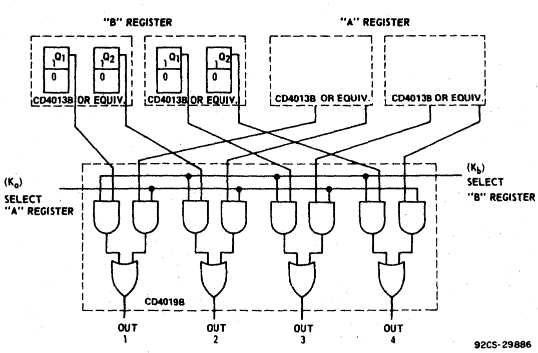


Fig. 13 — AND/OR select gating.

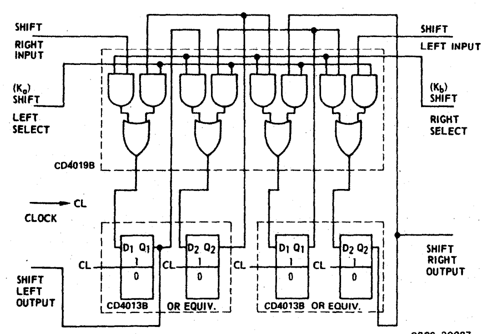
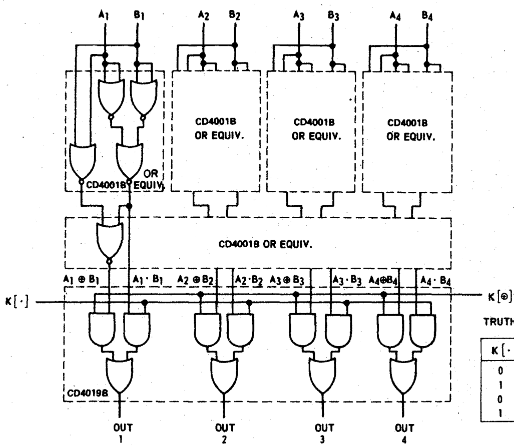


Fig. 14 — "Shift left/shift right" register.

TYPICAL APPLICATIONS (CONT'D)



TRUTH TABLE

K[·]	K[⊕]	OUT
0	0	0
1	0	A·B
0	1	A⊕B
1	1	A+B

Fig. 15 – AND/OR Exclusive-OR selector.

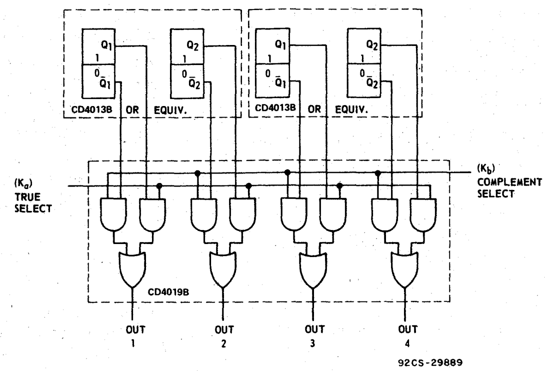
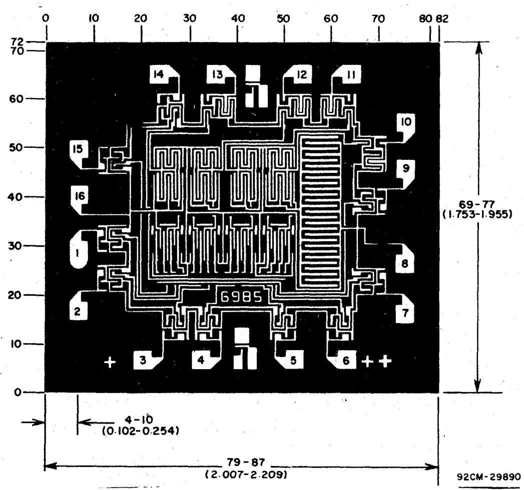


Fig. 16 – "True complement" selector.



Dimensions and pad layout for CD4019BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4020B, CD4024B, CD4040B Types

COS/MOS Ripple-Carry Binary Counter/Dividers

High-Voltage Types (20-Volt Rating)

CD4020B – 14 Stage
CD4024B – 7 Stage
CD4040B – 12 Stage

RCA-CD4020B, CD4024B, and CD4040B are ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse; a high level on the RESET line resets the counter to its all zeros state. Schmitt trigger action on the input-pulse line permits unlimited rise and fall times. All inputs and outputs are buffered.

The CD4020B and CD4040B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

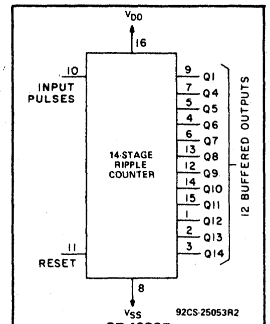
The CD4024B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

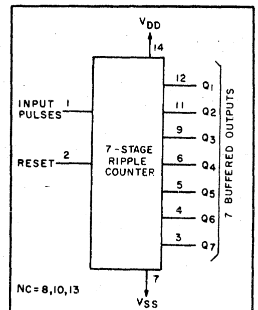
- **Medium-speed operation**
- **Fully static operation**
- **Buffered inputs and outputs**
- **100% tested for quiescent current at 20 V**
- **Standardized, symmetrical output characteristics**
- **Fully static operation**
- **Common reset**
- **5-V, 10-V, and 15-V parametric ratings**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package-temperature range):** 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

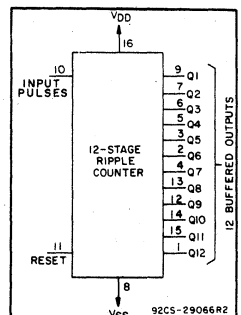
- **Control counters**
- **Timers**
- **Frequency dividers**
- **Time-delay circuits**



CD4020B FUNCTIONAL DIAGRAM



CD4024B 92CS-25051R4
FUNCTIONAL DIAGRAM



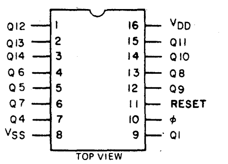
CD4040B FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, ***Absolute-Maximum Values:***

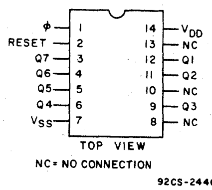
DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	–0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	–55 to +125°C
PACKAGE TYPE E	–40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	–65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

TERMINAL ASSIGNMENTS

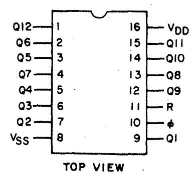
CD4020B



CD4024B



CD4040B



RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		V_{DD}	Min.	Max.	UNITS
Supply Voltage Range (at T_A = Full Package-Temperature Range)			3	18	V
Input-Pulse Frequency,	f_ϕ	5	–	3.5	MHz
		10	–	8	
		15	–	12	
Input-Pulse Width,	t_W	5	140	–	ns
		10	60	–	
		15	40	–	
Input-Pulse Rise or Fall Time,	$t_{r\phi}$, $t_{f\phi}$	5	Unlimited		μs
		10			
		15			
Reset Pulse Width,	t_W	5	200	–	ns
		10	80		
		15	60		
Reset Removal Time,	t_{REM}	5	350	–	ns
		10	150	–	
		15	100	–	

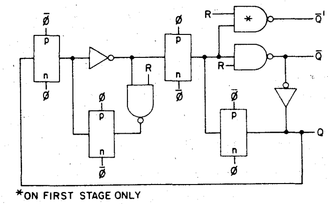


Fig. 4 – Detail of typical flip-flop stage.

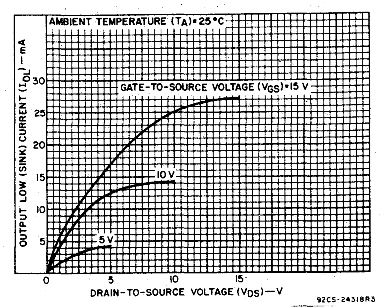


Fig. 5 – Typical output low (sink) current characteristics.

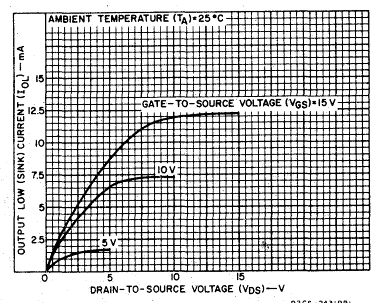


Fig. 6 – Minimum output low (sink) current characteristics.

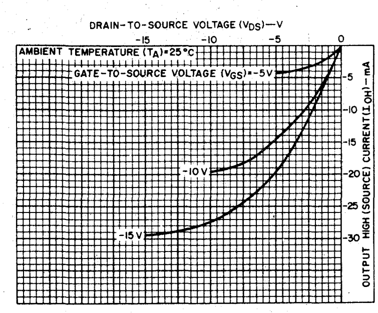


Fig. 7 – Typical output high (source) current characteristics.

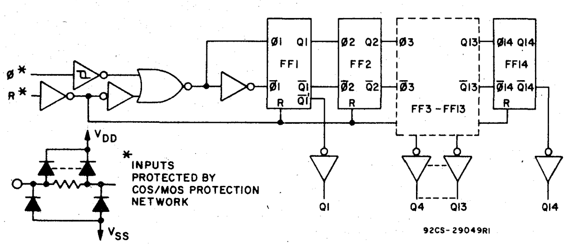


Fig. 1 – Logic diagram for CD4020B.

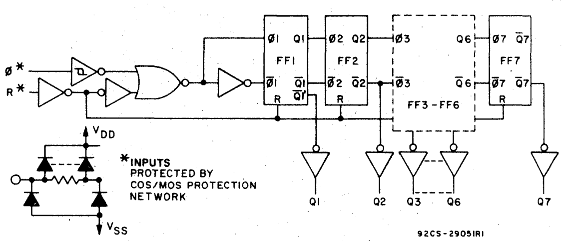


Fig. 2 – Logic diagram for CD4024B.

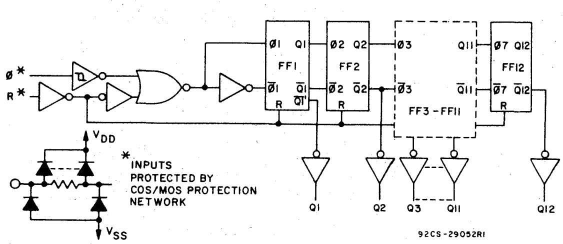


Fig. 3 – Logic diagram for CD4040B.

CD4020B, CD4024B, CD4040B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages Values at –40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

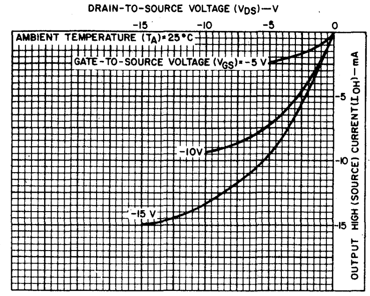


Fig. 8 – Minimum output high (source) current characteristics.

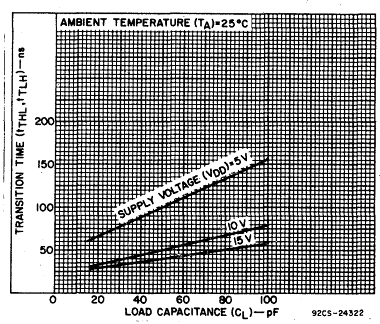
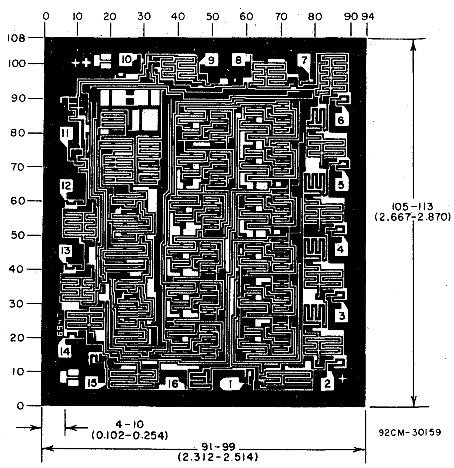
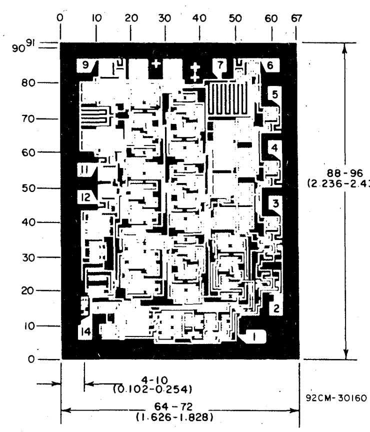


Fig. 9 – Typical transition time as a function of load capacitance.



Dimensions and Pad Layout for CD4020BH. Dimensions and pad layout for CD4040BH are identical.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).



Dimensions and Pad Layout for CD4024BH.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Input-Pulse Operation						
Propagation Delay Time, ϕ to Q_1 Out; t_{PHL}, t_{PLH}		5	–	180	360	ns
		10	–	80	160	
		15	–	65	130	
Q_n to $Q_n + 1$; t_{PHL}, t_{PLH}		5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
Transition Time, t_{THL}, t_{TLH}		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Minimum Input-Pulse Width, t_W		5	–	70	140	ns
		10	–	30	60	
		15	–	20	40	
Input-Pulse Rise or Fall Time, $t_{r\phi}$, $t_{f\phi}$		5	Unlimited			μs
		10				
		15				
Maximum Input-Pulse Frequency, f_ϕ		5	3.5	7	–	MHz
		10	8	16	–	
		15	12	24	–	
Input Capacitance, C_I	Any Input		–	5	7.5	pF
Reset Operation						
Propagation Delay Time, t_{PHL}		5	–	140	280	ns
		10	–	60	120	
		15	–	50	100	
Minimum Reset Pulse Width, t_W		5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
Reset Removal Time, t_{REM}		5	–	175	350	ns
		10	–	75	150	
		15	–	50	100	

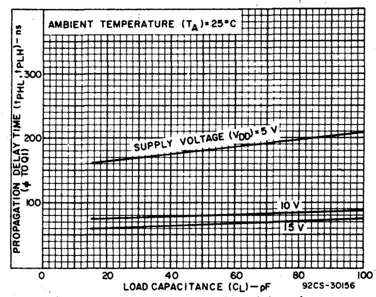


Fig. 10 – Typical propagation delay time as a function of load capacitance (ϕ to Q_1).

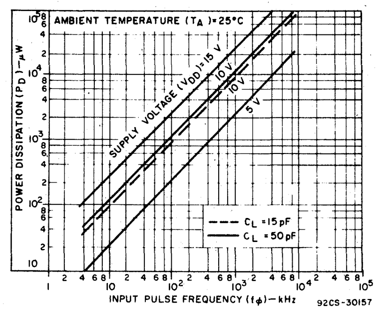


Fig. 11 – Typical dynamic power dissipation as a function of input pulse frequency for CD4020B.

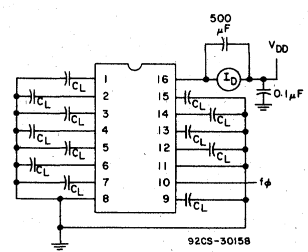


Fig. 12 – Dynamic power dissipation test circuit for CD4020B.

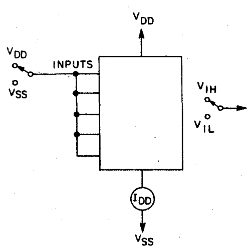


Fig. 13 – Quiescent device current test circuit.

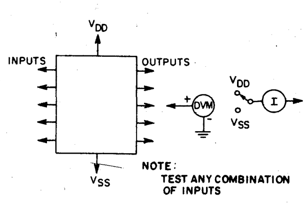


Fig. 14 – Input voltage test circuits.

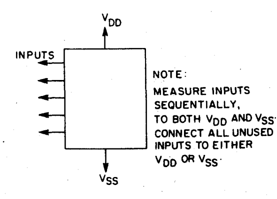


Fig. 15 – Input current test circuit.

CD4026B, CD4033B Types

COS/MOS Decade Counters/Dividers

High-Voltage Types (20-Volt Rating)
With Decoded 7-Segment Display Outputs and:
Display Enable – CD4026B
Ripple Blanking – CD4033B

The RCA-CD4026B and CD4033B each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving one stage in a numerical display.

These devices are particularly advantageous in display applications where low power dissipation and/or low package count are important.

Inputs common to both types are CLOCK, RESET, & CLOCK INHIBIT; common outputs are CARRY OUT and the seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the CD4026B include DISPLAY ENABLE input and DISPLAY ENABLE and UNGATED "C-SEGMENT" outputs. Signals peculiar to the CD4033B are RIPPLE-BLANKING INPUT AND LAMP TEST INPUT and a RIPPLE-BLANKING OUTPUT.

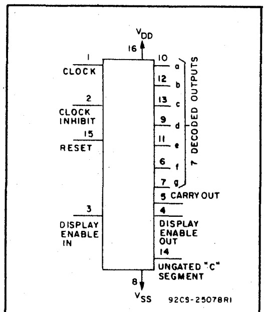
A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. The CLOCK INHIBIT signal can be used as a negative-edge clock if the clock line is held high. Antilock gating is provided on the JOHNSON counter, thus assuring proper counting sequence. The CARRY-OUT (C_{out}) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain. The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven segment display device used for representing the decimal numbers 0 to 9. The 7-segment outputs go high on selection in the CD4033B; in the CD4026B these outputs go high only when the DISPLAY ENABLE IN is high.

Features:

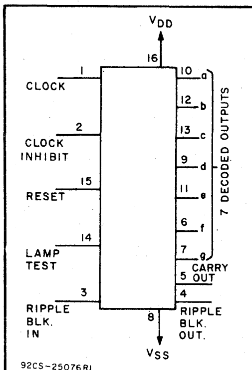
- Counter and 7-segment decoding in one package
- Easily interfaced with 7-segment display types
- Fully static counter operation: DC to 6 MHz (typ.) at V_{DD}=10 V
- Ideal for low-power displays
- Display enable output (CD4026B)
- "Ripple blanking" and lamp test (CD4033B)
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Schmitt-triggered clock inputs
- Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Decade counting 7-segment decimal display
- Frequency division 7-segment decimal displays
- Clocks, watches, timers (e.g. ÷60, ÷ 60, ÷ 12 counter/display)
- Counter/display driver for meter applications



CD4026B FUNCTIONAL DIAGRAM



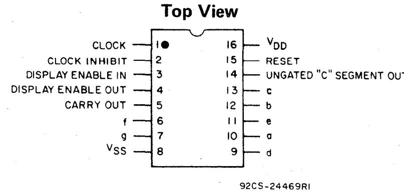
CD4033B FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltages referenced to V_{SS} Terminal)	–0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	–55 to +125°C
PACKAGE TYPE E	–40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	–65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

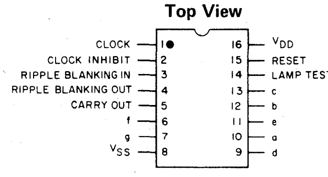
TERMINAL DIAGRAMS

Top View



CD4026B

Top View



CD4033B

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package Temperature Range)		3	18	V
Clock Input Frequency, f_{CL}	5	–	2.5	MHz
	10	–	5.5	
	15	–	8	
Clock Pulse Width, t_{WCL}	5	220	–	ns
	10	100	–	
	15	80	–	
Clock Rise and Fall Time, t_{rCL}, t_{fCL}	5	–	Unlimited	
	10	–		
	15	–		
Clock Inhibit Set Up Time, t_{SU}	5	200	–	
	10	50	–	
	15	30	–	
Reset Pulse Width, t_W	5	200	–	
	10	100	–	
	15	50	–	
Reset Removal Time	5	30	–	
	10	15	–	
	15	10	–	

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages Values at –40, +25, +85 Apply to E Package: –55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	µA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	-	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	µA

CD4026B

When the DISPLAY ENABLE IN is low the seven decoded outputs are forced low regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The CARRY OUT and UNGATED "C-SEGMENT" signals are not gated by the DISPLAY ENABLE and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

CD4033B

The CD4033B has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.0700 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the CD4033B associated with the most significant digit in the display to a low-level voltage and connecting the RBO terminal of that stage to the RBI terminal of the CD4033B in the next-lower significant position in the display. This procedure is continued for each succeeding CD4033B on the integer side of the display.

On the fraction side of the display the RBI of the CD4033B associated with the least significant bit is connected to a low-level voltage and the RBO of that CD4033B is connected to the RBI terminal of the CD4033B in the next more-significant-bit position. Again, this procedure is continued for all CD4033B's on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high level voltage (instead of to the RBO of the next more-significant-stage). For example: optional zero → 0.7346. Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the CD4033B associated with it to a high-level voltage.

Ripple blanking of non-significant zeros provides an appreciable savings in display power.

The CD4033B has a LAMP TEST input which, when connected to a high-level voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the high state.

The CD4026B- and CD4033B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

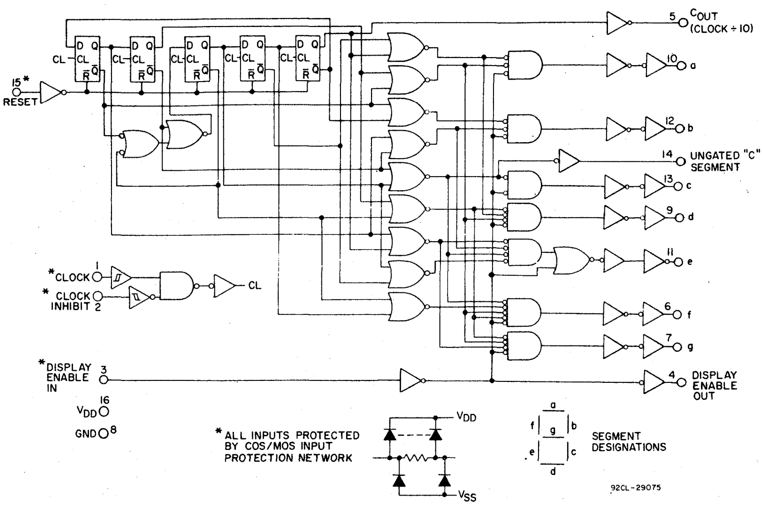


Fig. 1 – CD4026B logic diagram.

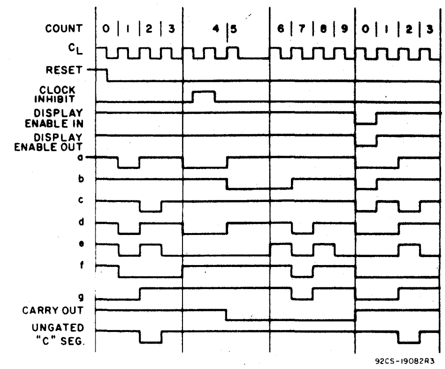


Fig. 3 – CD4026B timing diagram.

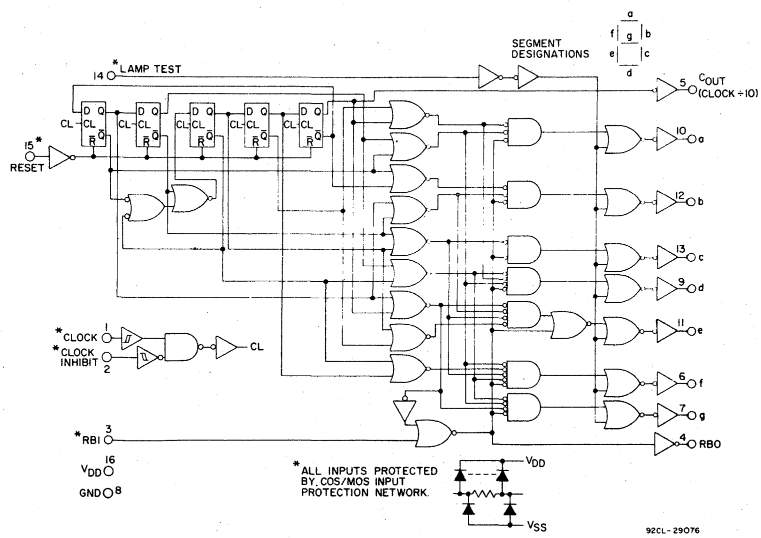


Fig. 2 – CD4033B logic diagram.

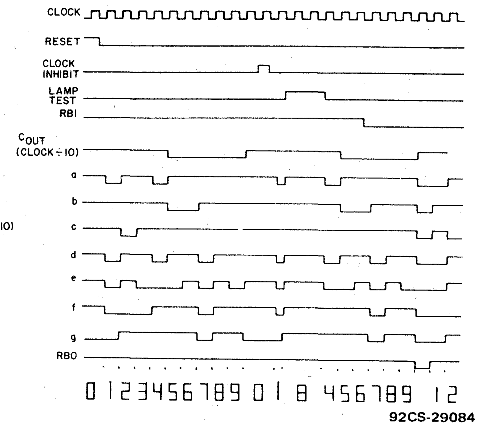


Fig. 4 – CD4033B timing diagram.

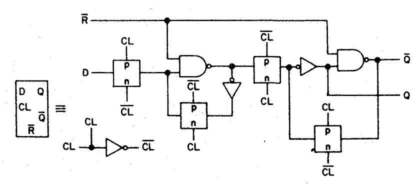


Fig. 5 – Detail of typical flip-flop stage for both types.

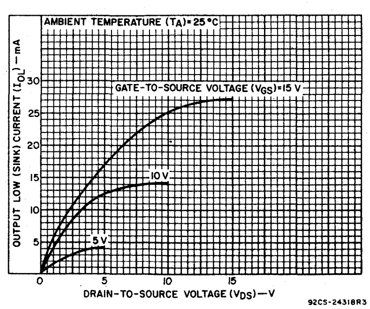


Fig. 6 – Typical n-channel output low (sink) current characteristics.

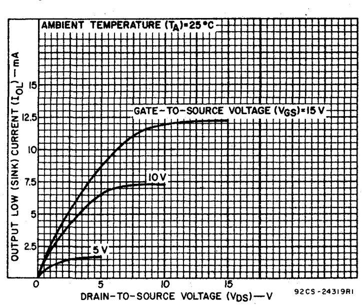


Fig. 7 – Minimum n-channel output low (sink) current characteristics.

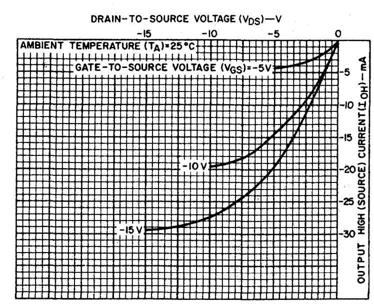


Fig. 8 – Typical p-channel output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25°C$, Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ*

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
CLOCKED OPERATION						
Propagation Delay Time; t_{PLH}, t_{PHL} Carry-Out Line		5	–	250	500	ns
		10	–	100	200	
		15	–	75	150	
Decode Outlines		5	–	350	700	
		10	–	125	250	
		15	–	90	180	
Transition Time; t_{THL}, t_{TLH} Carry-Out Line		5	–	100	200	
		10	–	50	100	
		15	–	25	50	
Maximum Clock Input Frequency, f_{CL}▲		5	2.5	5	–	MHz
		10	5.5	11	–	
		15	8	16	–	
Min. Clock Pulse Width, t_W		5	–	110	220	ns
		10	–	50	100	
		15	–	40	80	
Clock and Clock Inhibit Rise or Fall Time; t_{rCL}, t_{fCL}		5	Unlimited			
		10				
		15				
Average Input Capacitance, C_{IN}	Any Input		–	5	7	pF
RESET OPERATION						
Propagation Delay Time; To Carry-Out Line, t_{PLH}		5	–	275	550	ns
		10	–	120	240	
		15	–	80	160	
To Decode Out Lines, t_{PHL}, t_{PLH}		5	–	300	600	
		10	–	125	250	
		15	–	90	180	
Min. Reset Pulse Width, t_W		5	–	100	120	
		10	–	50	100	
		15	–	25	50	
Min. Reset Removal Time		5	–	0	30	
		10	–	0	15	
		15	–	0	10	

▲ Measured with respect to carry-out line.

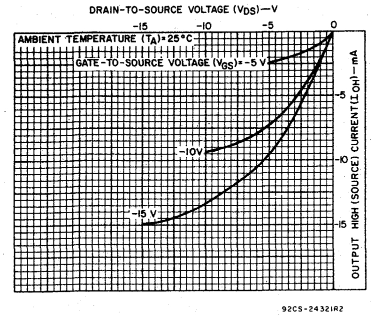


Fig. 9 – Minimum p-channel output high (source) current characteristics.

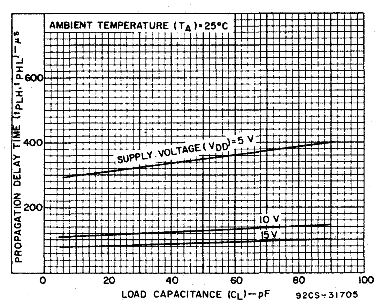


Fig. 10 – Typical propagation delay time as a function of load capacitance for decoded outputs.

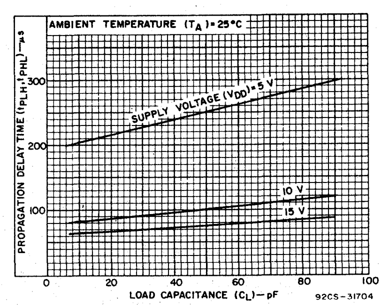


Fig. 11 – Typical propagation delay time as a function of load capacitance for carry-out outputs.

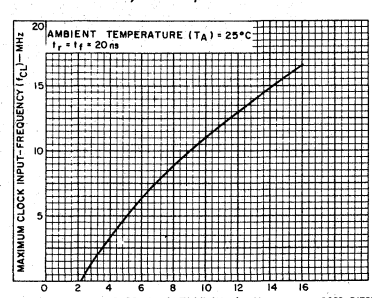


Fig. 12 – Typical maximum clock input-frequency as a function of supply voltage.

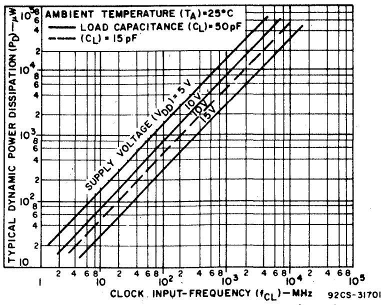


Fig. 13 – Typical power dissipation as a function of clock input frequency.

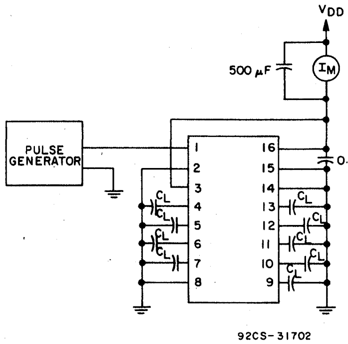


Fig. 14 – Dynamic power dissipation test circuit for CD4033B.

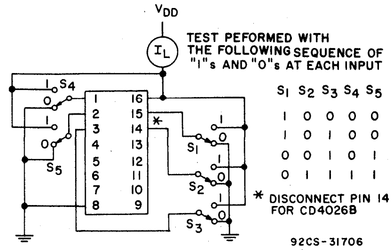


Fig. 15 – Quiescent device current.

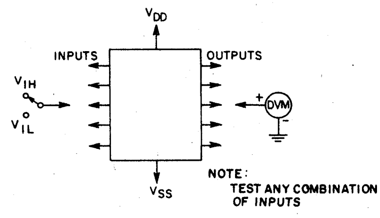
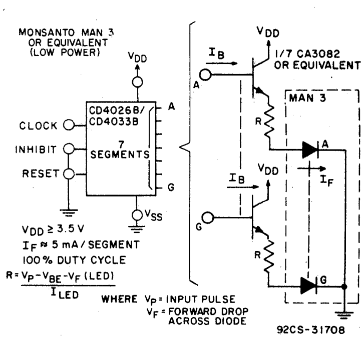
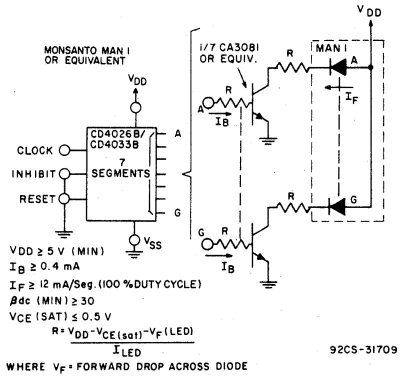


Fig. 16 – Input voltage.

INTERFACING THE CD4026B AND CD4033B WITH COMMERCIALLY AVAILABLE LIGHT EMITTING DIODE DISPLAYS





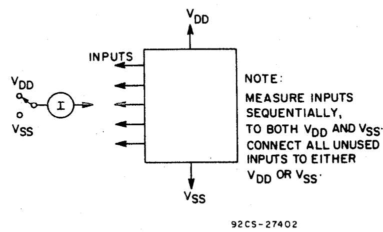
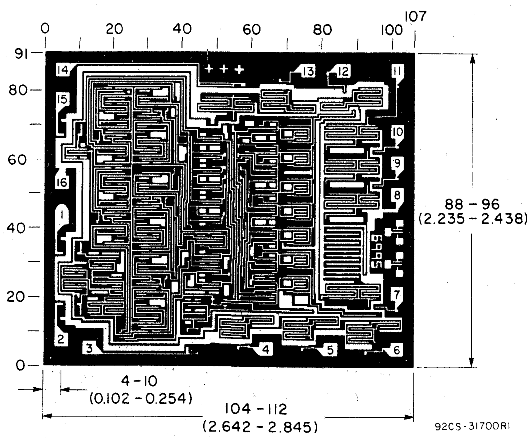
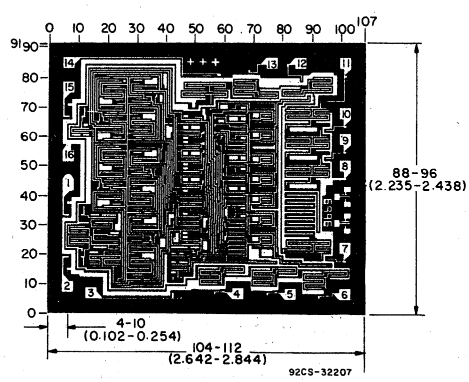


Fig. 17 – Input current.



Dimensions and pad layout for CD4026B.



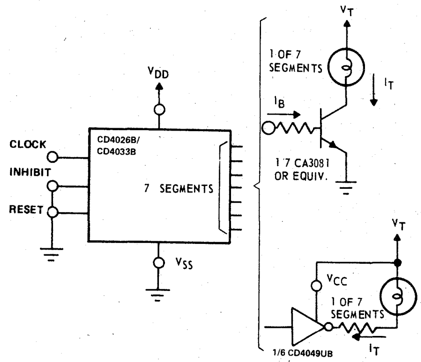
Dimensions and pad layout for CD4033B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

INTERFACING THE CD4026B AND CD4033B WITH COMMERCIALLY AVAILABLE 7-SEGMENT DISPLAY DEVICES*

(Refer to RCA Application Note ICAN-6733 for detailed interfacing information)



INCANDESCENT READOUTS

RCA Numitron- DR2000 Series

TUBE REQUIREMENTS:

V_T = 3.5 – 5 V

I_T = 24 mA Segment

ASSUMED TRANSISTOR CHARACTERISTICS

βdc (min.) ≥ 25

V_{CE}(sat.) ≤ 0.5 V

@ V_{DD} = 8 V (min.)

I_B = 1 mA (min.)

I_T = 24 mA (min.)

CD4049UB

@ V_{CC} = 10 V (min.)

V_o "0" ≤ 2 V

I_T = 8 mA (min.)

$V_T \approx$ 3.5 V TO 6 V

CD4049UB

@ V_{CC} = 10 V (min.)

V_o "0" ≤ 0.6 V

I_T = 8 mA (min.)

@ V_{CC} = 6 V (min.)

V_o "0" ≤ 1 V

I_T = 5 mA (min.)

$V_T \approx$ 1.5 V TO 3.5 V

LOW-POWER INCANDESCENT READOUTS

PINLITES INC– Series O and R

TUBE REQUIREMENTS:	V_T (V)	mA Segment
O-03-15	1.5	8
O-04-30	3	8
O-06-30	3	8
R-R3-20	2	4.3
R-R4-30	3	4.3

ASSUMED TRANSISTOR CHARACTERISTICS

βdc (min.) ≥ 30

V_{CE}(sat.) ≤ 0.5 V

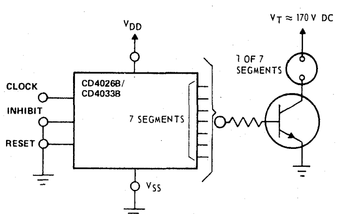
@ V_{CC} ≥ 3.5 V (min.)

I_B ≥ 0.25 mA (min.)

I_T ≤ 7.5 mA (min.)

92CM-31707

* The interfacing buffers shown, while a necessity with the CD4026A and CD4033A, are not required when using the "B" devices; the "B" outputs (≈ 10 times the "A" outputs) can drive most display devices directly especially at voltages above 10 V.



NEON READOUT (NIXIE TUBE▲)

1. Alco Electronics – MG19
2. Burroughs – B5971, B7971, B8971

TUBE REQUIREMENTS	V_T(Vdc)	mA Segment
Alco MG19	180	0.5
Burroughs B5971	170	3
Burroughs B7971, B8971 .	170	6

▲ (Trademark) Burroughs Corp.

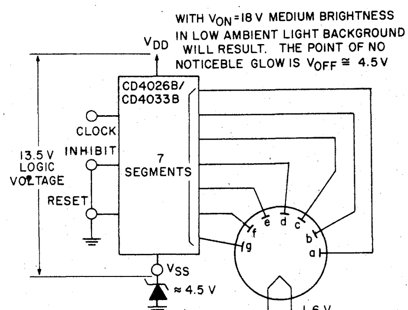
TRANSISTOR CHARACTERISTICS

Leakage with transistor cutoff – 0.05 mA

$V_{(BR)CER}$ . . . . . > V_T

β_{dc} (min.) ≥ 30

92CS-31710



LOW VOLTAGE VACUUM FLUORESCENT READOUTS

1. Tung-Sol DIGIVAC S/G ‡ Type DT1704A or DT1705C
2. Nippon Electric (NEC); Type DG12E or LD915

TUBE REQUIREMENTS: 100 to 300 μA/segment at tube voltages of 12 V to 25 V depending on required brightness Filament requirement 45 mA at 1.6 V, ac or dc.

‡ (Trademark) Wagner Electric Co.

92CS-31711

COS/MOS Dual J-K Master-Slave Flip-Flop

High-Voltage Types (20-Volt Rating)

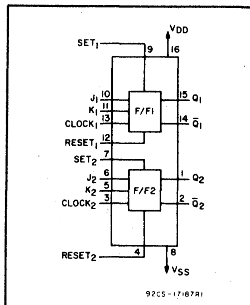
The RCA-CD4027B is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset, and Clock input signals. Buffered Q and $\overline{Q}$ signals are provided as outputs. This input-output arrangement provides for compatible operation with the RCA-CD4013B dual D-type flip-flop.

The CD4027B is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

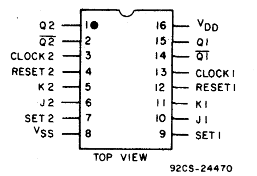
The CD4027B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:
- Set-Reset capability
- Static flip-flop operation – retains state indefinitely with clock level either "high" or "low"
- Medium speed operation – 16 MHz (typ.) clock toggle rate at 10 V
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:
- Registers, counters, control circuits



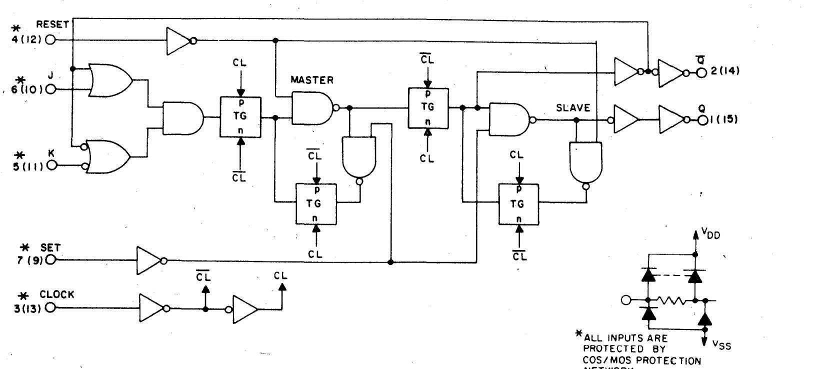
Functional Diagram



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . −55 to +125°C
PACKAGE TYPE E . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . +265°C



PRESENT STATE					CL▲	NEXT STATE		
INPUTS				OUTPUT		OUTPUTS		
J	K	S	R	Q		Q	$\overline{Q}$	
1	X	0	0	0	↗	1	0	
X	0	0	0	1	↗	1	0	
0	X	0	0	0	↗	0	1	
X	1	0	0	1	↗	0	1	
X	X	0	0	X	↘			← NO CHANGE
X	X	1	0	X	X	1	0	
X	X	0	1	X	X	0	1	
X	X	1	1	X	X	1	1	

LOGIC 1 = HIGH LEVEL
LOGIC 0 = LOW LEVEL
▲ LEVEL CHANGE
X DON'T CARE

92CM-27551R1

Fig. 1 – Logic diagram and truth table for CD4027B (one of two identical J-K flip flops).

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		V_{DD} (V)	LIMITS All Packages Min.	LIMITS All Packages Max.	UNITS
Supply-Voltage Range (For T_A = Full Package Temperature Range)		–	3	18	V
Data Setup Time	t_S	5	200	–	ns
		10	75	–	
		15	50	–	
Clock Pulse Width	t_W	5	140	–	ns
		10	60	–	
		15	40	–	
Clock Input Frequency (Toggle Mode)	f_{CL}	5	dc	3.5	MHz
		10		8	
		15		12	
Clock Rise or Fall Time	t_rCL*, t_fCL	5	–	15	μs
		10	–	4	
		15	–	1	
Set or Reset Pulse Width	t_W	5	180	–	ns
		10	80	–	
		15	50	–	

* If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

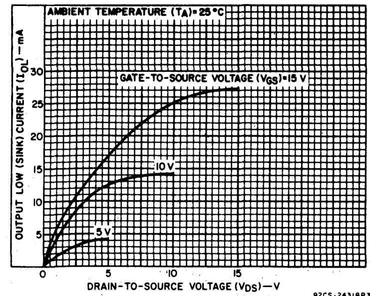


Fig.2 – Typical output low (sink) current characteristics.

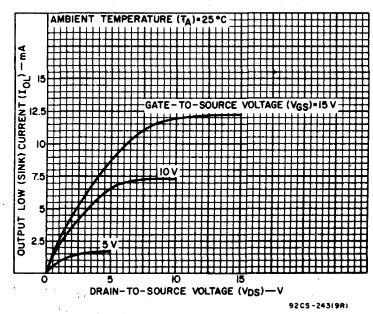


Fig.3 – Minimum output low (sink) current characteristics.

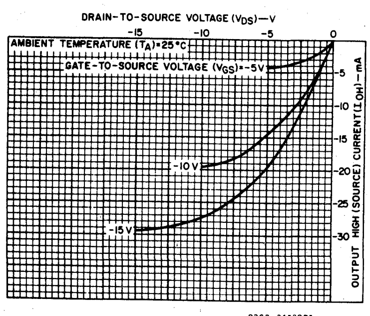


Fig.4 – Typical output high (source) current characteristics.

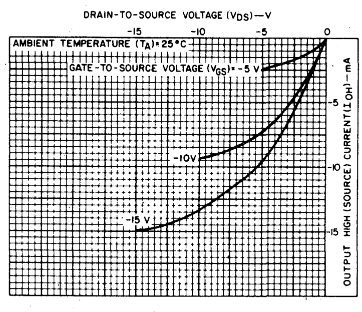


Fig.5 – Minimum output high (source) current characteristics.

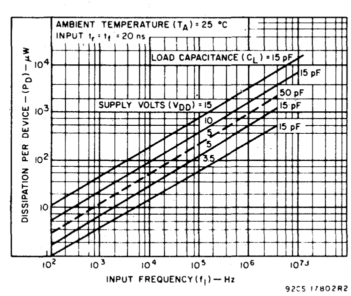


Fig.6 – Typical power dissipation vs. frequency.

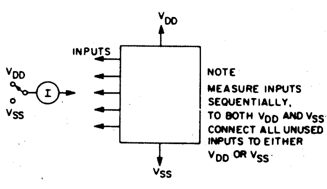


Fig.7 – Input current test circuit.

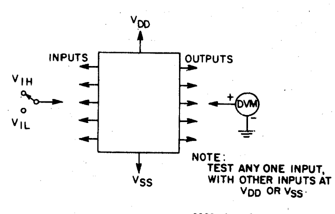


Fig.8 – Input-voltage test circuit.

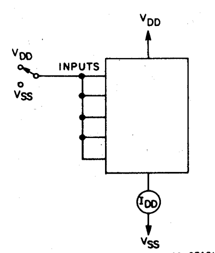
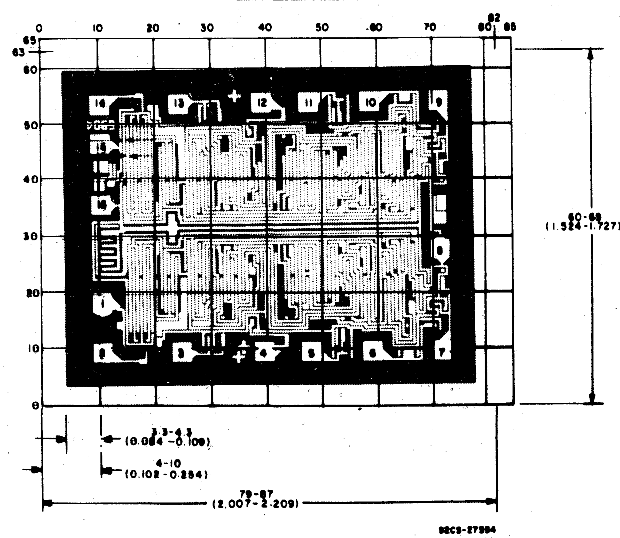


Fig.9 – Quiescent device current test circuit.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55,+25,+125 Apply to D,F,H Pkgs. Values at –40,+25,+85 Apply to E Pkgs.							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA



Dimensions in millimeters are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3}).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and Pad Layout for CD4027BH

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS All Packages Min.	Typ.	Max.	UNITS
Propagation Delay Time: Clock to Q or $\bar{Q}$ Outputs t_{PHL}, t_{PLH}	5	–	150	300	ns
	10	–	65	130	
	15	–	45	90	
Set to Q or Reset to $\bar{Q}$ t_{PLH}	5	–	150	300	ns
	10	–	65	130	
	15	–	45	90	
Set to $\bar{Q}$ or Reset to Q t_{PHL}	5	–	200	400	ns
	10	–	85	170	
	15	–	60	120	
Transition Time t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Maximum Clock Input Frequency# (Toggle Mode) f_{CL}	5	3.5	7	–	MHz
	10	8	16	–	
	15	12	24	–	
Minimum Clock Pulse Width t_W	5	–	70	140	ns
	10	–	30	60	
	15	–	20	40	
Minimum Set or Reset Pulse Width t_W	5	–	90	180	ns
	10	–	40	80	
	15	–	25	50	
Minimum Data Setup Time t_S	5	–	100	200	ns
	10	–	35	75	
	15	–	25	50	
Clock Input Rise or Fall Time t_{rCL}, t_{fCL}	5	–	–	15	µs
	10	–	–	4	
	15	–	–	1	
Input Capacitance C_I		–	5	7.5	pF

Input t_r, t_f = 5 ns.

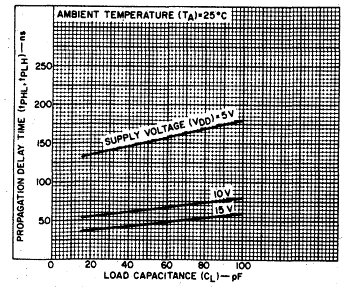


Fig.10 – Typical propagation delay time vs. load capacitance (CLOCK or SET to Q, CLOCK or RESET to $\bar{Q}$.

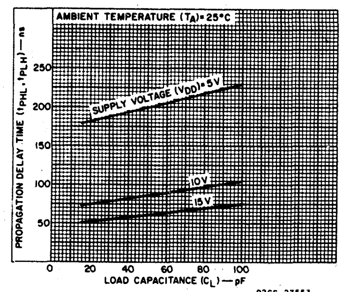


Fig.11 – Typical propagation delay time vs. load capacitance (SET to $\bar{Q}$ or RESET to Q).

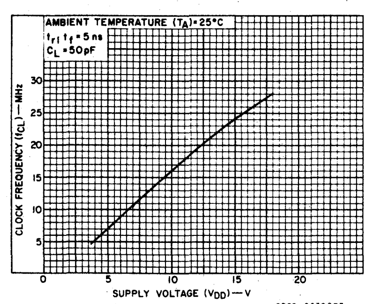


Fig.12– Typical maximum clock frequency vs. supply voltage (toggle mode).

CD4028B Types

COS/MOS BCD-to-Decimal Decoder

High-Voltage Types (20-Volt Rating)

The RCA-CD4028B types are BCD-to-decimal or binary-to-octal decoders consisting of buffering on all 4 inputs, decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7 if D = "0". High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

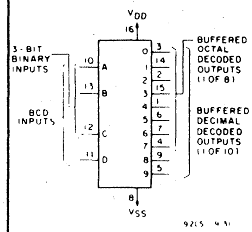
The CD4028B-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

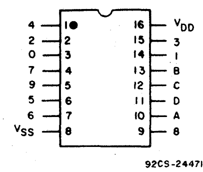
- BCD-to-decimal decoding or binary-to-octal decoding
- High decoded output drive capability
- "Positive logic" inputs and outputs.... ..... decoded outputs go high on selection
- Medium-speed operation.... t_{PHL}, t_{PLH} = 80 ns (typ.) @ V_{DD} = 10 V
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
  - 1 V at V_{DD} = 5 V
  - 2 V at V_{DD} = 10 V
  - 2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Code conversion
- Indicator-tube decoder
- Address decoding—memory selection control



CD4028B
FUNCTIONAL DIAGRAM



Top View
TERMINAL DIAGRAM

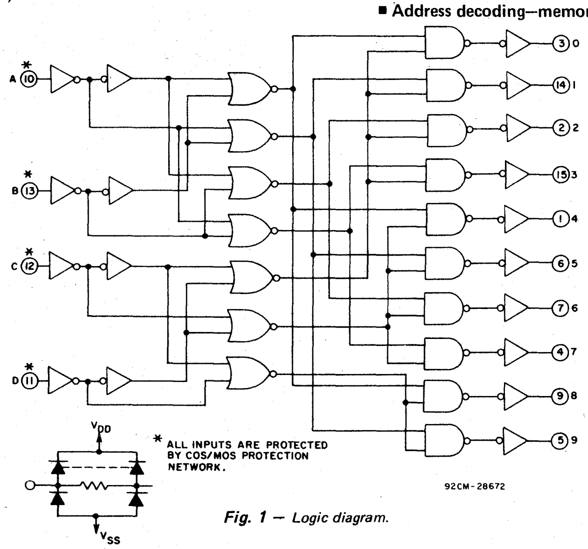


Fig. 1 — Logic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F,) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . . +265°C

TABLE I – TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

1 = HIGH LEVEL   0 = LOW LEVEL

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $C_L = 50$ pF, Input $t_r, t_f = 20$ ns, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
	V_{DD} (V)	Typ.	Max.	
Propagation Delay Time: t_{PHL}, t_{PLH}	5	175	350	ns
	10	80	160	
	15	60	120	
Transition Time t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN}	–	5	7.5	pF

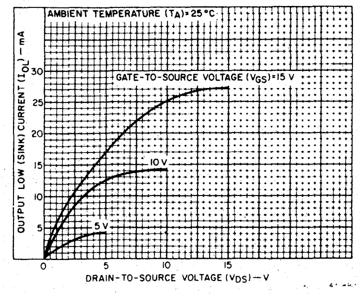


Fig. 2 — Typical output low (sink) current characteristics.

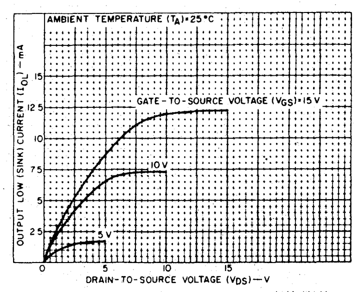


Fig. 3 — Minimum output low (sink) current characteristics.

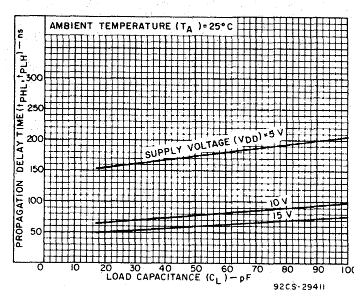


Fig. 4 — Typical propagation delay time as a function of load capacitance.

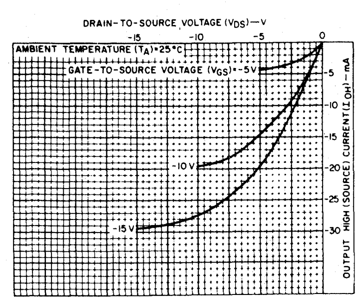


Fig. 5 — Typical output high (source) current characteristics.

TABLE II – CODE CONVERSION CHART

INPUTS				INPUT CODES: Hexa-Decimal		Decimal				OUTPUT NUMBER															
D	C	B	A	4-BIT BINARY	4-BIT GRAY	EXCESS-3	EXCESS-3 GRAY	AIKEN	4-2-2-1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0			0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1			1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	2	3		0	2	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	3	2	0	3	3		0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	4	7	1	4	4		0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	5	6	2			3	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	6	4	3	1		4	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	7	5	4	2			0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	8	15	5				0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	9	14	6			5	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	10	12	7	9		6	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	11	13	8		5		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	12	8	9	5	6		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	13	9		6	7	7	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	14	11		8	8	8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	15	10		7	9	9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

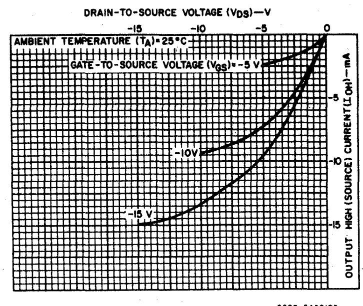


Fig. 6 — Minimum output high (source) current characteristics.

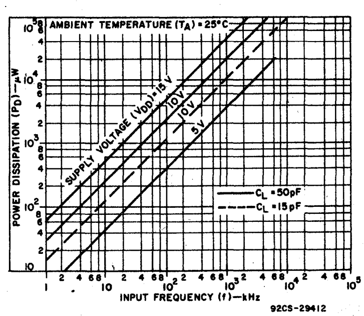


Fig. 7 — Typical dynamic power dissipation as a function of input frequency.

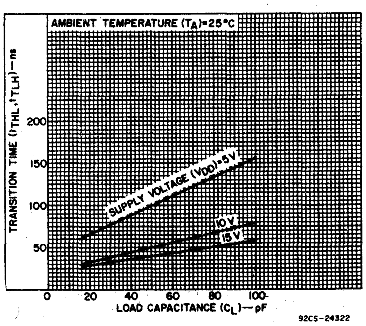


Fig. 8 — Typical transition time as a function of load capacitance.

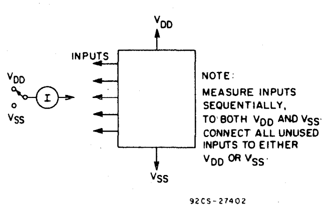


Fig. 9 — Input current test circuit.

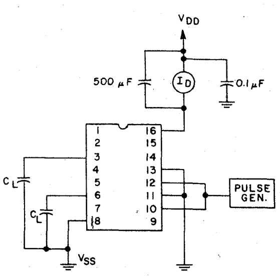


Fig. 10 — Dynamic power dissipation test circuit.

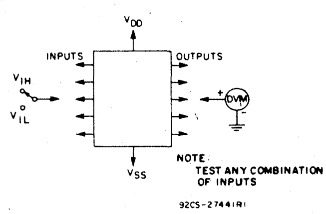


Fig. 11 — Input voltage test circuit.

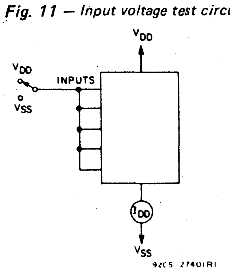


Fig. 12 — Quiescent device current test circuit.

TYPICAL APPLICATIONS

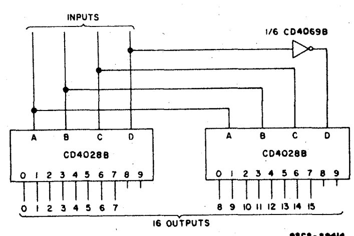
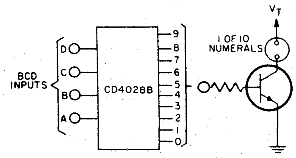


Fig. 13 — Code conversion circuit.

The circuit shown in Fig.13 converts any 4-bit code to a decimal or hexadecimal code. Table 2 shows a number of codes and the decimal or hexadecimal number in these codes which must be applied to the input terminals of the CD4028B to select a particular output. For example: in order to get a high on output No. 8 the input must be either an 8 expressed in 4-Bit Binary code, a 15 expressed in 4-Bit Gray code, or a 5 expressed in Excess-3 code.



TUBE REQUIREMENTS

Type		V_T (Vdc)	mA/numeral
Burroughs	B4081	170	1 4
	B4336/718	170	2
	B4032	170	1 4
	B4021	120	1 4

TRANSISTOR CHARACTERISTICS

Leakage with transistor cutoff ≤ 0.05mA

$V_{(BR)CEO}$ ≤ 70V

92CS-29413

▲(Trademark) Burroughs Corp.

Fig. 14 — Neon readout (Nixie Tube▲) display application.

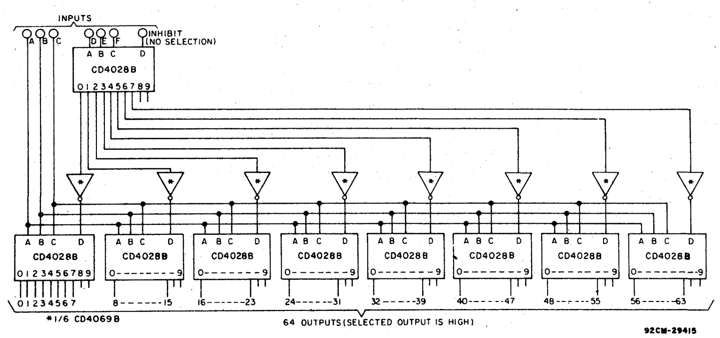
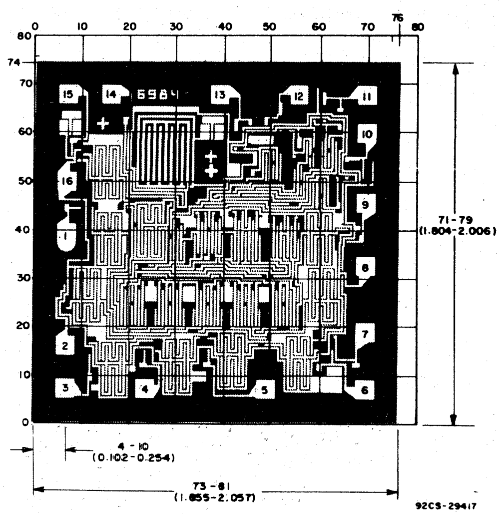


Fig. 15 — 6-bit binary to 1-of-64 address decoder.



CD4028BH

DIMENSIONS AND PAD LAYOUT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4029B Types

COS/MOS Presettable Up/Down Counter

Binary or BCD-Decade

High-Voltage Types (20-Volt Rating)

The RCA-CD4029B consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single CLOCK, $\overline{\text{CARRY-IN}}$ ($\overline{\text{CLOCK ENABLE}}$), BINARY/DECADE, UP/DOWN, PRESET ENABLE, and four individual JAM signals. Q1, Q2, Q3, Q4 and a $\overline{\text{CARRY OUT}}$ signal are provided as outputs.

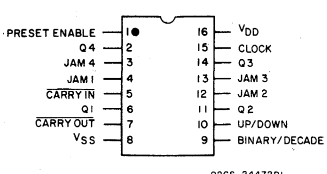
A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET-ENABLE signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the $\overline{\text{CARRY-IN}}$ and PRESET ENABLE signals are low. Advancement is inhibited when the $\overline{\text{CARRY-IN}}$ or PRESET ENABLE signals are high. The $\overline{\text{CARRY-OUT}}$ signal is normally high and goes low when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the $\overline{\text{CARRY-IN}}$ signal is low. The $\overline{\text{CARRY-IN}}$ signal in the low state can thus be considered a $\overline{\text{CLOCK ENABLE}}$. The $\overline{\text{CARRY-IN}}$ terminal must be connected to V_{SS} when not in use.

Binary counting is accomplished when the BINARY/DECADE input is high; the counter counts in the decade mode when the BINARY/DECADE input is low. The counter counts up when the UP/DOWN input is high, and down when the UP/DOWN input is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement as shown in Fig. 17.

Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

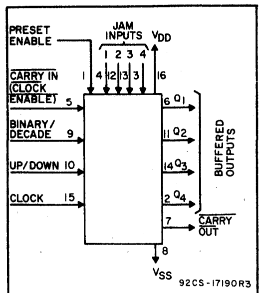
The CD4029B-series types are supplied in 16-lead ceramic dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

CD4029B Terminal Diagram



Features:
- **Medium-speed operation . . . 8 MHz (typ.) @ C_L = 50 pF and $V_{DD}-V_{SS}$ = 10 V**
- **Multi-package parallel clocking for synchronous high speed output response or ripple clocking for slow clock input rise and fall times**
- **"Preset Enable" and individual "Jam" inputs provided**
- **Binary or decade up/down counting**
- **BCD outputs in decade mode**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package-temperature range)**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:
- **Programmable binary and decade counting/frequency synthesizers-BCD output**
- **Analog to digital and digital to analog conversion**
- **Up/Down binary counting**
- **Magnitude and sign generation**
- **Up/Down decade counting**
- **Difference counting**



CD4029B FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	–	3	18	V
Setup Time t_{SU}: Carry-In	5	60	–	ns
	10	20	–	
	15	12	–	
U/D or B/D	5	340	–	
	10	140	–	
	15	100	–	
Clock Pulse Width, t_W	5	180	–	
	10	90	–	
	15	60	–	
Preset Enable Pulse Width, t_W	5	130	–	
	10	70	–	
	15	50	–	
Clock Input Frequency, f_{CL}	5	–	2	MHz
	10	–	4	
	15	–	5.5	
Clock Rise and Fall Time, t_rCL, t_fCL	5	–	15	μs
	10	–		
	15	–		

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F). . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

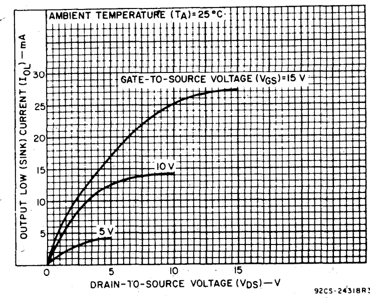


Fig. 1 — Typical output low (sink) current characteristics.

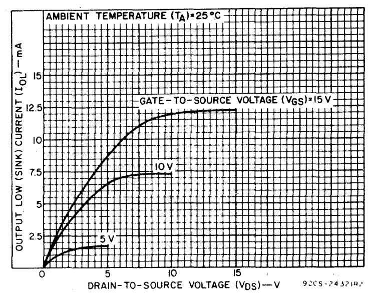


Fig. 2 — Minimum output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

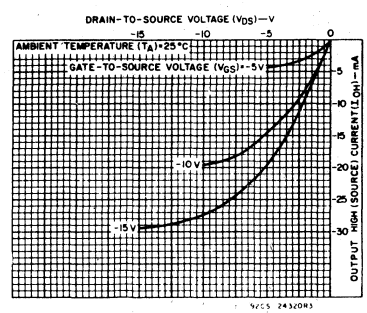


Fig. 3 — Typical output high (source) current characteristics.

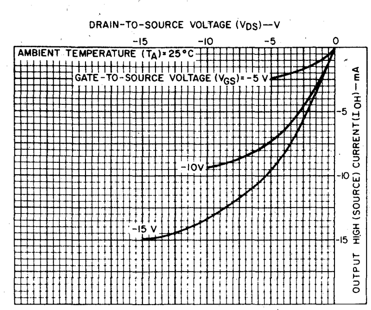


Fig. 4 — Minimum output high (source) current characteristics.

CD4029B Types

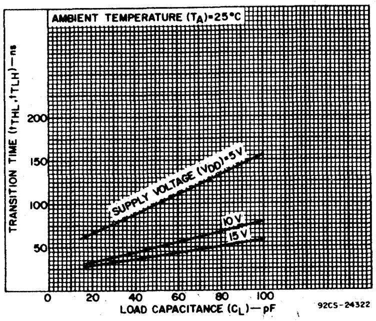


Fig. 5 – Typical transition time as a function of load capacitance.

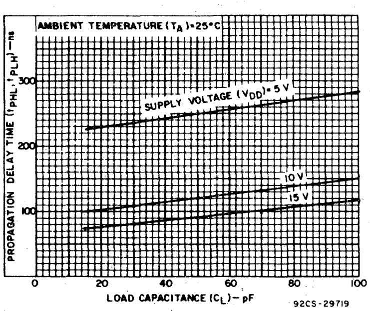


Fig. 6 – Typical propagation delay times as a function of load capacitance (Q output).

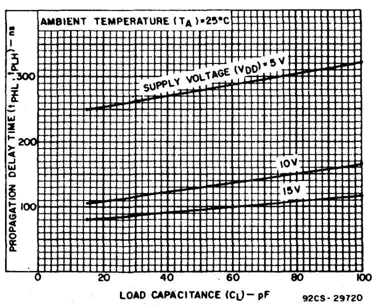


Fig. 7 – Typical propagation delay time as a function of load capacitance (carry output).

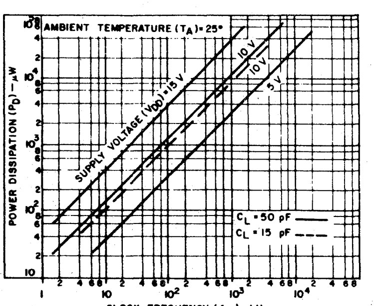
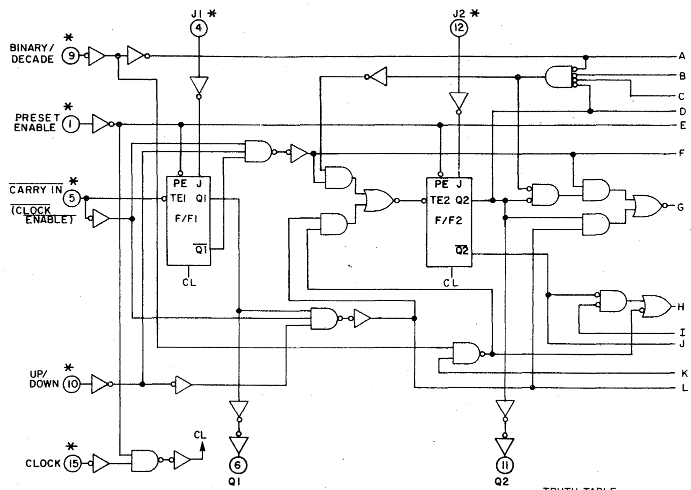
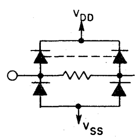


Fig. 8 – Typical power dissipation as a function of frequency.

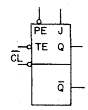




*ALL INPUTS ARE PROTECTED BY COS/MOS INPUT PROTECTION NETWORK

92CL-28675R1

TRUTH TABLE



CLOCK	TE	PE	J	Q	$\bar{Q}$
X	X	0	0	0	1
⌐L	0	1	X	$\bar{Q}$	Q
X	X	0	1	1	0
⌐L	1	1	X	Q	$\bar{Q}$ NC
⌐	X	1	X	Q	$\bar{Q}$ NC

X-DON'T CARE

Fig. 9 – Logic diagram.

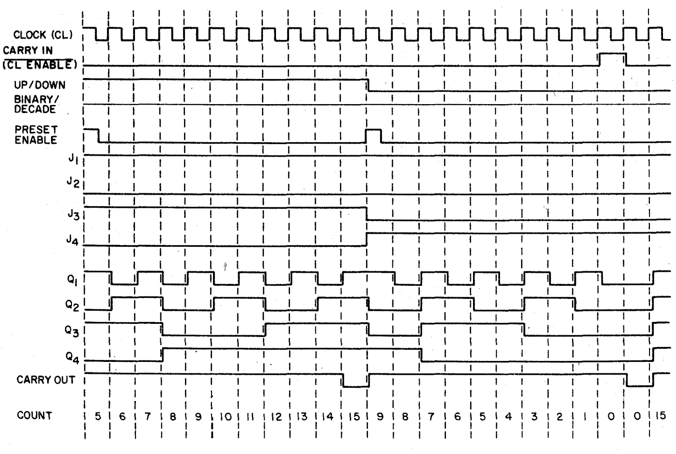
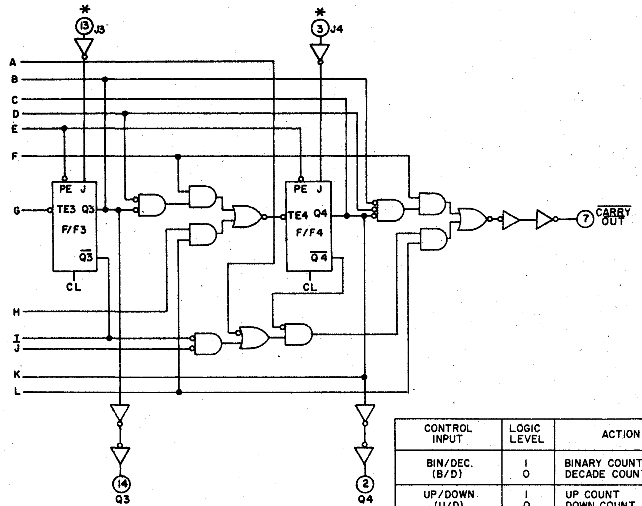


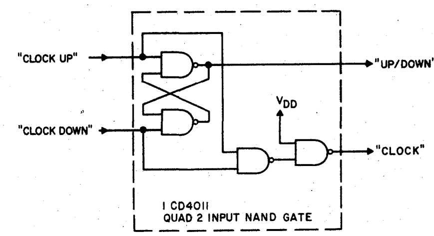
Fig. 10 – Timing diagram-binary mode.



CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC. (B/D)	1 0	BINARY COUNT DECADE COUNT
UP/DOWN (U/D)	1 0	UP COUNT DOWN COUNT
PRESET ENABLE (PE)	1 0	JAM IN NO JAM
$\overline{\text{CARRY IN}}$ ($\overline{\text{CI}}$) ($\overline{\text{CLOCK ENABLE}}$)	1 0	NO COUNTER ADVANCE AT POS. CLOCK TRANSITION ADVANCE COUNTER AT POS. CLOCK TRANSITION

92CL-28675R1

Fig. 9 – Logic diagram (cont'd).

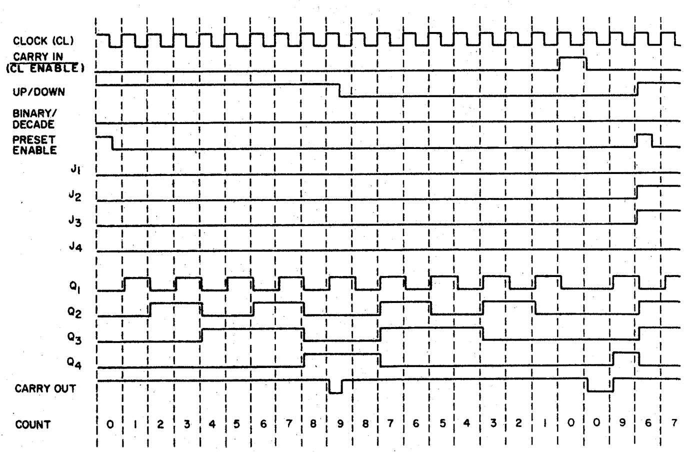


92CS-17195R2

Fig. 11 – Conversion of clock up, clock down input signals to clock and up/down input signals.

The CD4029B CLOCK and UP/DOWN inputs are used directly in most applications. In applications where CLOCK UP and CLOCK DOWN inputs are provided, conversion to the CD4029B CLOCK and UP/DOWN inputs can easily be realized by use of the circuit in Fig. 11.

CD4029B changes count on positive transitions of CLOCK UP or CLOCK DOWN inputs. For the gate configuration shown below, when counting up the CLOCK DOWN input must be maintained high and conversely when counting down the CLOCK UP input must be maintained high.



92CM-17193R3

Fig. 12 – Timing diagram-decade mode.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
Clocked Operation					
Propagation Delay Time: t_{PHL}, t_{PLH} Q Output	5	–	250	500	ns
	10	–	120	240	
	15	–	90	180	
Carry Output	5	–	280	560	
	10	–	130	260	
	15	–	95	190	
Transition Time: t_{THL}, t_{TLH} Q Outputs, Carry Output	5	–	100	200	
	10	–	50	100	
	15	–	40	80	
Minimum Clock Pulse Width, t_W	5	–	90	180	
	10	–	45	90	
	15	–	30	60	
Clock Rise & Fall Time, t_rCL, t_fCL**	5	–	–	15	μs
	10	–	–	15	
	15	–	–	15	
Minimum Setup Times, t_S* Carry In	5	–	30	60	ns
	10	–	10	20	
	15	–	6	12	
B/D or U/D	5	–	170	340	
	10	–	70	140	
	15	–	50	100	
Maximum Clock Input Frequency, f_{CL}	5	2	4	–	MHz
	10	4	8	–	
	15	5.5	11	–	
Input Capacitance, C_{IN}	Any Input	–	5	7.5	pF
Preset Enable					
Propagation Delay Time: t_{PHL}, t_{PLH} Q Outputs	5	–	235	470	ns
	10	–	100	200	
	15	–	80	160	
Carry Output	5	–	320	640	
	10	–	145	290	
	15	–	105	210	
Minimum Preset Enable Pulse Width, t_W	5	–	65	130	
	10	–	35	70	
	15	–	25	50	
Minimum Preset Enable Removal Time, t_{rem}*	5	–	100	200	
	10	–	55	110	
	15	–	40	80	
Carry Input					
Propagation Delay Time: t_{PHL}, t_{PLH} Carry Output	5	–	170	340	ns
	10	–	70	140	
	15	–	50	100	
Min Set-Up Time t_s*** Carry In	5	–	25	50	ns
	10	–	15	30	
	15	–	12	25	
Min. HOLD Time t_H*** Carry In	5	–	100	200	ns
	10	–	35	70	
	15	–	30	60	

* From Up/Down, Binary/Decode, Carry In, or Preset Enable Control Inputs to Clock Edge.

** If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load. This measurement was made with a decoupling capacitor (>1 μF) between V_{DD} and V_{SS}.

***From Carry In to Clock Edge

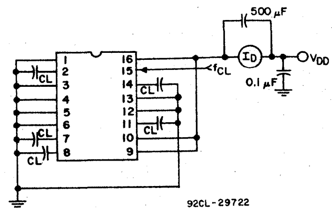


Fig. 13 – Power dissipation test circuit.

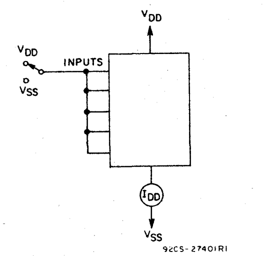


Fig. 14 – Quiescent-device current test circuit.

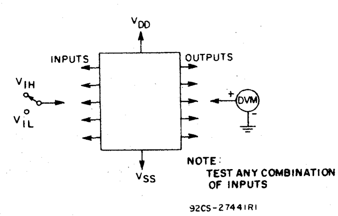


Fig. 15 – Input voltage test circuit.

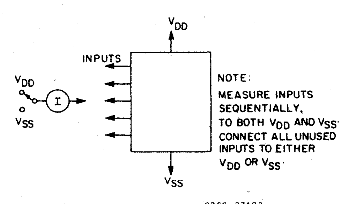
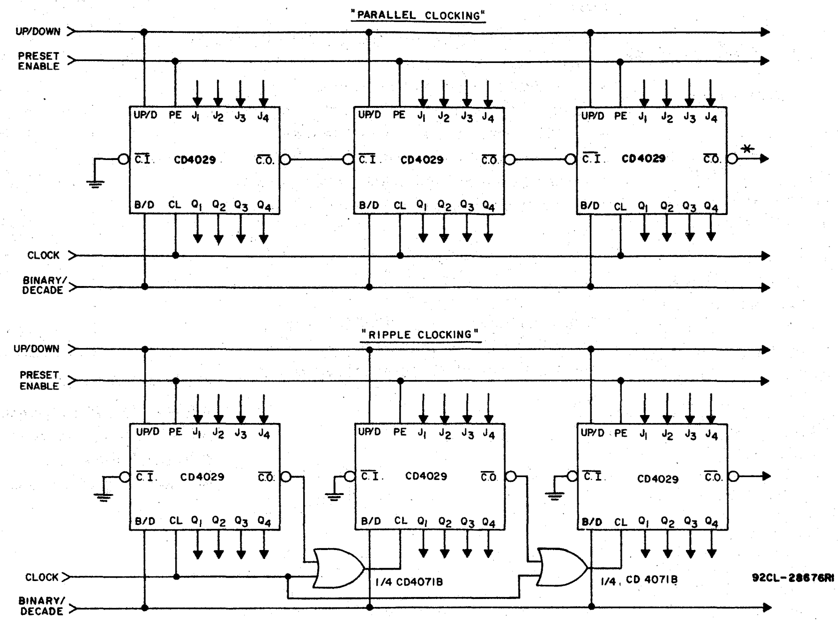


Fig. 16 – Input current test circuit.

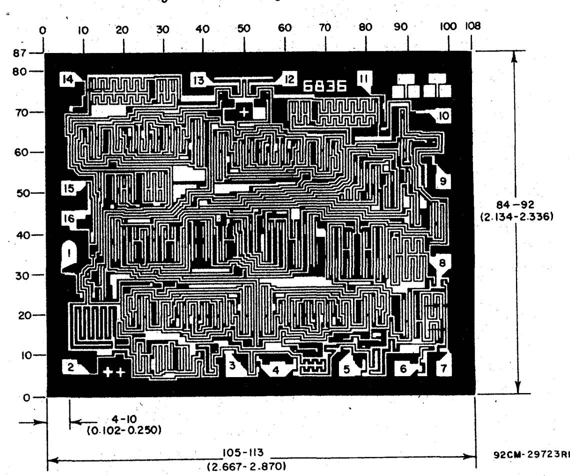


Ripple Clocking Mode:
The Up/Down control can be changed at any count. The only restriction on changing the Up/Down control is that the clock input to the first counting stage must be high.

* CARRY OUT lines at the 2nd, 3rd, etc., stages may have a negative-going glitch pulse resulting from differential delays of different CD4029B IC's. These negative-going glitches do not affect proper CD4029B operation. However, if the CARRY OUT signals are used to trigger other edge-sensitive logic devices, such as FF's or counters, the CARRY OUT signals should be gated with the clock signal using a 2-input OR gate such as CD4071B.

For cascading counters operating in a fixed up-count or down-count mode, the OR gates are not required between stages, and $\overline{CO}$ is connected directly to the CL input of the next stage with $\overline{CI}$ grounded.

Fig. 17 – Cascading counter packages.



Dimensions and pad layout for CD4029B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4030B Types

COS/MOS Quad Exclusive-OR Gate

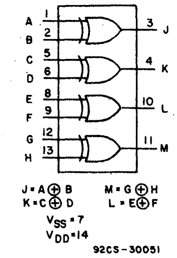
High-Voltage Types (20-Volt Rating)

The RCA-CD4030B types consist of four independent Exclusive-OR gates. The CD4030B provides the system designer with a means for direct implementation of the Exclusive-OR function.

The CD4030B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Medium-speed operation—t_{PHL}, t_{PLH} = 65 ns (typ.) at V_{DD} = 10 V, C_L = 50 pF**
- **100% tested for quiescent current at 20 V**
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package-temperature range):**
  - **1 V at V_{DD} = 5 V**
  - **2 V at V_{DD} = 10 V**
  - **2.5 V at V_{DD} = 15 V**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



CD4030B FUNCTIONAL DIAGRAM

Applications:

- **Even and odd-parity generators and checkers**
- **Logical comparators**
- **Adders/subtractors**
- **General logic functions**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

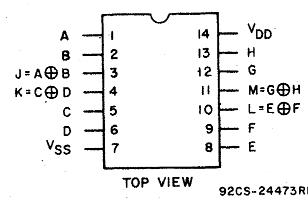
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . −55 to +125°C
PACKAGE TYPE E . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . +265°C

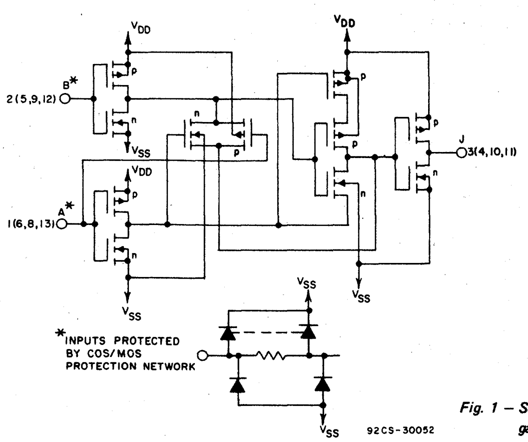
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

TERMINAL DIAGRAM
Top View





TRUTH TABLE FOR ONE OF FOUR IDENTICAL GATES

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

1 = HIGH LEVEL
0 = LOW LEVEL

Fig. 1 – Schematic diagram (1 of 4 identical gates).

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6		
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8		
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–		0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

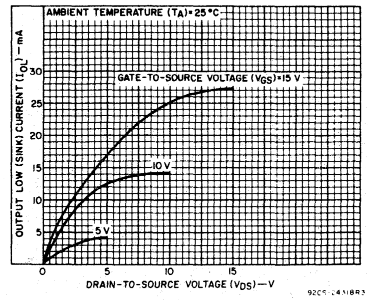


Fig. 2 – Typical output low (sink) current characteristics.

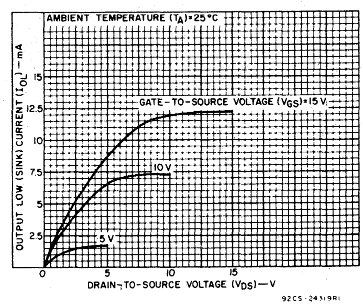


Fig. 3 – Minimum output low (sink) current characteristics.

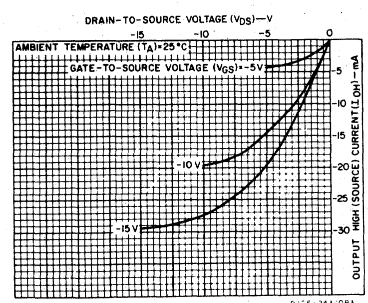


Fig. 4 – Typical output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		CONDITIONS V_{DD} (V)	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time,	t_{PLH}, t_{PHL}	5	140	280	ns
		10	65	130	
		15	50	100	
Transition Time,	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance,	C_{IN}	Any Input	5	7.5	pF

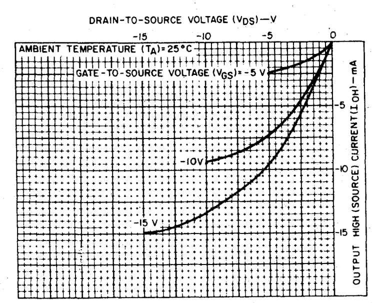


Fig. 5 – Minimum output high (source) current characteristics.

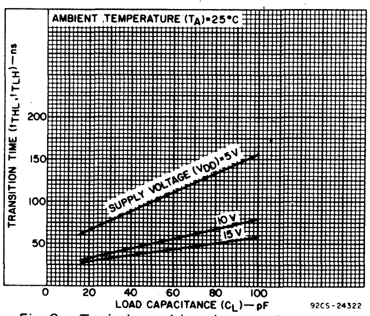


Fig. 6 – Typical transition time as a function of load capacitance.

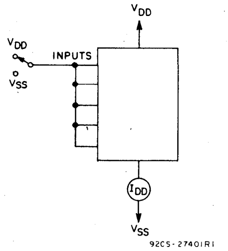


Fig. 10 – Quiescent-device current test circuit.

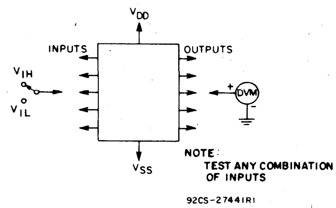


Fig. 11 – Input-voltage test circuit.

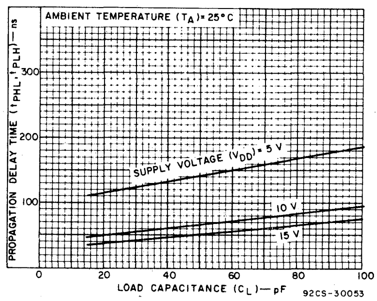


Fig. 7 – Typical propagation delay time as a function of load capacitance.

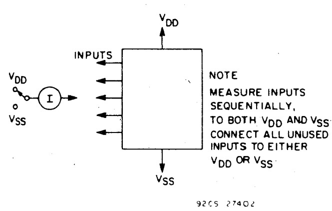


Fig. 12 – Input-current test circuit.

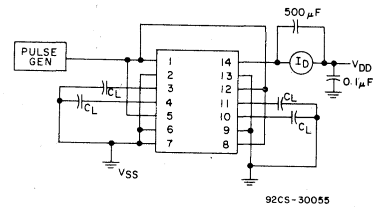


Fig. 13 – Dynamic power dissipation test circuit.

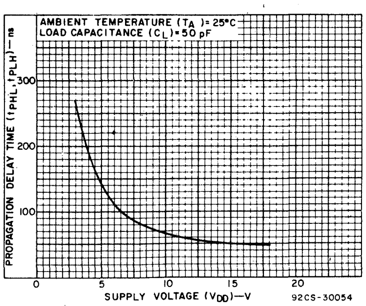


Fig. 8 – Typical propagation delay time as a function of supply voltage.

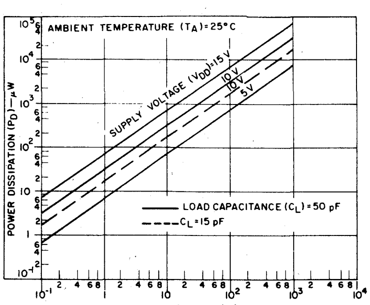
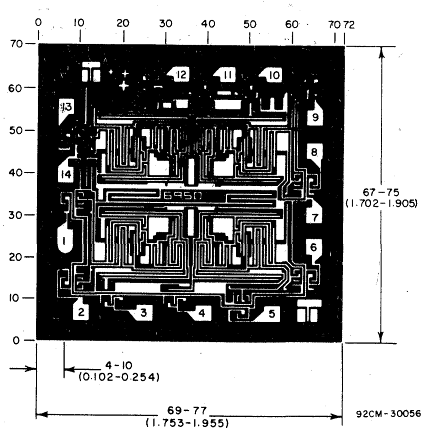


Fig. 9 – Typical dynamic power dissipation as a function of input frequency.



Dimensions and pad layout for CD4030BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS 64-Stage Static Shift Register

High-Voltage Types (20-Volt Rating)

The RCA-CD4031B is a static shift register that contains 64 D-type, master-slave flip-flop stages and one stage which is a D-type master flip-flop only (referred to as a 1/2 stage).

The logic level present at the DATA input is transferred into the first stage and shifted one stage at each positive-going clock transition. Maximum clock frequencies up to 12 Megahertz (typical) can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the low or high state. The CD4031B has a MODE CONTROL input that, when in the high state, allows operation in the recirculating mode. The MODE CONTROL input can also be used to select between two separate data sources. Register packages can be cascaded and the clock lines driven directly for high-speed operation. Alternatively, a delayed clock output (CL_D) is provided that enables cascading register packages while allowing reduced clock drive fan-out and transition-time requirements. A third cascading option makes use of the Q' output from the 1/2 stage, which is available on the next negative-going transition of the clock after the Q output occurs. This delayed output, like the delayed clock CL_D, is used with clocks having slow rise and fall times.

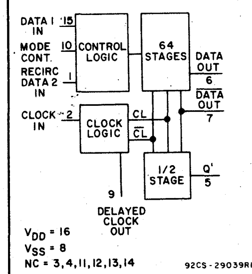
The CD4031B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead plastic dual-in-line packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Fully static operation: DC to 12 MHz typ. @ $V_{DD}-V_{SS}$ = 15 V**
- **Standard TTL drive capability on Q output**
- **Recirculation capability**
- **Three cascading modes:**
  Direct clocking for high-speed operation
  Delayed clocking for reduced clock drive requirements
  Additional 1/2 stage for slow clocks
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package-temperature range)**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Serial shift registers**
- **Time delay circuits**



FUNCTIONAL DIAGRAM

INPUT CONTROL CIRCUIT TRUTH TABLE

DATA	RECIRC.	MODE	BIT INTO STAGE I
1	X	0	1
0	X	0	0
X	1	1	1
X	0	1	0

TYPICAL STAGE TRUTH TABLE

Data	CL	Data + 1
0	↑	0
1	↑	1
X	↓	NC

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

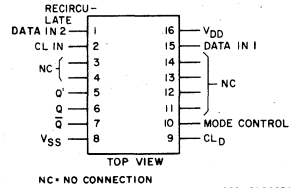
TRUTH TABLE FOR OUTPUT FROM Q' (TERMINAL 5)

Data + 64	CL	Data + 64½
0	↓	0
1	↓	1
X	↑	NC

1 = HIGH LEVEL   0 = LOW LEVEL
X = DON'T CARE   NC = NO CHANGE

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . . +265°C



TERMINAL ASSIGNMENT

CD4031B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages Values at –40, +25, +85, Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min. Q	0.4	0,5	5	2.56	2.44	1.68	1.44	2.04	4	–	mA
	0.5	0,10	10	6.4	6	4.4	3.6	5.2	10.4	–	
	1.5	0,15	15	16.8	16	11.2	9.6	13.6	27.2	–	
$\overline{Q}$, Q', CL_D	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min. Q, $\overline{Q}$, Q', CLD	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5, 13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5, 13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

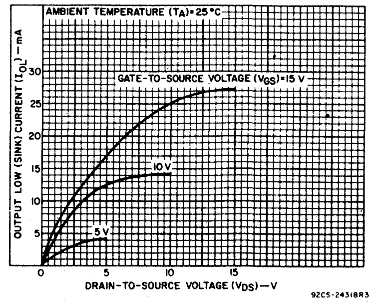


Fig. 2 — Typical output low (sink) current characteristics (Q sink current = 4X ordinate).

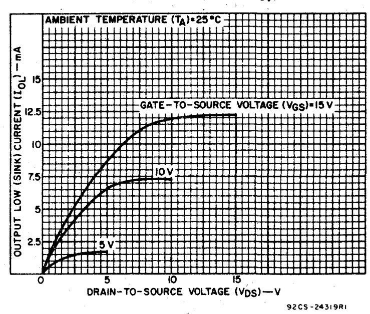


Fig. 3 — Minimum output low (sink) current characteristics (Q sink current = 4X ordinate).

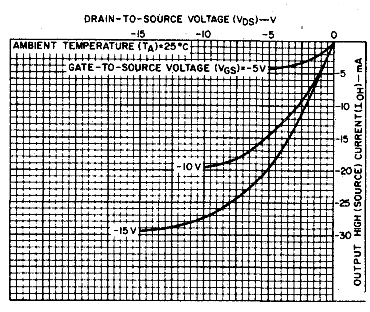


Fig. 4 — Typical output high (source) current characteristics.

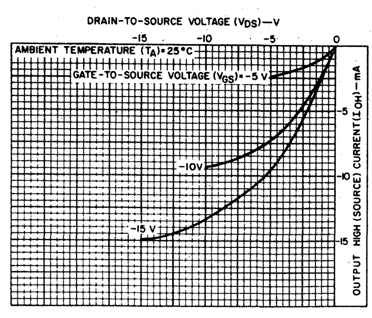


Fig. 5 — Minimum output high (source) current characteristics.

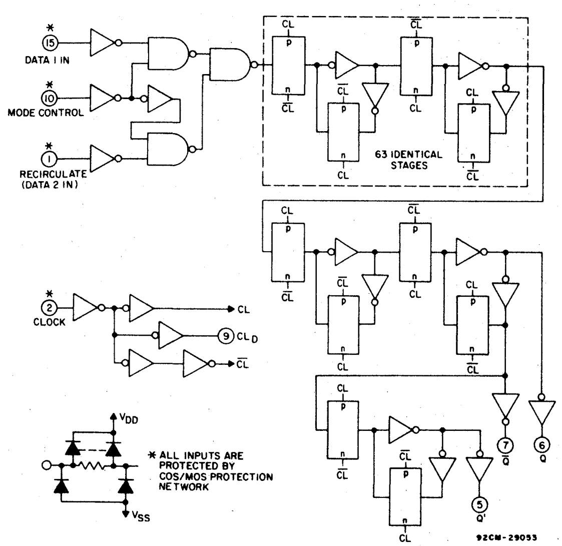


Fig. 1 — Logic diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25^oC$; Input $t_r, t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ*

CHARACTERISTIC	TEST CONDITIONS V_{DD}(V)	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time: Clock to $\overline{Q}$, t_{PHL}, t_{PLH}; Clock to Q, t_{PLH}	5	–	250	500	ns
	10	–	110	220	
	15	–	90	180	
$\overline{Clock}$ to Q′, t_{PHL}, t_{PLH}; Clock to Q, t_{PHL}	5	–	190	380	ns
	10	–	80	160	
	15	–	65	130	
Clock to CL_D	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Transition Time, t_{THL}, t_{TLH} (Any Output, except Q, t_{THL})	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Q, t_{THL}	5	–	50	100	ns
	10	–	25	50	
	15	–	20	40	
Minimum Data Setup Time, t_S	5	–	30	60	ns
	10	–	15	30	
	15	–	10	20	
Minimum Data Hold Time, t_H	5	–	30	60	ns
	10	–	15	30	
	15	–	10	20	
Minimum Clock Pulse Width, t_W	5	–	120	240	ns
	10	–	50	100	
	15	–	40	80	
Maximum Clock Input Frequency, f_{CL}**	5	2	4	–	MHz
	10	5	10	–	
	15	6	12	–	
Clock Input Rise or Fall Time, t_{rCL}, t_{fCL}*	5	–	–	1000	μs
	10	–	–	1000	
	15	–	–	200	
Input Capacitance, C_{IN} (Any Input)	–	–	5	7.5	pF

*If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 50 pF and the transition time of the output driving stage.

**Maximum Clock Frequency for Cascaded Units;

a) Using Delayed Clock Feature in Recirculation Mode:

$$f_{max} = \frac{1}{(n-1)\ CL_D \text{ prop. delay} + Q \text{ prop. delay} + \text{set-up time}}$$ where n = number of packages

b) Not Using Delayed Clock:

$$f_{max} = \frac{1}{\text{propagation delay} + \text{set-up time}}$$

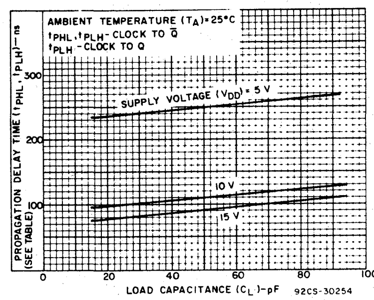


Fig. 6 – Typical propagation delay time as a function of load capacitance (see table).

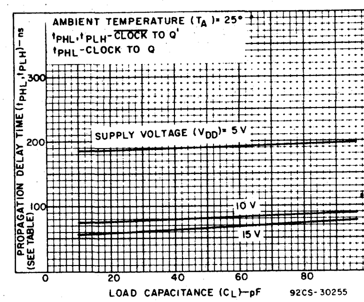


Fig. 7 – Typical propagation delay time as a function of load capacitance (see table).

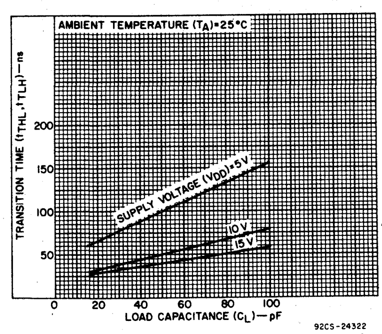


Fig. 8 – Typical transition time as a function of load capacitance (except Q, t_{THL}).

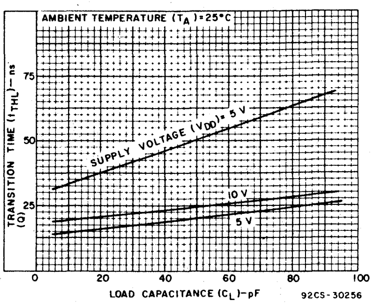


Fig. 9 — Typical transition time as a function of load capacitance (Q, t_{THL}).

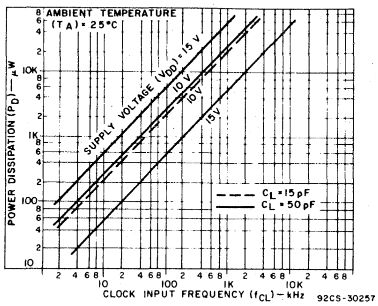


Fig. 10 — Typical dynamic power dissipation as a function of clock input frequency.

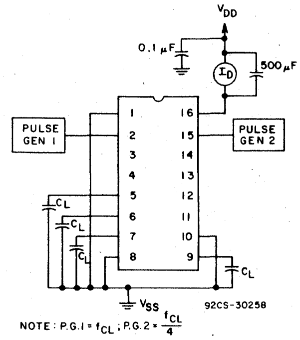


Fig. 11 — Dynamic power dissipation test circuit.

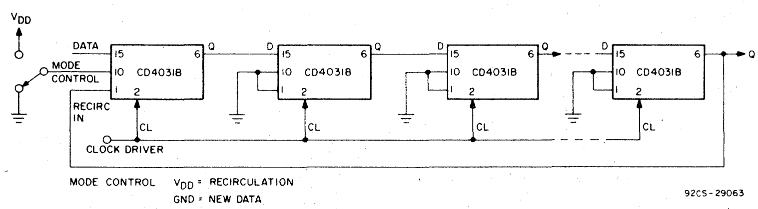


Fig. 12 — Cascading using direct clocking for high-speed operation (see clock rise and fall time requirement).

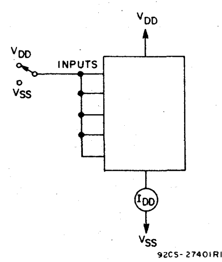


Fig. 13 — Quiescent-device-current test circuit.

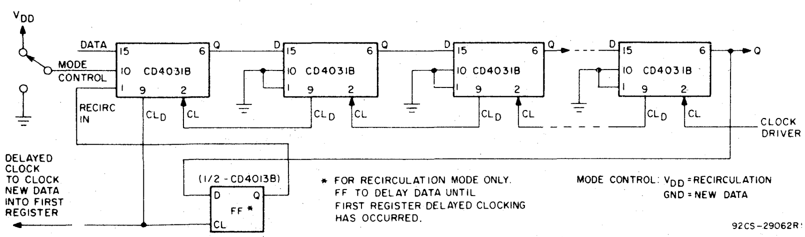


Fig. 14 — Cascading using delayed clocking for reduced clock drive requirements.

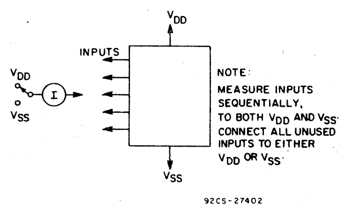


Fig. 15 — Input-leakage current.

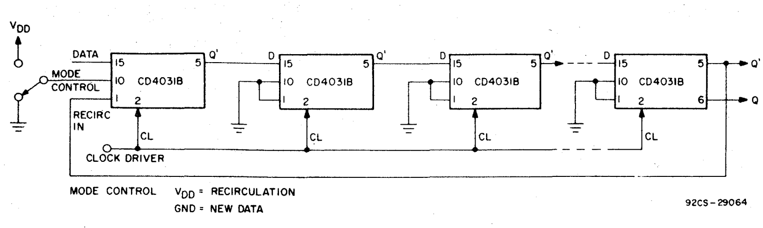


Fig. 16 — Cascading using half-clock-pulse delayed data output (Q') to permit use of slow rise and fall time clock inputs.

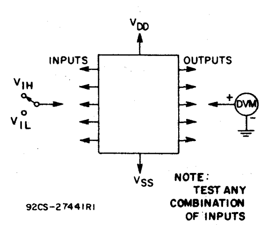
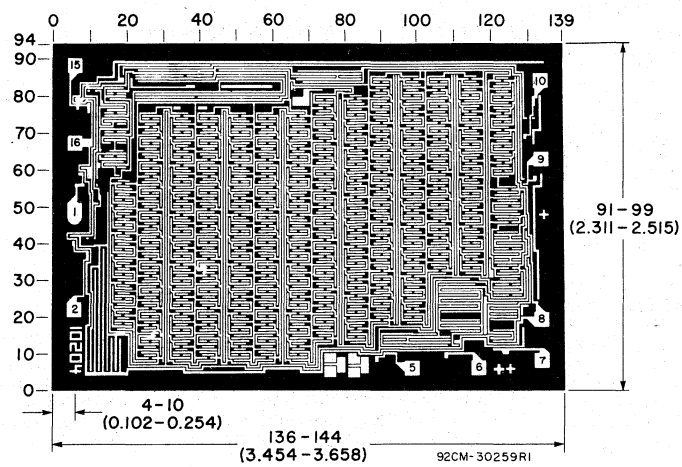


Fig. 17 — Input-voltage test circuit.



Dimensions and pad layout for CD4031B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4032B, CD4038B Types

COS/MOS Triple Serial Adders

High-Voltage Types (20-Volt Rating)
Positive Logic Adder – CD4032B
Negative Logic Adder – CD4038B

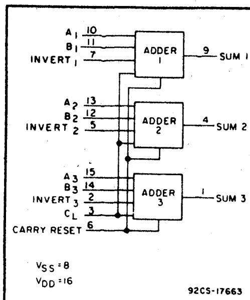
The RCA-CD4032B and CD4038B types consist of three serial adder circuits with common CLOCK and CARRY-RESET inputs. Each adder has provisions for two serial DATA INPUT signals and an INVERT command signal. When the command signal is a logical "1", the sum is complemented. Data words enter the adder with the least significant bit first; the sign bit trails. The output is the MOD 2 sum of the input bits plus the carry from the previous bit position. The carry is only added at the positive-going clock transition for the CD4032B or at the negative-going clock for the CD4038B, thus, for spike-free operation the input data transitions should occur as soon as possible after the triggering edge.

The CARRY is reset to a logical "0" at the end of each word by applying a logical "1" signal to a CARRY-RESET input one-bit-position before the application of the first bit of the next word.

The CD4032B and CD4038B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Invert inputs on all adders for sum complementing applications
- Fully static operation . . . . dc to 10 MHz (typ.) @ V_{DD} = 10 V
- Single-phase clocking
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range)
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



CD4032B, CD4038B
FUNCTIONAL DIAGRAM

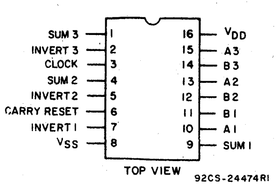
Applications:

- Serial arithmetic units
- Digital correlators
- Digital datalink computers
- Flight control computers
- Digital servo control systems

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

CD4032B, CD4038B
TERMINAL DIAGRAM



RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC		V_{DD}	Min.	Max.	UNITS
Supply Voltage Range (at T_A = Full Package-Temperature Range)			3	18	V
Clock Input Frequency,	f_{CL}	5 10 15	– – –	2.5 5 7.5	MHz
Clock Input Rise or Fall Time,	t_rCL, t_fCL	5 10 15	– – –	500 500 500	µs
Data Input Set-Up Time, Clock to A or B Inputs	t_{SU}	5 10 15	200 80 60	– – –	ns

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages; Values at –40, +25, +85 Apply to E Package: –55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

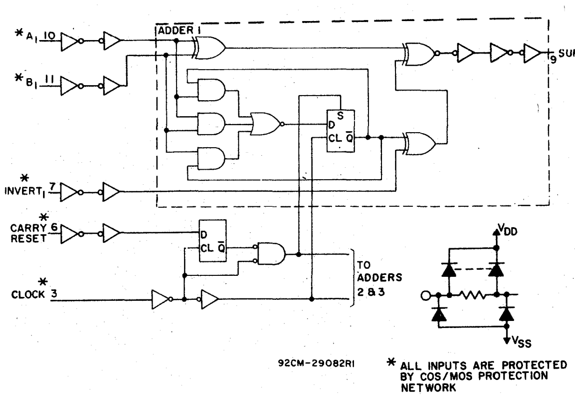


Fig.1 – CD4032B logic diagram of one of three serial adders.

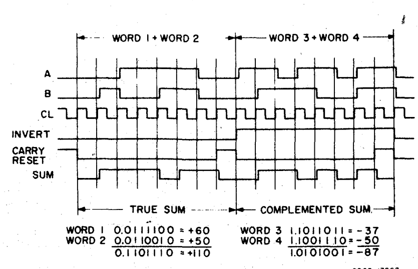


Fig.2 – CD4032B timing diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25°C$, Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ*

CHARACTERISTIC	TEST CONDITIONS V_{DD}(V)	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} A,B, Carry Reset, or Invert Inputs to Sum Outputs	5 10 15	– – –	260 120 90	520 240 180	ns
Clock Input to Sum Outputs	5 10 15	– – –	325 175 150	650 350 300	ns
Transition Time: t_{THL}, t_{TLH}	5 10 15	– – –	100 50 40	200 100 80	ns
Minimum Data Input Setup Time, t_{SU} Clock to A or B Inputs	5 10 15	– – –	125 50 40	200 80 60	ns
Maximum Clock Input Frequency, f_{CL}	5 10 15	2.5 5 7.5	4.5 10 15	– – –	MHz
Clock Input Rise or Fall Time, t_{rCL}, t_{fCL}*	5 10 15	– – –	– – –	500 500 500	µs
Input Capacitance, C_{IN}	(Any Input)	–	5	7.5	pF

* If more than one unit is cascaded t_{rCL} should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

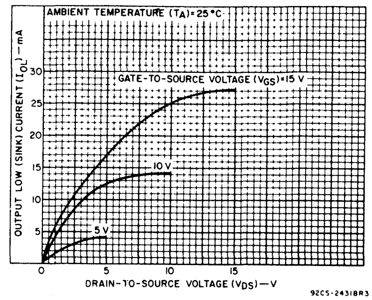


Fig. 5 – Typical output low (sink) current characteristics.

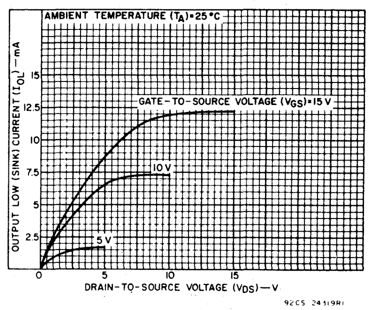


Fig. 6 – Minimum output low (sink) current characteristics.

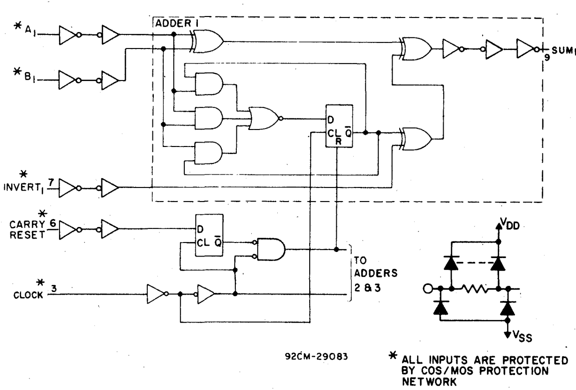


Fig. 3 – CD4038B logic diagram of one of three serial adders.

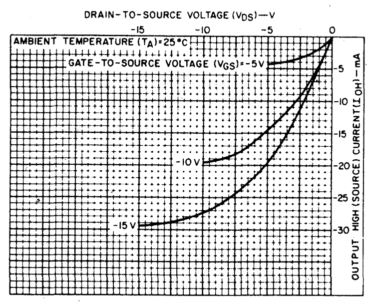


Fig. 7 – Typical output high (source) current characteristics.

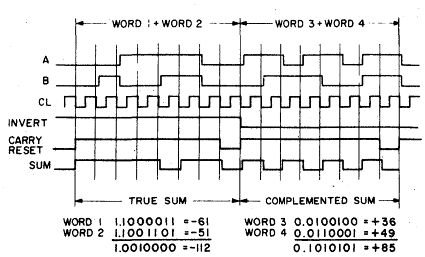


Fig.4 – CD4038B timing diagram.

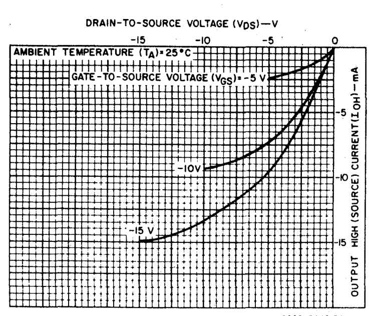


Fig. 8 – Minimum output high (source) current characteristics.

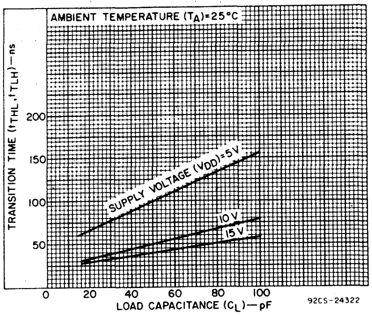


Fig. 9 – Typical transition time as a function of load capacitance.

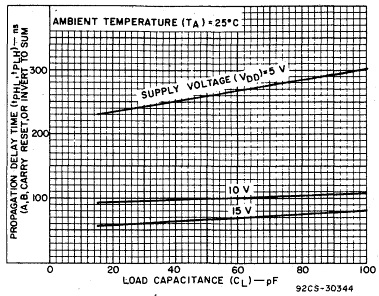


Fig. 10 – Typical propagation delay times as a function of load capacitance (A, B, carry reset or invert to SUM).

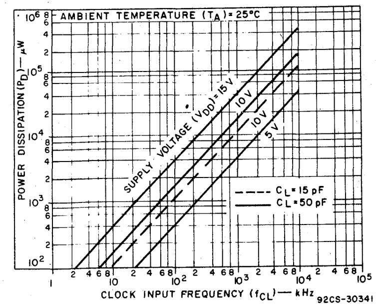


Fig. 11 – Typical dynamic power dissipation as a function of clock input frequency.

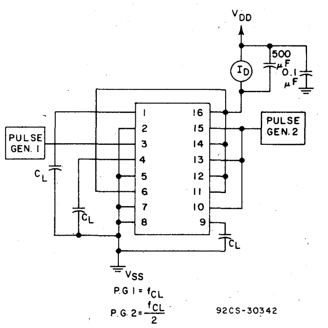


Fig. 12 – Dynamic power dissipation test circuit.

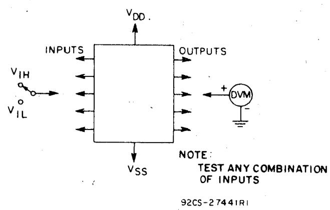


Fig. 13 – Input voltage test circuit.

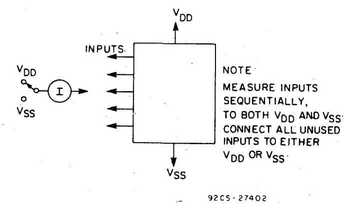


Fig. 14 – Input current test circuit.

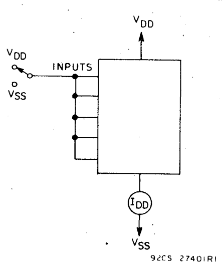
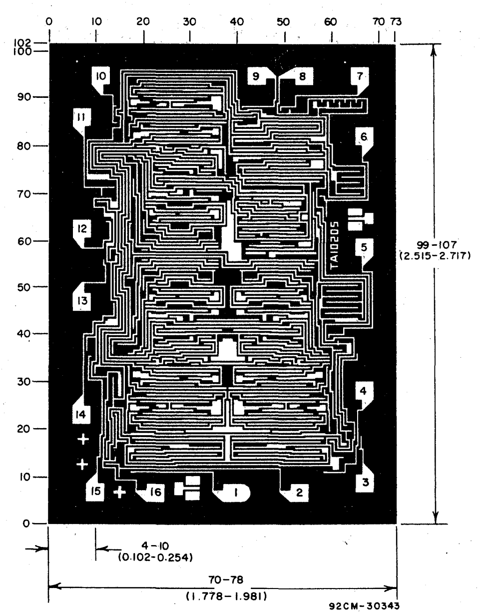


Fig. 15 – Quiescent-device current test circuit.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

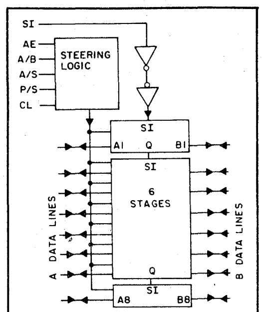


Dimensions and pad layout for CD4032BH; dimensions and pad layout for CD4038BH are identical.

CD4034B Types

COS/MOS 8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register

High-Voltage Types (20-Volt Rating)



92CS-29108
Functional Diagram

The RCA-CD4034B is a static eight-stage parallel-or serial-input parallel-output register. It can be used to:

1) bidirectionally transfer parallel information between two buses, 2) convert serial data to parallel form and direct the parallel data to either of two buses, 3) store (recirculate) parallel data, or 4) accept parallel data from either of two buses and convert that data to serial form. Inputs that control the operations include a single-phase CLOCK (CL), A DATA ENABLE (AE), ASYNCHRONOUS/SYNCHRONOUS (A/S), A-BUS-TO-B-BUS/B-BUS-TO-A-BUS (A/B), and PARALLEL/SERIAL (P/S).

Data inputs include 16 bidirectional parallel data lines of which the eight A data lines are inputs (3-state outputs) and the B data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for SERIAL DATA is also provided.

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

PARALLEL OPERATION

A high P/S input signal allows data transfer into the register via the parallel data lines synchronously with the positive transition of the clock provided the A/S input is low. If the A/S input is high the transfer is independent of the clock. The direction of data flow is controlled by the A/B input. When this signal is high the A data lines are inputs (and B data lines are outputs); a low A/B signal reverses the direction of data flow.

The AE input is an additional feature which allows many registers to feed data to a common bus. The A DATA lines are enabled only when this signal is high.

Data storage through recirculation of data in each register stage is accomplished by making the A/B signal high and the AE signal low.

Applications:

- **Parallel Input/Parallel Output, Parallel Input/Serial Output, Serial Input/Parallel Output, Serial Input/Serial Output Register**
- **Shift right/shift left register**
- **Shift right/shift left with parallel loading**
- **Address register**
- **Buffer register**
- **Bus system register with enable parallel lines at bus side**
- **Double bus register system**
- **Up-Down Johnson or ring counter**
- **Pseudo-random code generators**
- **Sample and hold register (storage, counting, display)**
- **Frequency and phase comparator**

SERIAL OPERATION

A low P/S signal allows serial data to transfer into the register synchronously with the positive transition of the clock. The A/S input is internally disabled when the register is in the serial mode (asynchronous serial operation is not allowed).

The serial data appears as output data on either the B lines (when A/B is high) or the A lines (when A/B is low and the AE signal is high).

Register expansion can be accomplished by simply cascading CD4034B packages.

The CD4034B types are supplied in 24-lead dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Bidirectional parallel data input**
- **Parallel or serial inputs/parallel outputs**
- **Asynchronous or synchronous parallel data loading**
- **Parallel data-input enable on "A" data lines (3-state output)**
- **Data recirculation for register expansion**
- **Multipackage register expansion**
- **Fully static operation dc-to-10 MHz (typ.) at V_{DD} = 10 V**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package-temperatur range):**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specification for Description of 'B' Series CMOS Devices'**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	–0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	–55 to +125°C
PACKAGE TYPE E	–40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	–65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)			3	18	V
Data Setup Time, t_S	Serial Data to Clock	5	160	–	ns
		10	60	–	
		15	40	–	
	Parallel Data to Clock	5	50	–	ns
		10	30	–	
		15	20	–	
Clock Pulse Width, t_W		5	350	–	ns
		10	140	–	
		15	80	–	
Clock Input Frequency, f_{CL}		5	dc	2	MHz
		10		5	
		15		7	
Clock Input Rise or Fall Time, t_rCL, t_fCL*		5, 10, 15	–	15	μs

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

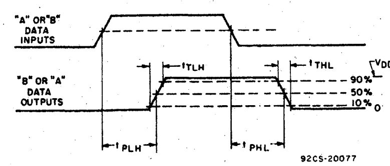
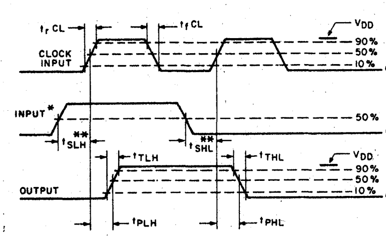
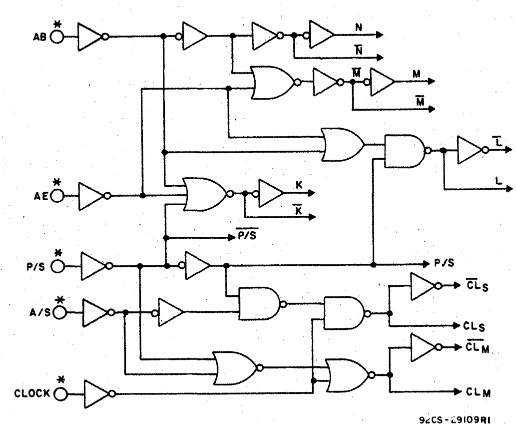


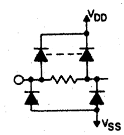
Fig. 2 – Asynchronous operation propagation delay time and transition time.



*INPUT REFERS TO ANY OF THE "A" OR "B" DATA INPUTS, "A" ENABLE, SERIAL INPUT, A/B, P/S, OR A/S INPUTS
** t_{SLH} AND t_{SHL} ARE SET-UP TIMES
92CS-20078

Fig. 3 – Synchronous operation propagation delay times, transition times, and set-up times.





* INPUTS PROTECTED BY COS/MOS PROTECTION NETWORK

Fig. 1 – Steering logic diagram.

FLIP-FLOP TRUTH TABLE

INPUTS			OUTPUT
$\overline{CL}_M$	$\overline{CL}_S$	D	Q
↓	↓	0	0
↑	↓	0	0
↓	↑	0	INVALID CONDITION
↑	↑	X	0
↓	↓	1	1
↑	↓	1	1
↓	↑	1	INVALID CONDITION

1 = High Level   0 = Low Level   X = Don't Care

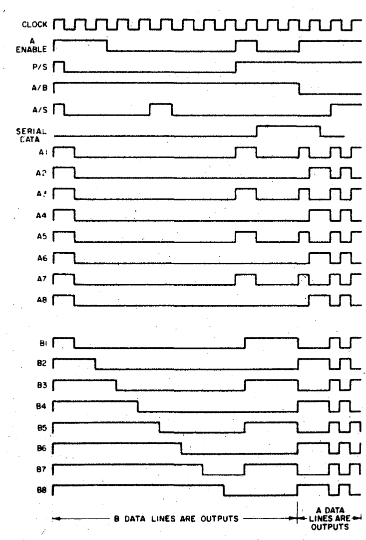


Fig. 4 – Timing diagram.

CD4034B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages Values at –40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current* I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm10^{-4}$	±0.4	μA

* All inputs except A and B Lines.

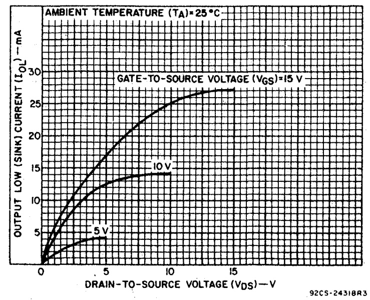


Fig. 5 – Typical output low (sink) current characteristics.

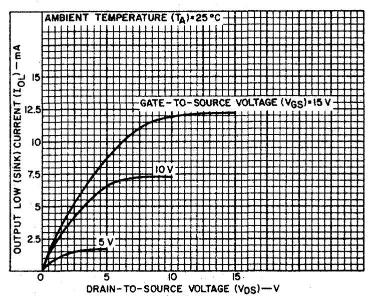


Fig. 6 – Minimum output low (sink) current characteristics.

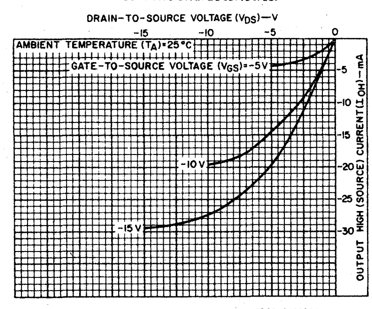


Fig. 7 – Typical output high (source) current characteristics.

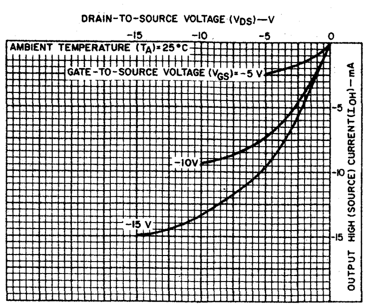


Fig. 8 – Minimum output high (source) current characteristics.

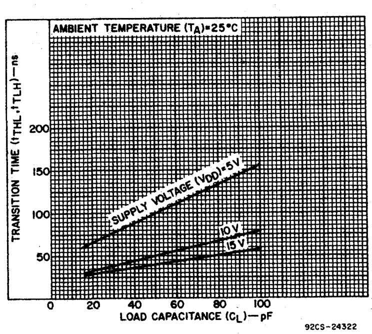


Fig. 9 – Typical transition time as a function of load capacitance.

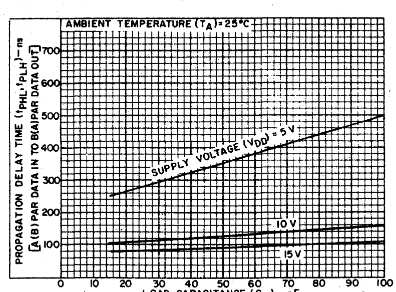


Fig. 10 – Typical propagation delay time as a function of load capacitance [A(B) parallel Data Input to B(A) parallel Data Output, synchronous or asynchronous].

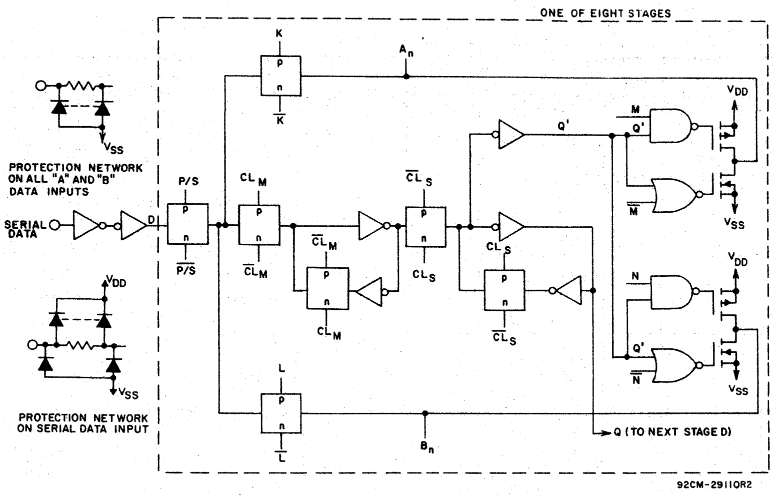


Fig. 11 – Register stage logic diagram (1 of 8 stages).

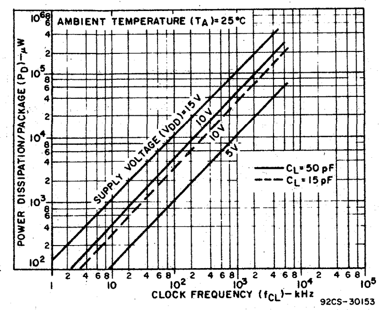


Fig. 12 – Typical dynamic power dissipation as a function of clock frequency.

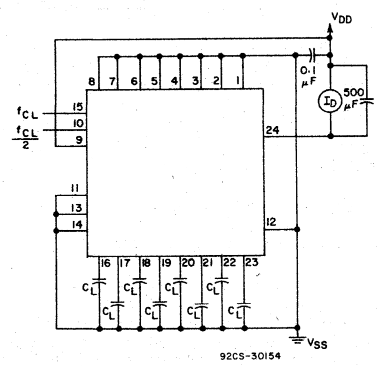


Fig. 13 – Dynamic power dissipation test circuit.

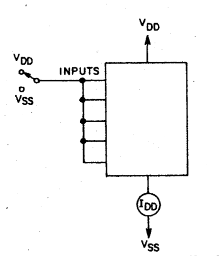


Fig. 14 – Quiescent-device-current test circuit.

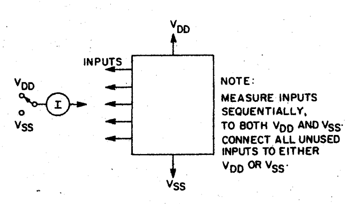


Fig. 15 – Input-current test circuit.

TRUTH TABLE FOR REGISTER INPUT-LEVELS AND RESULTING REGISTER OPERATION

"A" Enable	P/S	A/B	A/S	Operation*
0	0	0	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Outputs Disabled
0	0	1	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
0	1	0	0	Parallel Mode; "B" Synch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
0	1	0	1	Parallel Mode; "B" Asynch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
0	1	1	0	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Synch. Data Recirculation
0	1	1	1	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Asynch. Data Recirculation
1	0	0	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Output
1	0	1	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
1	1	0	0	Parallel Mode; "B" Synch. Parallel Data Input, "A" Parallel Data Output
1	1	0	1	Parallel Mode; "B" Asynch. Parallel Data Input, "A" Parallel Data Output
1	1	1	0	Parallel Mode; "A" Synch. Parallel Data Input, "B" Parallel Data Output
1	1	1	1	Parallel Mode; "A" Asynch. Parallel Data Input, "B" Parallel Data Output

*Outputs change at positive transition of clock in the serial mode and when the A/S control input is "low" in the parallel mode. During transfer from parallel to serial operation A/S should remain low in order to prevent D_S transfer into Flip Flops.

1 = HIGH LEVEL   0 = LOW LEVEL   X = DON'T CARE

CD4034B Types

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25^oC$; Input $t_r, t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ*

CHARACTERISTIC		V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time, A(B) Parallel Data In to B(A) Parallel Data Out	t_{PHL}, t_{PLH}	5 10 15	– – –	350 120 85	700 240 170	ns
3-State Propagation Delay Time, A/B or AE to "A" OUT	$t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}$	5 10 15	– – –	200 80 60	400 160 120	ns
Transition Time,	t_{THL}, t_{TLH}	5 10 15	– – –	100 50 40	200 100 80	ns
Minimum Data Setup Time, Serial Data to Clock	t_{SU}	5 10 15	– – –	80 30 20	160 60 40	ns
Parallel Data to Clock		5 10 15	– – –	25 15 10	50 30 20	ns
Minimum High-Level Pulse Width, AE, P/S, A/S	t_W	5 10 15	– – –	175 70 40	350 140 80	ns
Maximum Clock Frequency,	f_{CL}	5 10 15	2 5 7	4 10 14	– – –	MHz
Minimum Clock Pulse Width,	t_W	5 10 15	– – –	125 50 35	250 100 70	ns
Maximum Clock Rise or Fall Time, t_rCL, t_fCL*		5,10,15	–	–	15	μs
Input Capacitance, (Any Input)	C_{IN}	–	–	5	7.5	pF

*If more than one unit is cascaded, t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

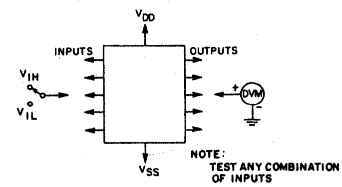


Fig. 16 – Input-voltage test circuit.

Applications

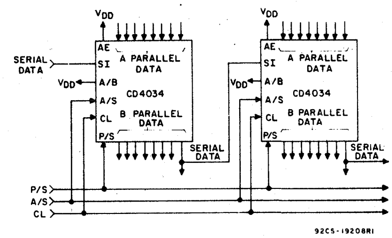


Fig. 17 – 16-bit parallel in/parallel out, parallel in/serial out, serial in/ parallel out, serial in/serial out register.

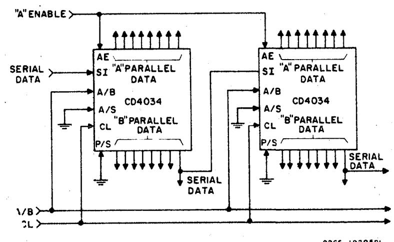
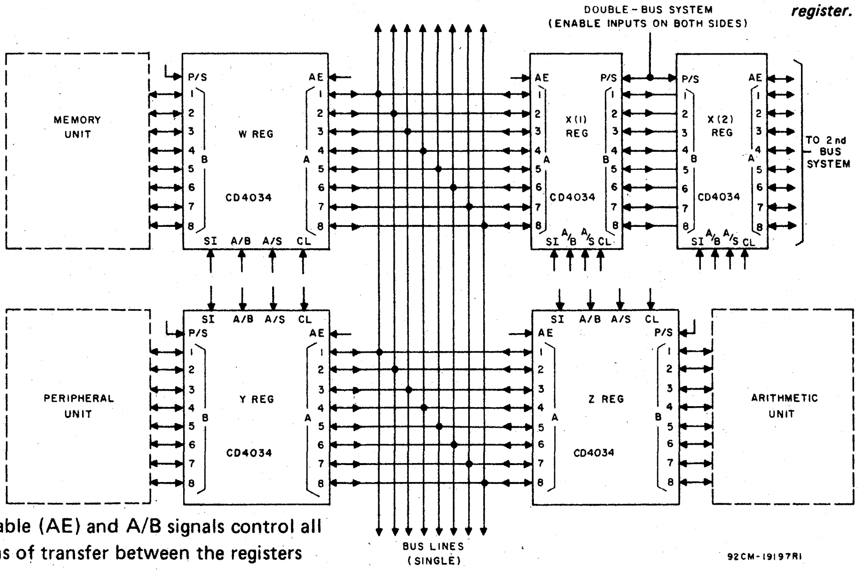
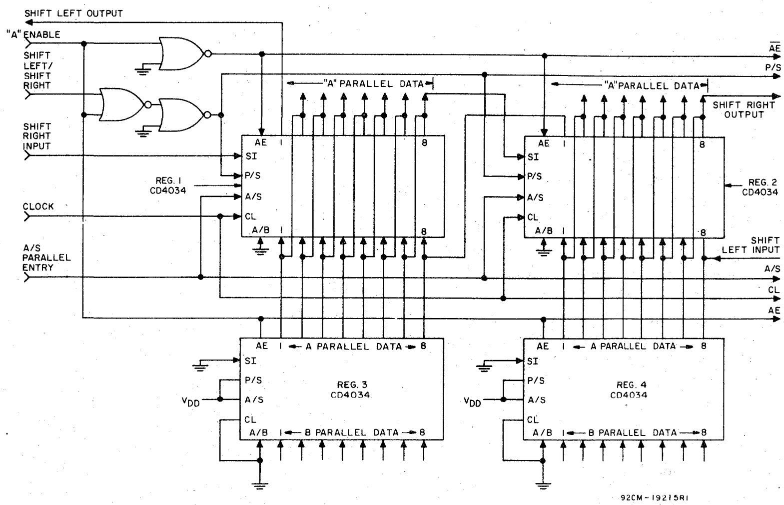


Fig. 18 – 16-bit serial in/gated parallel out register.



The "A" enable (AE) and A/B signals control all combinations of transfer between the registers and bus systems.

Fig. 19 – Single- and double-bus systems.



A "High" ("Low") on the shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Reg. 1 and 2 and enables the "A" data lines on registers 3 and 4 and allows parallel data into registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Reg. 3 and 4 and associated logic are not required.

* Shift left input must be disabled during parallel entry.

Fig. 20 – Shift right/shift left with parallel inputs.

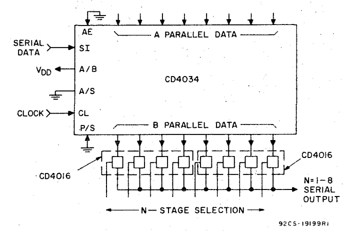


Fig. 21 – N-stage shift register with fixed serial output line.

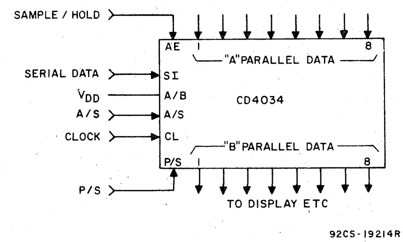
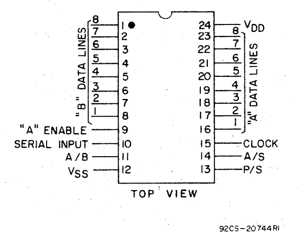
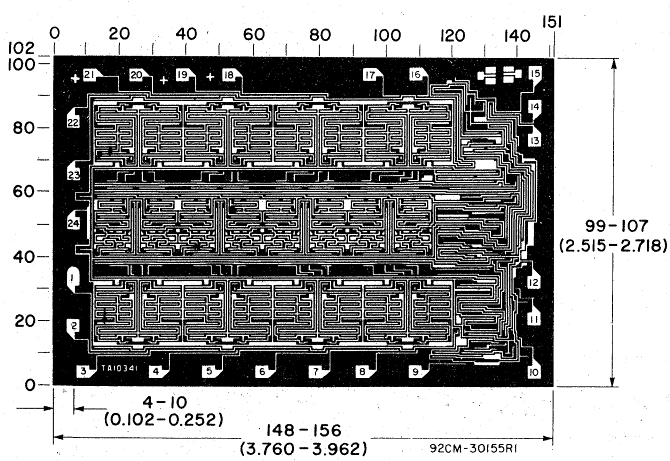


Fig. 22 – Sample and hold register—serial/ parallel in—parallel out.



TERMINAL DIAGRAM



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for CD4034BH.

CD4035B Types

COS/MOS 4-Stage Parallel In/Parallel Out Shift Register

with J-$\overline{K}$ Serial Inputs and True/ Complement Outputs

High-Voltage Types (20-Volt Rating)

The RCA-CD4035B is a four-stage clocked signal serial register with provision for synchronous PARALLEL inputs to each stage and SERIAL inputs to the first stage via J$\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low).

Parallel entry into each register stage is permitted when the PARALLEL/SERIAL control is high.

In the parallel or serial mode information is transferred on positive clock transitions.

When the TRUE/COMPLEMENT control is high, the true contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with respect to the CLOCK signal.

J$\overline{K}$ input logic is provided on the first stage SERIAL input to minimize logic requirements particularly in counting and sequence-generation applications. With J$\overline{K}$ inputs connected together, the first stage becomes a D flip-flop. An asynchronous common RESET is also provided.

The CD4035B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

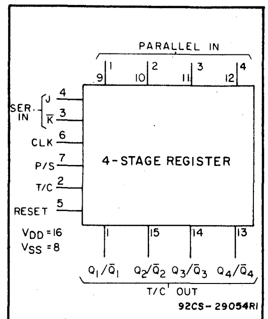
- 4-Stage clocked shift operation
- Synchronous parallel entry on all 4 stages
- J$\overline{K}$ inputs on first stage
- Asynchronous True/Complement control on all outputs
- Static flip-flop operation; Master-slave configuration
- Buffered inputs and outputs
- High speed — 12 MHz (typ.) at V_{DD} = 10 V
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of "B" Series CMOS Devices"

Applications:

- Counters, Registers
  Arithmetic-unit registers
  Shift-left — shift right registers
  Serial-to-parallel/parallel-to-serial conversions
- Sequence generation
- Control circuits
- Code conversion

FIRST STAGE TRUTH TABLE

	t_{n-1} (INPUTS)				t_n (OUTPUTS)
CL	J	$\overline{K}$	R	Q_{n-1}	Q_n
↑ (rising edge)	0	X	0	0	0
↑ (rising edge)	1	X	0	0	1
↑ (rising edge)	X	0	0	1	0
↑ (rising edge)	1	0	0	Q_{n-1}	$\overline{Q}_{n-1}$ TOGGLE MODE
↑ (rising edge)	X	1	0	1	1
↓ (falling edge)	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0



FUNCTIONAL DIAGRAM

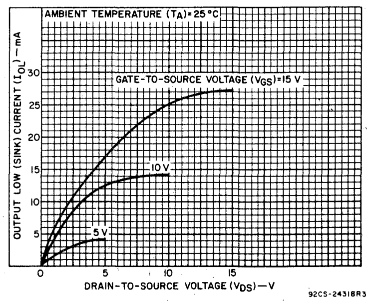


Fig. 1 — Typical output low (sink) current characteristics.

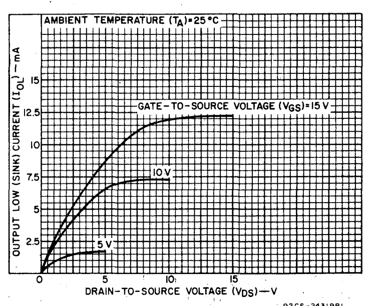


Fig. 2 — Minimum output low (sink) current characteristics.

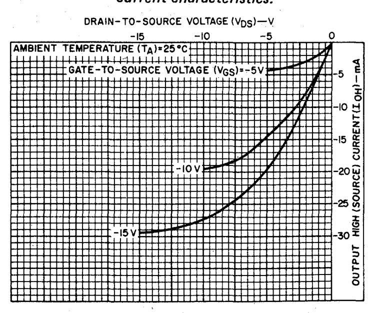


Fig. 3 — Typical output high (source) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . −55 to +125°C
PACKAGE TYPE E . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . +265°C

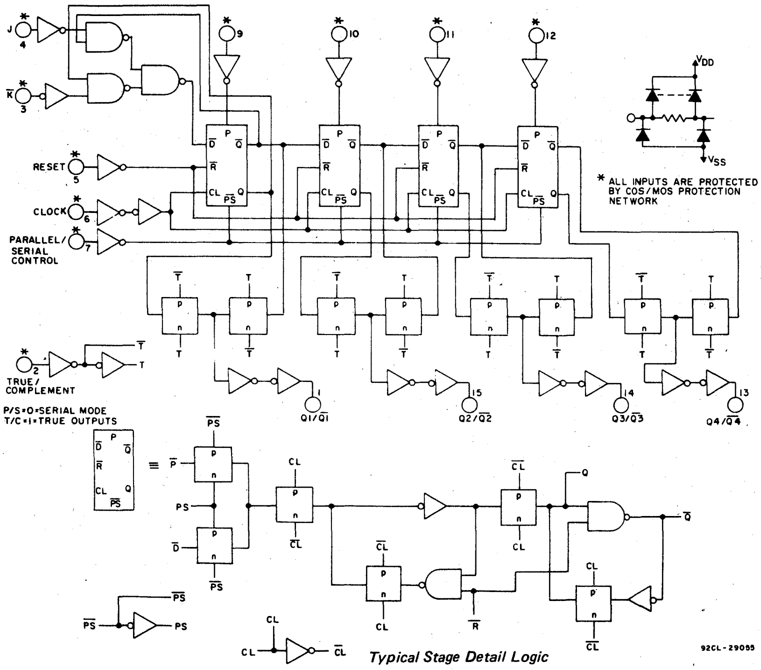


Fig. 4 — Logic diagram.

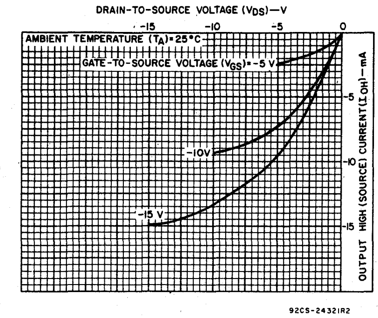


Fig. 5 — Minimum output high (source) current characteristics.

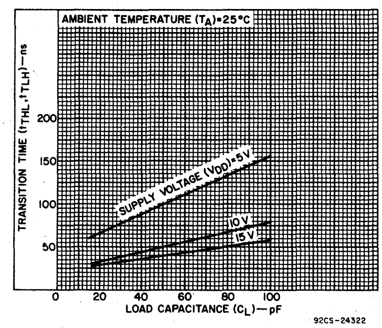


Fig. 6 — Typical transition time as a function of load capacitance.

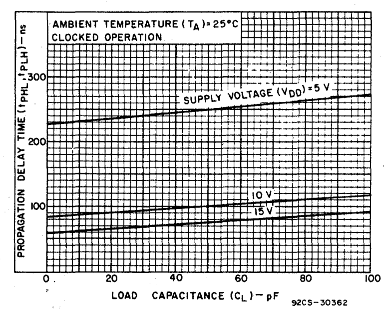


Fig. 7 — Typical propagation delay times as a function of load capacitance (Q output).

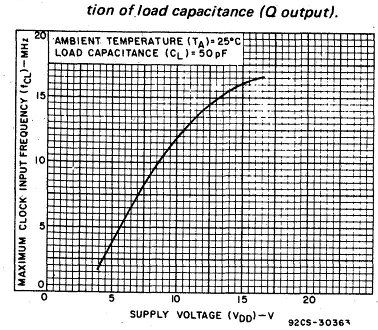


Fig. 8 — Typical maximum clock input frequency as a function of supply voltage.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S: J/$\overline{K}$ Lines	5	220	–	ns
	10	80	–	ns
	15	60	–	ns
Parallel-In Lines	5	140	–	ns
	10	50	–	ns
	15	40	–	ns
Clock Pulse Width, t_W	5	200	–	ns
	10	90	–	ns
	15	60	–	ns
Clock Input Frequency, f_{CL}	5	dc	2	MHz
	10	dc	6	MHz
	15	dc	8	MHz
Clock Rise or Fall Time, t_rCL, t_fCL:	5	–	15	μs
	10	–	15	μs
	15	–	15	μs
Reset Pulse Width, t_W	5	250	–	ns
	10	110	–	ns
	15	80	–	ns

CD4035B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages; Values at −40, +25, +85 Apply to E Package: −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
		0,10	10	9.95				9.95	10	–	
		0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5		5	1.5				–	–	1.5	V
	1,9		10	3				–	–	3	
	1.5,13.5		15	4					–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5		5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5		15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

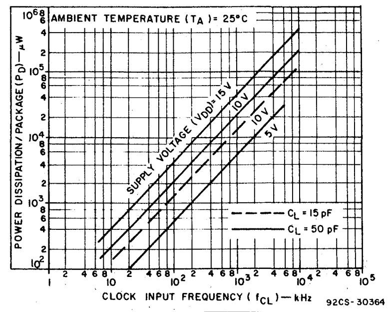


Fig. 9 – Typical dynamic power dissipation as a function of clock input frequency.

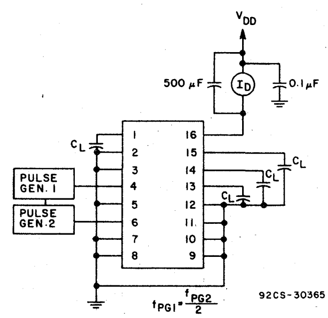


Fig. 10 – Dynamic power dissipation test circuit.

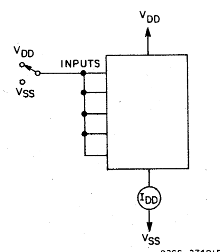


Fig. 11 – Quiescent-device current test circuit.

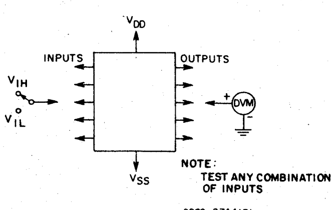


Fig. 12 – Input-voltage test circuit.

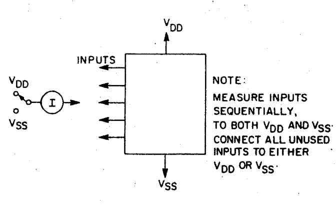


Fig. 13 – Input-current test circuit.

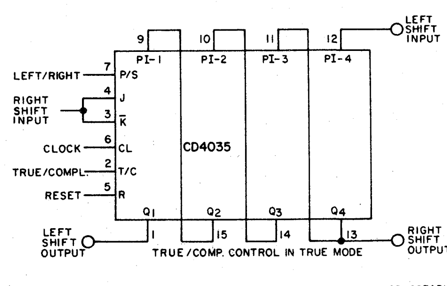
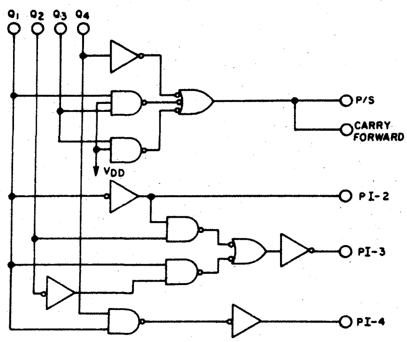


Fig. 14 – Shift left/shift right register.



Using Couleur's Technique (BIDEC)▲, a binary number (most significant bit, MSB) first is shifted and processed, such that the BCD equivalent is obtained when the last binary bit is clocked into the register. The CD4035B, with the correct conversion logic, can also be used as a BCD-to-binary converter.

▲The basic rule is: If a 4 or less is in a decade, shift with the next clock pulse; if a 5 or greater is in a decade, add 3 and then shift at the next clock pulse. For more information refer to "IRE TRANSACTIONS ON ELECTRONIC COMPUTERS", Dec. 1958, Pages 313–316.

Fig. 15 – BIDEC logic.

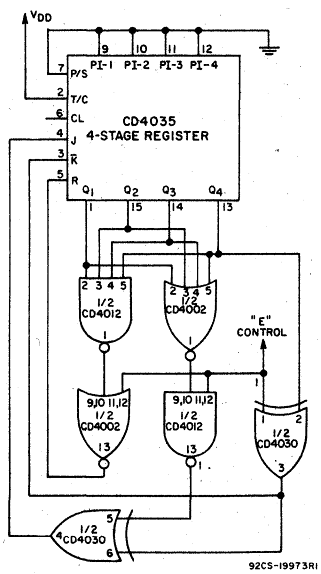


Fig. 16(a) – Double sequence generator.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$, Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ

CHARACTERISTICS	TEST CONDITIONS V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
CLOCKED OPERATION					
Propagation Delay Time: t_{PHL}, t_{PLH}	5	–	250	500	ns
	10	–	100	200	
	15	–	75	150	
Transition Time: t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Minimum Clock Pulse Width, t_W	5	–	100	200	ns
	10	–	45	90	
	15	–	30	60	
Clock Rise or Fall Time, t_rCL, t_fCL*	5,10, 15	–	–	15	μs
Minimum Setup Time: J/K̄ Lines	5	–	110	220	ns
	10	–	40	80	
	15	–	30	60	
Parallel-In-Lines	5	–	70	140	ns
	10	–	25	50	
	15	–	20	40	
Maximum Clock Frequency, f_{CL}	5	2	4	–	MHz
	10	6	12	–	
	15	8	16	–	
Input Capacitance, C_{IN}	Any Input	–	5	7.5	pF
RESET OPERATION					
Propagation Delay Time: t_{PHL}, t_{PLH}	5	–	230	460	ns
	10	–	100	200	
	15	–	80	160	
Minimum Reset Pulse Width, t_W	5	–	125	250	ns
	10	–	55	110	
	15	–	40	40	

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

Control = E =	0				1				
	Q_1 A	Q_2 B	Q_3 C	Q_4 D		Q_1 A	Q_2 B	Q_3 C	Q_4 D
0	0	0	0	0	15	1	1	1	1
1	1	0	0	0	14	0	1	1	1
2	0	1	0	0	13	1	0	1	1
5	1	0	1	0	10	0	1	0	1
10	0	1	0	1	5	1	0	1	0
4	0	0	1	0	11	1	1	0	1
9	1	0	0	1	6	0	1	1	0
3	1	1	0	0	12	0	0	1	1
6	0	1	1	0	9	1	0	0	1
13	1	0	1	1	2	0	1	0	0
11	1	1	0	1	4	0	0	1	0
7	1	1	1	0	8	0	0	0	1
14	0	1	1	1	1	1	0	0	0
12	0	0	1	1	3	1	1	0	0
8	0	0	0	1	7	1	1	1	0

Using a control line (E) two different state sequences can be generated. For example, suppose the following two sequences are desired on command (control line E)

Fig. 16(b) – State sequences.

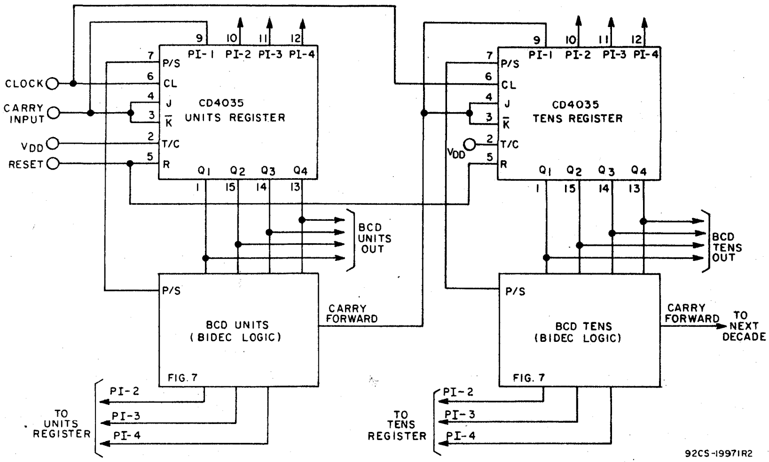
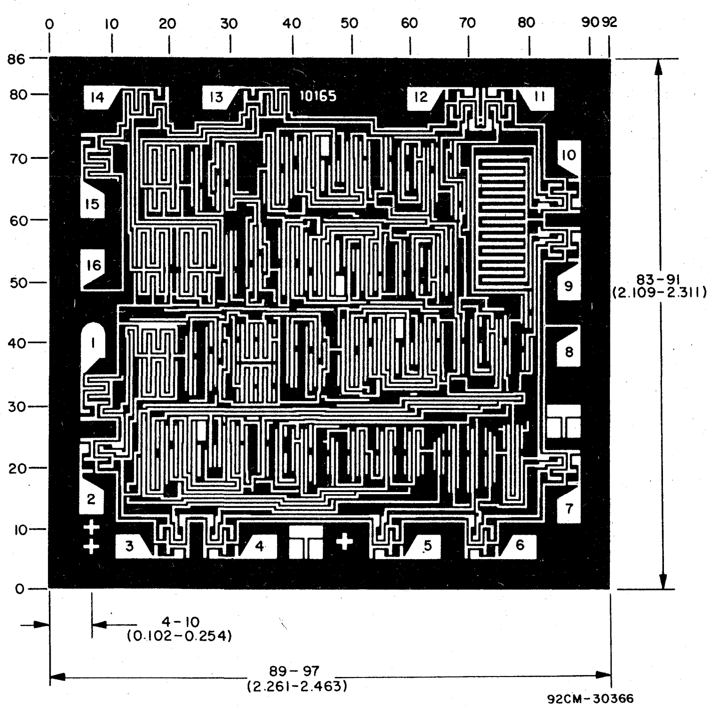


Fig. 17 – Binary-to-BCD converter.

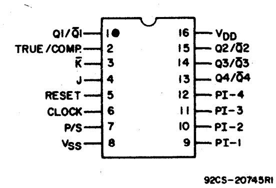


Dimensions and pad layout for CD4035BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

TERMINAL DIAGRAM
Top View



COS/MOS Quad True/Complement Buffer

High Voltage Types (20-Volt Rating)

The RCA-CD4041UB types are quad true/complement buffers consisting of n- and p-channel units having low-channel resistance and high current (sourcing and sinking) capability. The CD4041UB is intended for use as a buffer, line driver, or COS/MOS-to-TTL driver. It can be used as an ultra-low power resistor-network driver for A/D and D/A conversion, as a transmission-line driver, and in other applications where high noise immunity and low-power dissipation are primary design requirements.

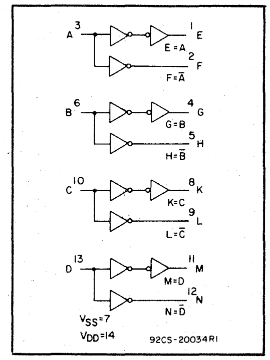
The CD4041UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

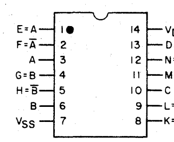
Features:

- **Balanced sink and source current; approximately 4 times standard "B" drive**
- **Equalized delay to true and complement outputs**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **High current source/sink driver**
- **COS/MOS-to-DTL/TTL Converter Buffer**
- **Display driver**
- **MOS clock driver**
- **Resistor network driver (Ladder or weighted R)**
- **Buffer**
- **Transmission line driver**





92CS-20755R1

TOP VIEW
TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

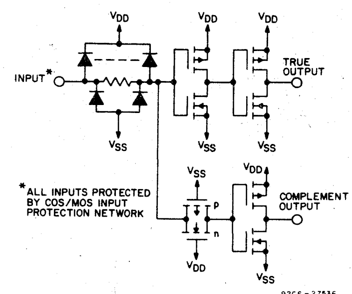


Fig.1 – Schematic diagram 1 of 4 buffers.

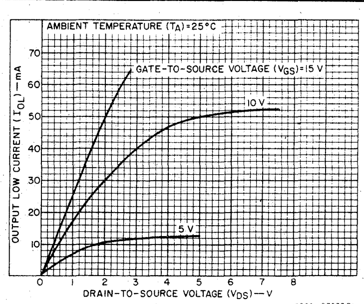


Fig.2 – Typical output low (sink) current characteristics.

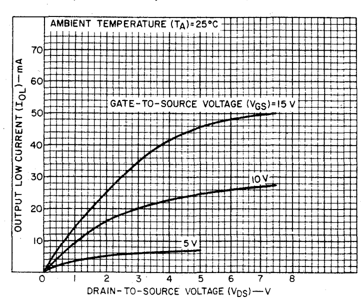


Fig.3 – Minimum low (sink) current characteristics.

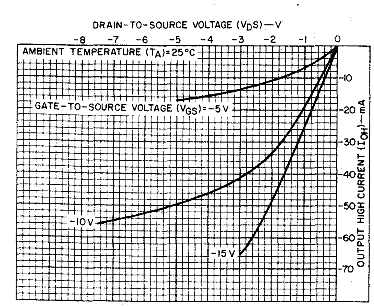


Fig.4 – Typical output high (source) current characteristics.

CD4041UB Types

STATIC ELECTRICAL CHARACTERISTICS

CHARAC-TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55,+25,+125 Apply to D, F,H Pkgs. Values at –40,+25,+85 Apply to E Pkgs.							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25 Min.	Typ.	Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	2.1	1.8	1.44	1.2	1.6	3.2	–	mA
	0.5	0,10	10	6.25	5.6	4.5	3.5	5	10	–	
	1.5	0,15	15	24	23	17	13	19	38	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–2.1	–1.8	–1.44	–1.2	–1.6	–3.2	–	
	2.5	0,5	5	–8.4	–6.7	–5.4	–4.6	–6.4	–12.8	–	
	9.5	0,10	10	–6.25	–5.6	–4.5	–3.5	–5	–10	–	
	13.5	0,15	15	–24	–23	–17	–13	–19	–38	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1				–	–	1	V
	1,9	–	10	2				–	–	2	
	1.5,13.5	–	15	2.5				–	–	2.5	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	4				4	–	–	
	1,9	–	10	8				8	–	–	
	1.5,13.5	–	15	12.5				12.5	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

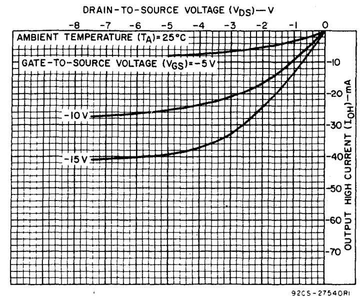


Fig.5 – Minimum output high (source) current characteristics.

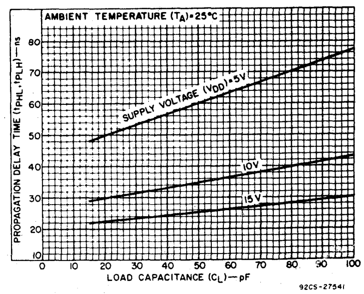


Fig.6 – Typical propagation delay time vs. load capacitance.

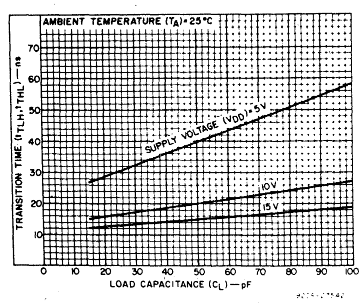


Fig.7 – Typical transition time vs. load capacitance.

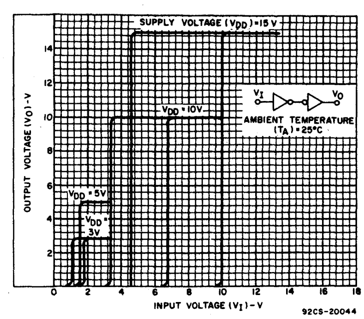


Fig.8 – Minimum and maximum transfer characteristics – true output.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, Input $t_r,t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ

CHARACTERISTIC		CONDITIONS V_{DD} Volts	ALL TYPES LIMITS Typ.	Max.	UNITS
Propagation Delay Time:	t_{PHL}, t_{PLH}	5	60	120	ns
		10	35	70	
		15	25	50	
Transition Time	t_{THL}, t_{TLH}	5	40	80	ns
		10	20	40	
		15	15	30	
Input Capacitance	C_{IN}	Any Input	15	22.5	pF

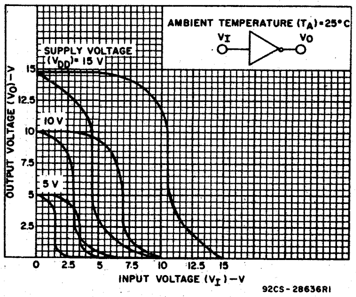


Fig.9 – Minimum and maximum transfer characteristics – complement output.

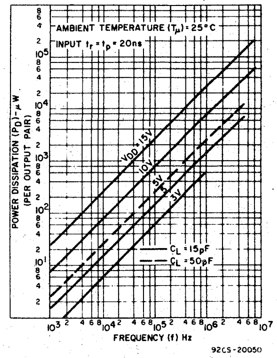


Fig.11 – Typical power dissipation vs frequency per output pair.

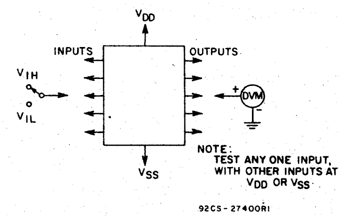


Fig.13 – Input voltage test circuit.

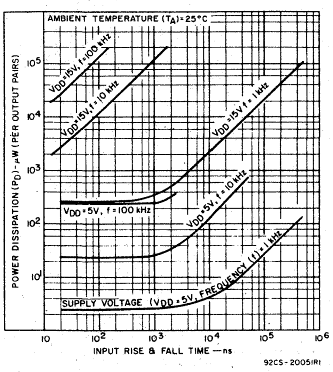


Fig.10 – Typical power dissipation vs. input rise & fall time per output pair.

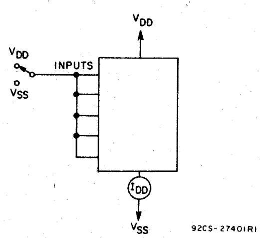


Fig.12 – Quiescent device current test circuit.

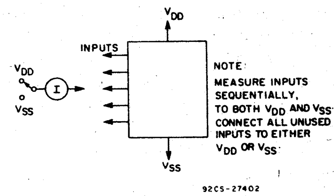
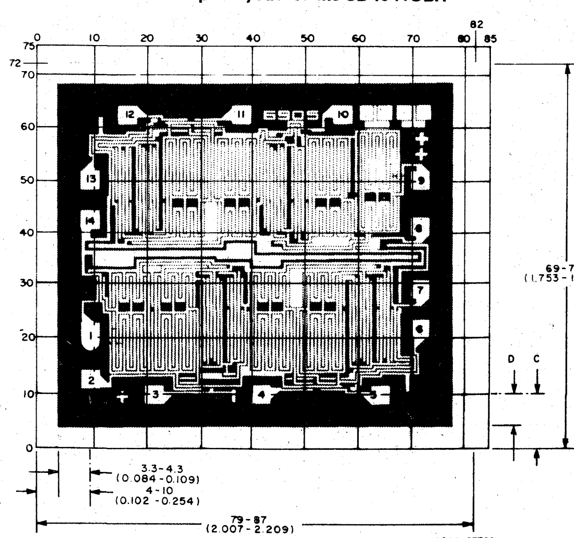


Fig.14 – Input-leakage-current test circuit.

Dimensions and pad layout for the CD4041UBH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Quad Clocked "D" Latch

High-Voltage Types (20-Volt Rating)

The RCA-CD4042B types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the n- and p-channel output devices is balanced and all outputs are electrically identical. Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

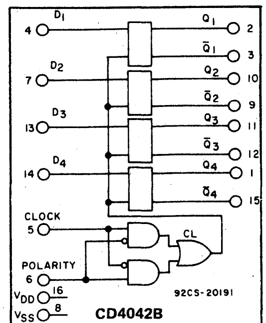
The CD4042B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

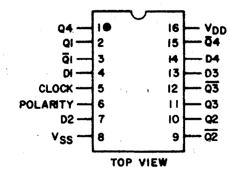
- Clock polarity control
- Q and $\overline{Q}$ outputs
- Common clock
- Low power TTL compatible
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin (over full package temperature range):
  - 1 V at V_{DD} = 5 V
  - 2 V at V_{DD} = 10 V
  - 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

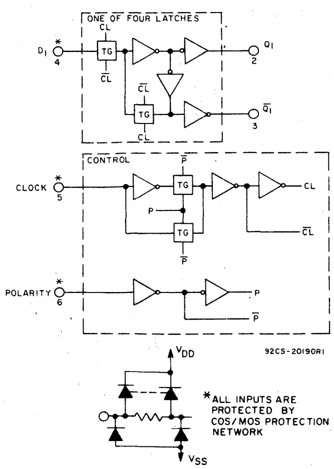
- Buffer storage
- Holding register
- General digital logic



CD4042B FUNCTIONAL DIAGRAM



TERMINAL ASSIGNMENT



CLOCK	POLARITY	Q
0	0	D
⌐ (rising)	0	LATCH
1	1	D
⌐ (falling)	1	LATCH

Fig. 1 – Logic block diagram and truth table.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D, F, H Pkgs. Values at –40,+25,+85 Apply to E Pkgs. –55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	µA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	µA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

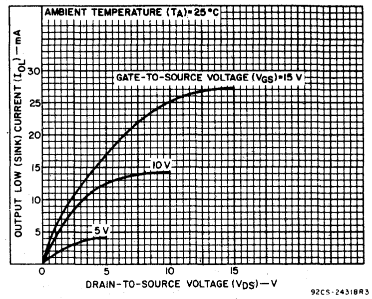


Fig. 2 – Typical output low (sink) current characteristics.

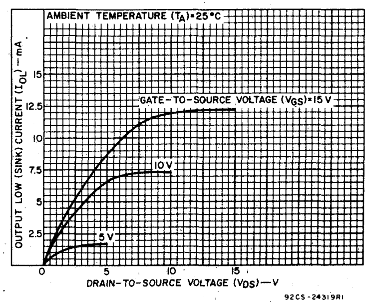


Fig. 3 – Minimum output low (sink) current characteristics.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL TYPES Min.	LIMITS ALL TYPES Max.	UNITS
Supply-Voltage Range (For T_A=Full Package Temperature Range)	—	3	18	V
Clock Pulse Width, t_W	5 10 15	200 100 60	— — —	ns
Setup Time, t_S	5 10 15	50 30 25	— — —	ns
Hold Time, t_H	5 10 15	120 60 50	— — —	ns
Clock Rise or Fall Time: t_r, t_f	5,10 15	Not rise or fall time sensitive.		μs

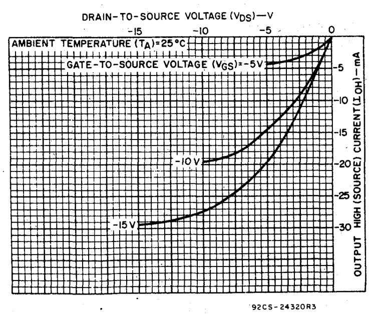


Fig. 4 – Typical output high (source) current characteristics.

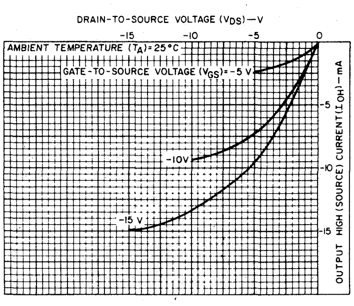


Fig. 5 – Minimum output high (source) current characteristics.

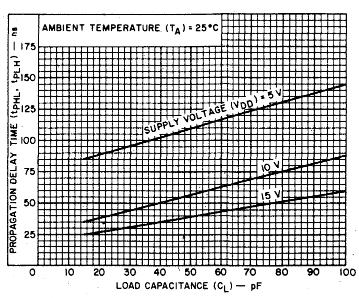


Fig. 6 – Typical propagation delay time vs. load capacitance—data to Q.

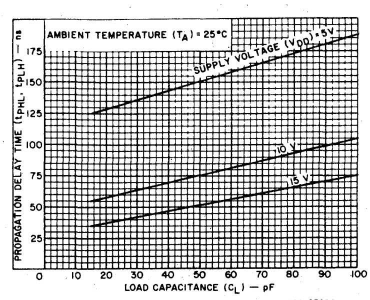


Fig. 7 – Typical propagation delay time vs. load capacitance—data to $\overline{Q}$.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL TYPES Typ.	Max.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} Data In to Q	5 10 15	110 55 40	220 110 80	ns
Data In to $\overline{Q}$	5 10 15	150 75 50	300 150 100	ns
Clock to Q	5 10 15	225 100 80	450 200 160	ns
Clock to $\overline{Q}$	5 10 15	250 115 90	500 230 180	ns
Transition Time : t_{THL}, t_{TLH}	5 10 15	100 50 40	200 100 80	ns
Minimum Clock Pulse Width, t_W	5 10 15	100 50 30	200 100 60	ns
Minimum Hold Time, t_H	5 10 15	60 30 25	120 60 50	ns
Minimum Setup Time, t_S	5 10 15	0 0 0	50 30 25	ns
Clock Input Rise or Fall Time: t_r, t_f	5,10 15	Not rise or fall time sensitive.		μS
Input Capacitance, C_{IN} (Any Input)	–	5	7.5	pF

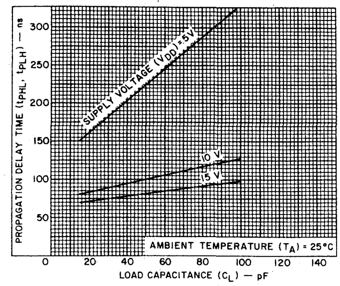


Fig. 8 – Typical propagation delay time vs. load capacitance–clock to Q

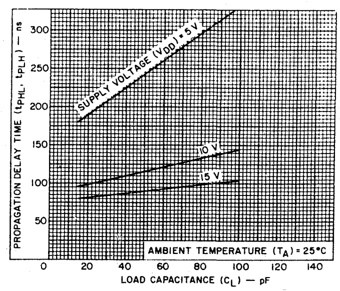


Fig. 9 – Typical propagation delay time vs. load capacitance–clock to $\overline{Q}$.

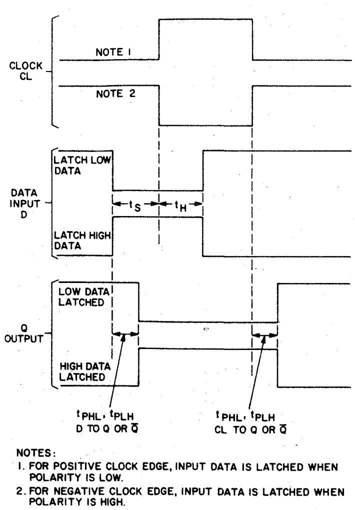


Fig. 12 – Dynamic test parameters.

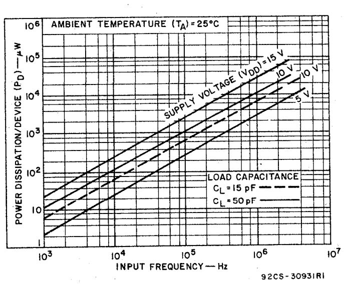


Fig. 10 – Typical power dissipation vs. frequency.

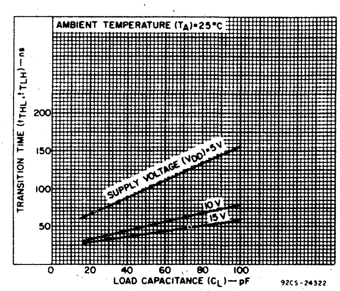


Fig. 11 – Typical transition time vs. load capacitance.

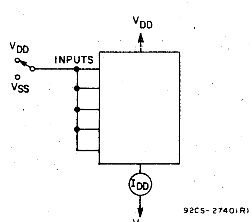


Fig. 13 – Quiescent device current test circuit.

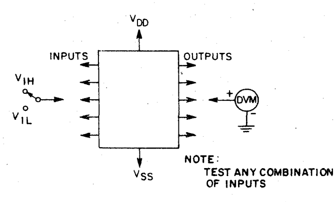


Fig. 14 – Input voltage test circuit.

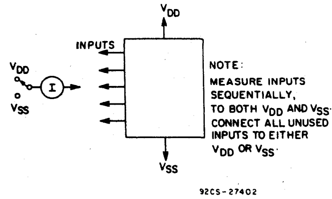
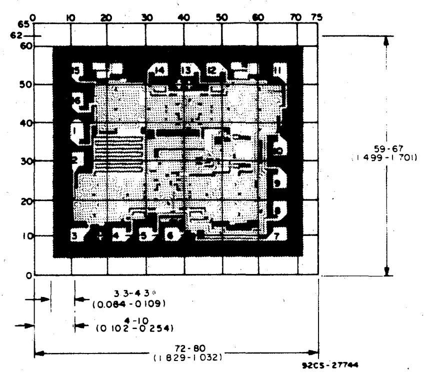


Fig. 15 – Input current test circuit.

Chip Photograph, Dimensions, and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Quad 3-State R/S Latches

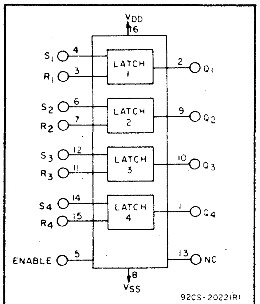
High-Voltage Types (20-Volt Rating)
Quad NOR R/S Latch – CD4043B
Quad NAND R/S Latch – CD4044B

The RCA-CD4043B types are quad cross-coupled 3-state COS/MOS NOR latches and the CD4044B types are quad cross-coupled 3-state COS/MOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or high on the ENABLE input connects the latch states to the Q outputs. A logic "0" or low on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common busing of the outputs.

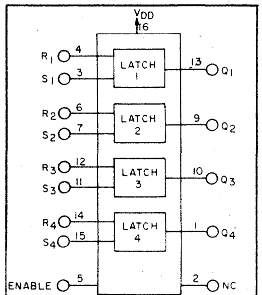
The CD4043B and CD4044B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:
- **3-state outputs with common output ENABLE**
- **Separate SET and RESET inputs for each latch**
- **NOR and NAND configurations**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:
- **Holding register in multi-register system**
- **Four bits of independent storage with output ENABLE**
- **Strobed register**
- **General digital logic**



CD4043B
FUNCTIONAL DIAGRAM



CD4044B
FUNCTIONAL DIAGRAM

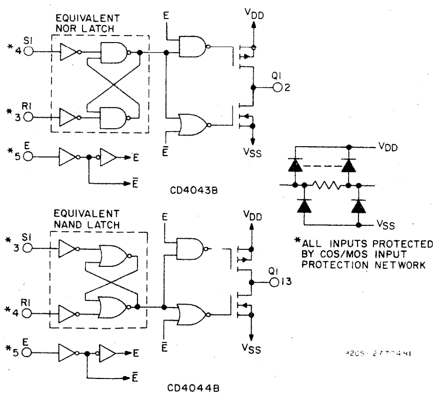
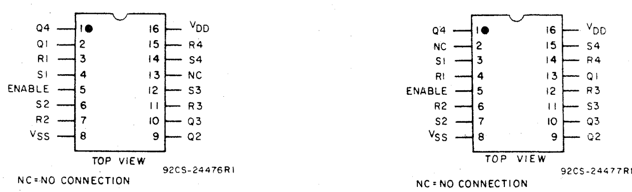


Fig. 1 – Logic diagrams.



CD4043B **TERMINAL ASSIGNMENTS** CD4044B

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . . +265°C

Recommended Operating Conditions T_A=25°C
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD} (V)	Min.	Max.	Units
Supply-Voltage Range (T_A = Full Package Temperature Range)	–	3	18	V
SET or RESET Pulse Width, t_W	5	160	–	ns
	10	80	–	
	15	40	–	

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5, 3.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm10^{-4}$	±0.4	μA

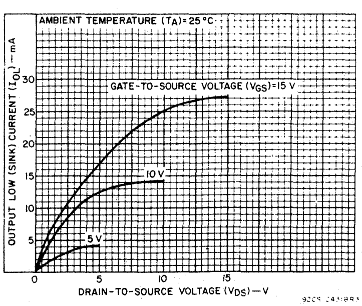


Fig. 2 – Typical output low (sink) current characteristics.

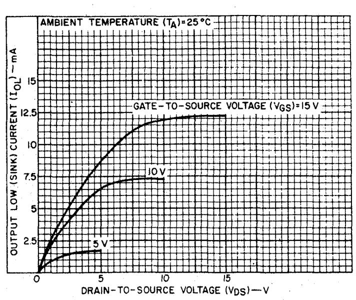


Fig. 3 – Minimum output low (sink) current characteristics.

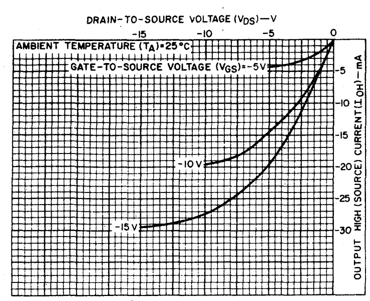


Fig. 4 – Typical output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25° C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ*

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL TYPES		UNITS
		TYP.	MAX.	
Propagation Delay Time: t_{PHL}, t_{PLH} SET or RESET to Q	5 10 15	150 70 50	300 140 100	ns
3-State Propagation Delay Time: ENABLE to Q t_{PHZ}, t_{PZH}	5 10 15	115 55 40	230 110 80	ns
t_{PLZ}, t_{PZL}	5 10 15	90 50 35	180 100 70	ns
Transition Time: t_{THL}, t_{TLH}	5 10 15	100 50 40	200 100 80	ns
Minimum SET or RESET Pulse Width, t_W	5 10 15	80 40 20	160 80 40	ns
Input Capacitance, (Any Input) C_{IN}	–	5	7.5	pF

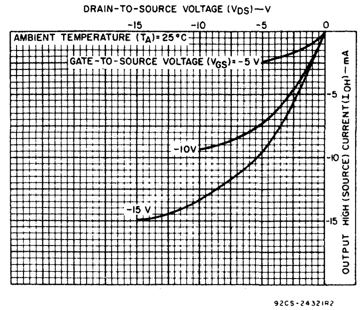


Fig. 5 – Minimum output high (source) current characteristics.

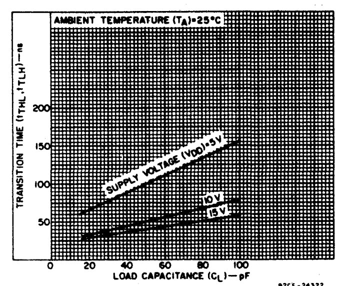


Fig. 6 – Typical transition time vs. load capacitance.

TEST CIRCUITS

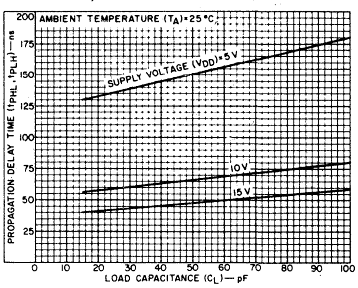


Fig. 7 – Typical propagation delay time vs. load capacitance–SET, RESET to Q, $\bar{Q}$.

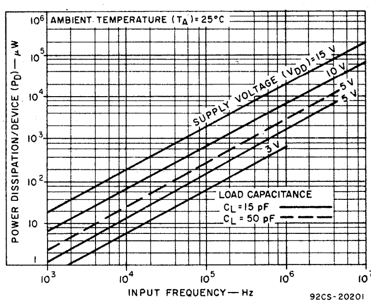


Fig. 8 – Typical power dissipation vs. frequency.

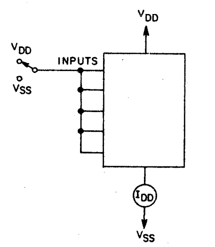


Fig. 9 – Quiescent device current.

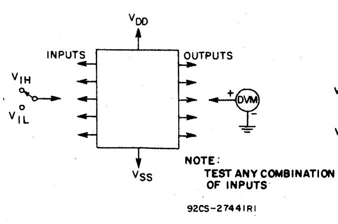


Fig. 10 – Input voltage.

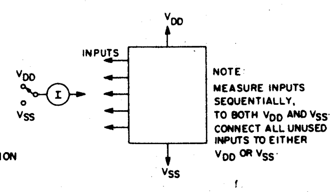


Fig. 11 – Input current.

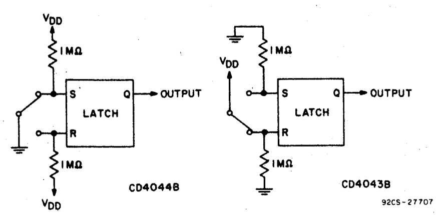
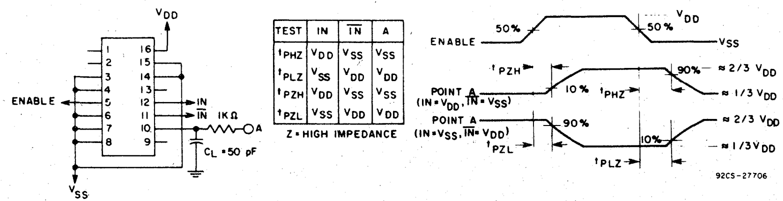


Fig. 12 – Switch bounce eliminator.

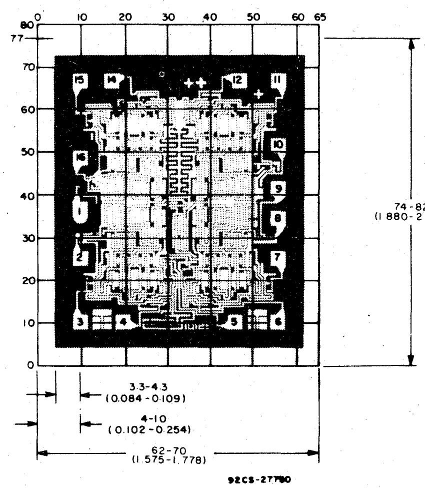


TEST	IN	$\overline{IN}$	A
t_{PHZ}	V_{DD}	V_{SS}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}	V_{DD}
t_{PZH}	V_{DD}	V_{SS}	V_{SS}
t_{PZL}	V_{SS}	V_{DD}	V_{DD}

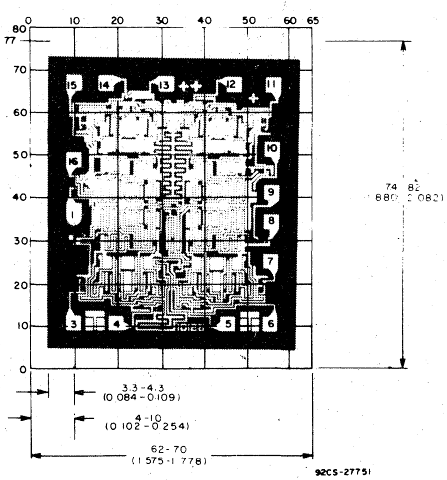
Z = HIGH IMPEDANCE

Fig. 13 – ENABLE propagation delay time test circuit and waveforms.

CHIP PHOTOGRAPHS DIMENSIONS AND PAD LAYOUTS



CD4043BH



CD4044BH

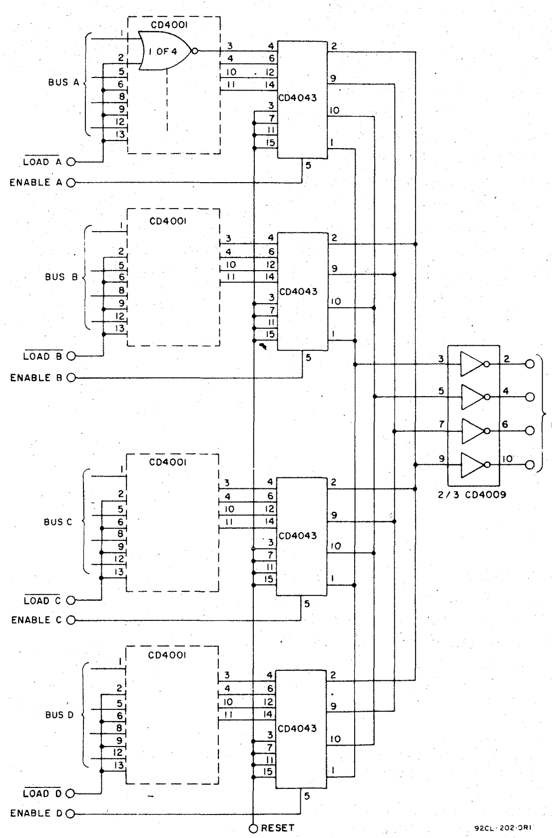


Fig. 14 – Multiple bus storage.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS 21-Stage Counter

High-Voltage Types (20-Volt Rating)

The RCA-CD4045B is a timing circuit consisting of 21 counter stages, two output-shaping flip-flops, two inverter output drivers, and input inverters for use in a crystal oscillator. The CD4045B configuration provides 21 flip-flop counting stages, and two flip-flops for shaping the output waveform for a 3.125% duty cycle. Push-pull operation is provided by the inverter output drivers.

The first inverter is intended for use as a crystal oscillator/amplifier. However, it may be used as a normal logic inverter if desired. A crystal oscillator circuit can be made less sensitive to voltage-supply variations by the use of source resistors. In this device, the sources of the p and n transistors have been brought out to package terminals. If external resistors are not required, the sources must be shorted to their respective substrates (S_p to V_{DD}, S_n to V_{SS}). See Fig. 1. The first inverter in conjunction with an outboard inverter, such as 1/6 CD4069, and R_X, C_X, and R_S can also be used to construct an RC oscillator. The following data is supplied as a guide in the selection of values for R_X, R_S, and C_X used in Fig. 11:

1. R_X max = 10 MΩ with R_S = 10 MΩ and C_X = 50 pF
2. C_X max = 25 μF with R_S = 560 kΩ and R_X = 50 kΩ

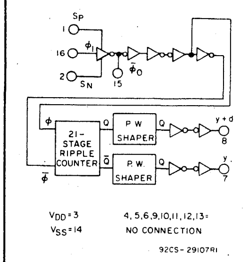
The CD4045B types are supplied in 16-lead dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

- **Digital equipment in which ultra-low dissipation and/or operation using a battery source is required.**
- **Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs at various intervals in the counting sequence.**
- **Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.**

Features:

- **Very low operating dissipation . . . . .**
  <1 mW (typ.) @ V_{DD} = 5 V, fϕ = 1 MHz
- **Output drivers with sink or source capability . . . . .**
  7 mA (typ.) @ V_{DD} = 5 V
- **Medium speed (typ.) . . . fϕ = 25 MHz @ V_{DD} = 10 V**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, Standard Specifications for Descripiton of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

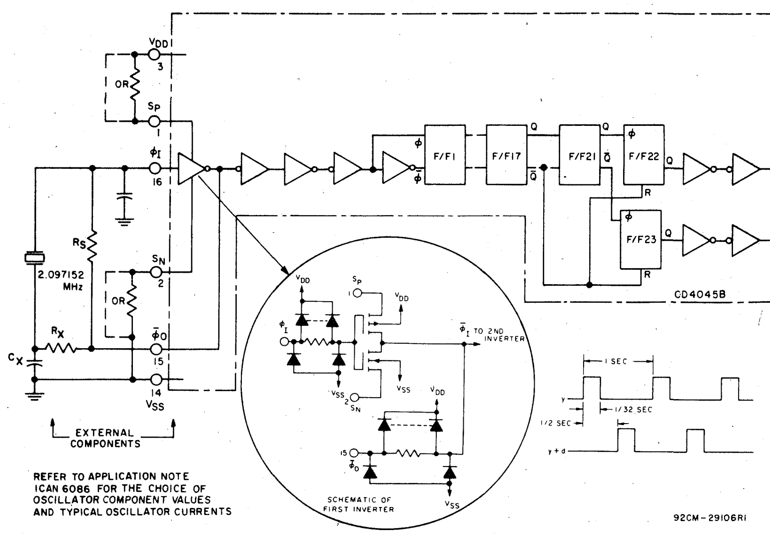


Fig. 1 — CD4045B and outboard components in a typical 21-stage counter application.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55,+25,+125 Apply to D,F,H Packages Values at −40,+25,+85, Apply to E Package −55	−40	+85	+125	+25 Min.	Typ.	Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	4.5	4.3	2.9	2.5	3.6	7	–	mA
	0.5	0,10	10	11.2	10.5	7.7	6.3	9.1	18	–	
	1.5	0,15	15	29.4	28	19.6	16.8	23.8	47	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−4.5	−4.3	−2.9	−2.5	−3.6	−7	–	
	9.5	0,10	10	−11.2	−10.5	−7.7	−6.3	−9.1	−18	–	
	13.5	0,15	15	−29.4	−28	−19.6	−16.8	−23.8	−47	–	
Pin 15 Output, Low and High Current, I_{OL}, I_{OH}	0.4,4.6	0,5	5	–				±0.1	±0.18	–	mA
	0.5,9.5	0,10	10	–				±0.2	±0.3	–	
	1.5,13.5	0,15	15	–				±0.5	±1	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	–	0.05	V
	–	0,10	10	0.05				–	–	0.05	
	–	0,15	15	0.05				–	–	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	–	3	18	V
Minimum Input-Pulse Width, t_W	5	–	100	ns
	10	–	50	
	15	–	40	
Maximum Input–Pulse Frequency, $f\phi$ (External Pulse Source)	5	5	–	MHz
	10	12	–	
	15	15	–	

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} V	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time: ϕ_I to y or y+d out t_{PHL}, t_{PLH}		5	–	2.2	5.5	μs
		10	–	0.9	2.7	
		15	–	0.65	2	
Transition Time: t_{THL}, t_{TLH}		5	–	25	50	ns
		10	–	13	25	
		15	–	10	20	
Minimum Input-Pulse Width t_W		5	–	50	100	
		10	–	25	50	
		15	–	20	40	
Input-Pulse Rise or Fall Time: $t_r\phi$, $t_f\phi$		5	–	–	500	μs
		10	–	–	500	
		15	–	–	500	
Maximum Input-Pulse Frequency: (External Pulse Source) f_ϕ		5	5	10	–	MHz
		10	12	25	–	
		15	15	30	–	
Input Capacitance, C_{IN}	Any Input		–	5	7.5	pF
Variation of Output Frequency (Unit-to-Unit)	f = 5 MHz	5	–	0.05	–	%
		10	–	0.03	–	
		15	–	0.1	–	
RC Oscillator Operation						
Maximum Oscillator Frequency (See Fig. 11) f_{osc}	R_X = 50 kΩ,	5	45	60	75	kHz
	R_S = 560 kΩ,	10	45	60	75	
	C_X = 50 pF	15	45	60	75	

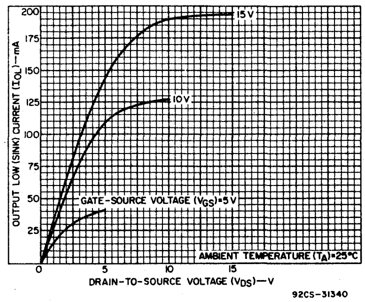


Fig. 2 – Typical output low (sink) current characteristics.

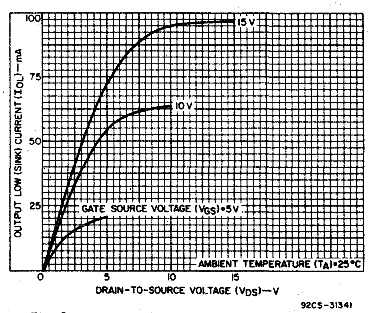


Fig. 3 – Minimum output low (sink) current characteristics.

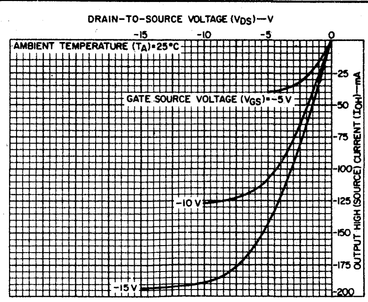


Fig. 4 – Typical output high (source) current characteristics.

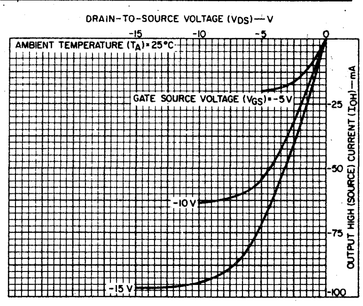


Fig. 5 – Minimum output high (source) characteristics.

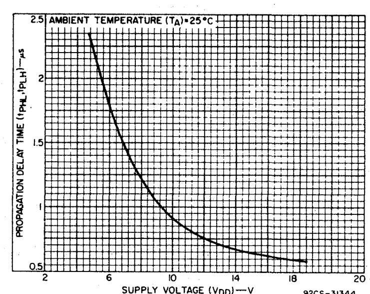


Fig. 6 – Typical propagation delay time as a function of supply voltage (ϕ_I to y or y+d out vs. V_{DD}).

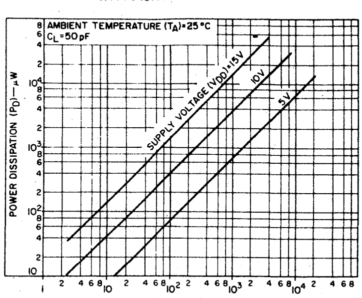


Fig. 7 – Typical power dissipation as a function of input frequency (21 counting stages).

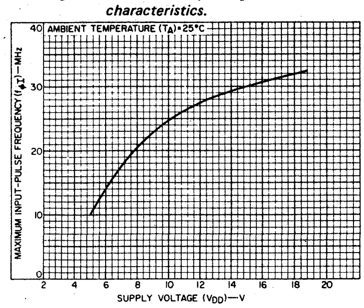


Fig. 8 – Typical maximum input-pulse frequency as a function of supply voltage.

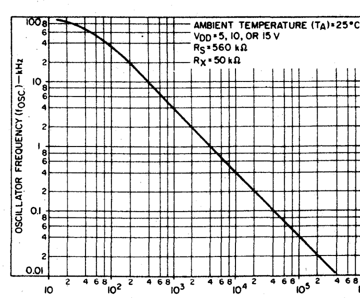


Fig. 9 – Typical RC oscillator frequency as a function of capacitance (C_X), See Fig. 11.

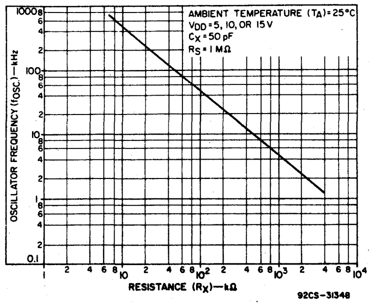


Fig. 10 – Typical RC oscillator frequency as a function of resistance (R_X), See Fig. 11.

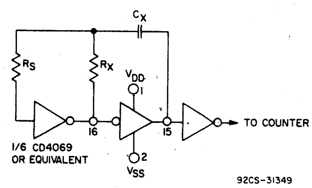


Fig. 11 – Typical RC circuit.

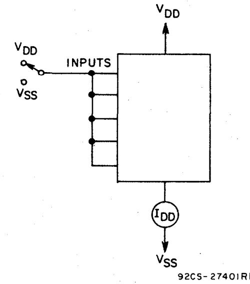


Fig. 12 – Quiescent-device-current test circuit.

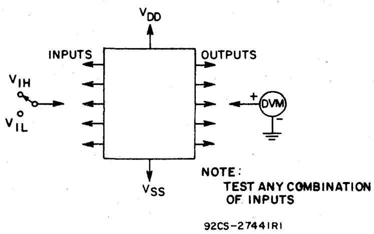


Fig. 13 – Noise-immunity test circuit.

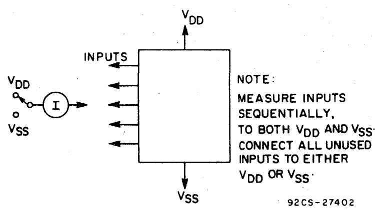


Fig. 14 – Input-leakage-current test circuit.

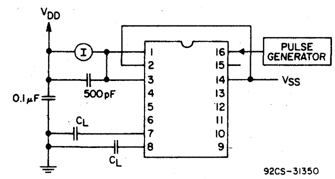
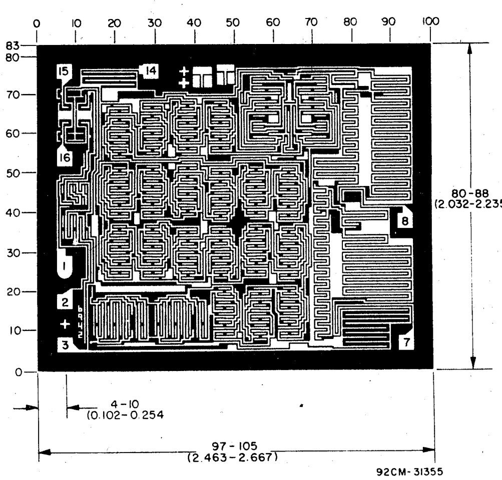


Fig. 15 – Dynamic power dissipation test circuit.

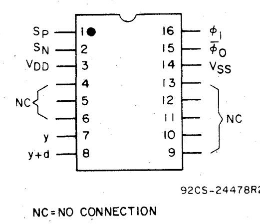


Dimensions and pad layout for CD4045B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

TERMINAL DIAGRAM
Top View



NOTE Observe power-supply terminal connections, V_{DD} is terminal No. 3 and V_{SS} is terminal No. 14 (not 16 and 8 respectively, as in other CD4000B Series 16-lead devices).

CD4046B Types

COS/MOS Micropower Phase-Locked Loop

The RCA-CD4046B COS/MOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2-V zener diode is provided for supply regulation if necessary.

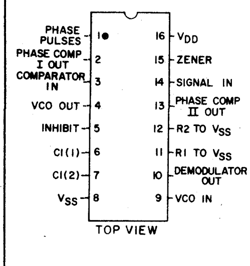
The CD4046B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\Omega$) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R_S) of 10 kΩ or more should be connected from this terminal to V_{SS}. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full COS/MOS logic swing is available at the output of the VCO and allows direct coupling to COS/MOS frequency dividers such as the RCA-CD4024, CD4018, CD4020, CD4022, CD4029, and CD4059. One or more CD4018 (Presettable Divide-by-N Counter) or CD4029 (Presettable Up/Down Counter), or CD4059A (Programmable Divide-by-"N" Counter), together with the CD4046B (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

Features:

- Very low power consumption: 70 μW (typ.) at VCO f_o = 10 kHz, V_{DD} = 5 V
- Operating frequency range up to 1.4 MHz (typ.) at V_{DD} = 10 V, RI = 5 kΩ
- Low frequency drift: 0.04%/°C (typ.) at V_{DD} = 10 V
- Choice of two phase comparators:
  Exclusive-OR network (I)
  Edge-controlled memory network with phase-pulse output for lock indication (II)
- High VCO linearity: <1% (typ.) at V_{DD} = 10 V
- VCO inhibit control for ON-OFF keying and ultra-low standby power consumption
- Source-follower output of VCO control input (Demod. output)
- Zener diode to assist supply regulation
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A,"Standard Specifications for Description of 'B' Series CMOS Devices"



TERMINAL ASSIGNMENT

Applications:

- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discriminator
- Data synchronization
- Voltage-to-frequency conversion
- Tone decoding
- FSK – Modems
- Signal conditioning
- (See ICAN-6101) "RCA COS/MOS Phase-Locked Loop – A Versatile Building Block for Micropower Digital and Analog Applications"

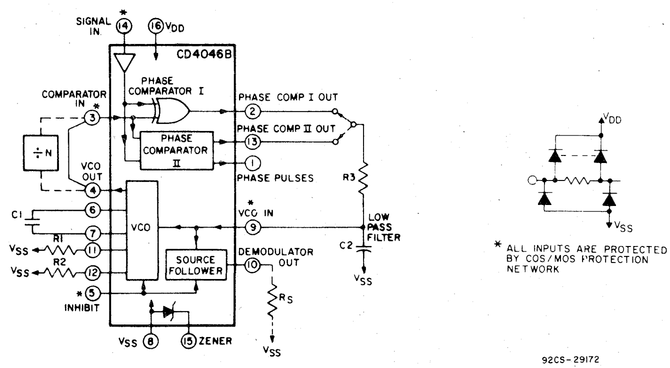


Fig.1 – COS/MOS phase-locked loop block diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	–0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F,)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	–55 to +125°C
PACKAGE TYPE E	–40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	–65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within COS/MOS logic levels [logic "0" ≤30% (V_{DD}–V_{SS}), logic "1" ≥ 70% (V_{DD}–V_{SS})]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase comparator I is an exclusive-OR network; it operates analagously to an over-driven balanced mixer. To maximize the lock range, the signal- and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to V_{DD}/2. The low-pass filter connected to the output of phase comparator

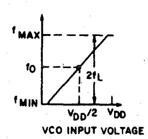
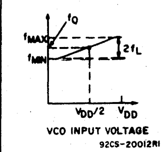
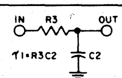
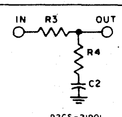
RECOMMENDED OPERATING CONDITIONS at T_A = Full Package-Temperature Range
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range VCO Section:			V
As Fixed Oscillator	3	18	
Phased-Lock-Loop Operation	5	18	
Supply-Voltage Range Phase Comparator Section:			
Comparators	3	18	
VCO Operation	5	18	

DESIGN INFORMATION

This information is a guide for approximating the values of external components for the CD4046A in a Phase-Locked-Loop system.

The selected external components must be within the following ranges:
$5\ k\Omega \leq R1, R2, R_S \leq 1\ M\Omega$
$C1 \geq 100$ pF at $V_{DD} \geq 5$ V;
$C1 \geq 50$ pF at $V_{DD} \geq 10$ V

Characteristics	Phase Comparator Used	Design Information: VCO WITHOUT OFFSET $R_2 = \infty$	Design Information: VCO WITH OFFSET
VCO Frequency	1		
	2	Same as for No.1	
For No Signal Input	1	VCO will adjust to center frequency, f_o	
	2	VCO will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2\ f_L$	1	$2\ f_L$ = full VCO frequency range	
		$2\ f_L = f_{max} - f_{min}$	
	2	Same as for No.1	
Frequency Capture Range, $2\ f_C$	1		(1), (2) $2\ f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau 1}}$
Loop Filter Component Selection			For $2\ f_C$, see Ref. (2)
	2	$f_C = f_L$	
Phase Angle Between Signal and Comparator	1	90° at center frequency (f_o) approximating 0° and 180° at ends of lock range ($2\ f_L$)	
	2	Always 0° in lock	
Locks On Harmonic of Center Frequency	1	Yes	
	2	No	
Signal Input Noise Rejection	1	High	
	2	Low	

For further information, see

(1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York, 1966
(2) G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_o).

The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ($2f_C$).

The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2f_L$). The capture range is ≤ the lock range.

With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. 2 shows the typical, triangular, phase-to-output response characteristic of phase-comparator I. Typical waveforms for a COS/MOS phase-locked-loop employing phase comparator I in locked condition of f_o is shown in Fig. 3.

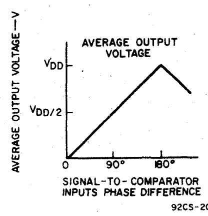


Fig.2 – Phase-comparator I characteristics at low-pass filter output.

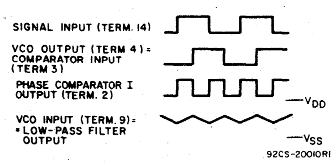


Fig.3 – Typical waveforms for COS/MOS phase-locked loop employing phase comparator I in locked condition of f_o.

Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURE (°C) Values at −55, +25, +125 Apply to D,F,H Packages; Values at −40, +25, +85 Apply to E Package −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
VCO Section											
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0.15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	Term. 4 driving CMOS	0,5	5	0.05				–	0	0.05	V
		0,10	10	0.05				–	0	0.05	
		0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	e.g. Term.3	0,5	5	4.95				4.95	5	–	
		0,10	10	9.95				9.95	10	–	
		0,15	15	14.95				14.95	15	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	µA
Phase Comparator Section											
Total Device Current, I_{DD} Max. Term. 14 open, Term. 5 = V_{DD}	–	0,5	5	0.1				–	0.05	0.1	mA
	–	0,10	10	0.5				–	0.25	0.5	
	–	0,15	15	1.5				–	0.75	1.5	
	–	0,20	20	4				–	2	4	
Term. 14 = V_{SS} or V_{DD}, Term. 5 = V_{DD}	–	0,5	5	20				–	10	20	µA
	–	0,10	10	40				–	20	40	
	–	0,15	15	80				–	40	80	
	–	0,20	20	160				–	80	160	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
DC-Coupled Signal Input and Comparator Input Voltage Sensitivity Low Level V_{IL} Max.	0.5,4.5	–	5			1.5		–	–	1.5	V
	1,9	–	10			3		–	–	3	
	1.5,13.5	–	15			4		–	–	4	
High Level V_{IH} Min.	0.5,4.5	–	5			3.5		3.5	–	–	
	1,9	–	10			7		7	–	–	
	1.5,13.5	–	15			11		11	–	–	

control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal- and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURE (°C) Values at −55, +25, +125 Apply to D,F,H Packages; Values at −40, +25, +85 Apply to E Package: −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Phase Comparator Section (cont'd)											
Input Current I_{IN} Max. (except Term. 14)	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA
3-State Leakage Current, I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm10^{-4}$	±0.4	μA

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS		V_{DD} (V)	LIMITS ALL TYPES Min.	Typ.	Max.	UNITS
VCO Section							
Operating Power Dissipation, P_D	f_o = 10 kHz, $R_2 = \infty$	R_1 = 1 MΩ, $VCO_{IN} = \frac{V_{DD}}{2}$	5	–	70	140	μW
			10	–	800	1600	
			15	–	3000	6000	
Maximum Operating Frequency f_{max}	C_1=50 pF, $R_2 = \infty$, $VCO_{IN}=V_{DD}$	R_1 = 10 kΩ	5	0.3	0.6	–	MHz
			10	0.6	1.2	–	
			15	0.8	1.6	–	
	C_1 = 50 pF, $R_2 = \infty$, $VCO_{IN}=V_{DD}$	R_1 = 5 kΩ	5	0.5	0.8	–	
			10	1	1.4	–	
			15	1.4	2.4	–	
Center Frequency (f_o) and Frequency Range ($f_{max}-f_{min}$)	Programmable with external components R1, R2, and C1 *See Design Information*						
Linearity	VCO_{IN} = 2.5 V ± 0.3V,	R_1=10 kΩ	5	–	1.7	–	%
	=5 V ± 1 V,	= 100 kΩ	10	–	0.5	–	
	=5 V ± 2.5 V,	=400 kΩ	10	–	4	–	
	=7.5 V ± 1.5 V,	= 100 kΩ	15	–	0.5	–	
	= 7.5 V ± 5 V,	= 1 MΩ	15	–	7	–	
Temperature-Frequency Stability: No Frequency Offset f_{MIN} = 0			5	–	±0.12	–	%/°C
			10	–	±0.04	–	
			15	–	±0.015	–	
Frequency Offset $f_{MIN} \neq 0$			5	–	±0.09	–	
			10	–	±0.07	–	
			15	–	±0.03	–	
Output Duty Cycle			5,10,15	–	50	–	%
Output Transition Times, t_{THL}, t_{TLH}			5	–	100	200	ns
			10	–	50	100	
			15	–	40	80	

the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. 10 shows typical waveforms for a COS/MOS PLL employing phase comparator II in a locked condition.

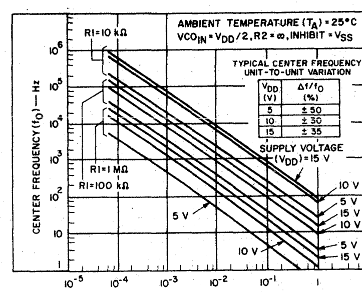


Fig. 4 – Typical center frequency as a function of C1 and R1 at V_{DD} = 5 V, 10 V, and 15 V.

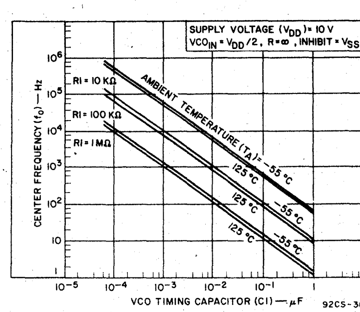


Fig. 5 – Center frequency as a function of C1 and R1 for ambient temperatures of −55°C to 125°C.

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS ALL TYPES Min.	Typ.	Max.	UNITS
VCO Section (cont'd)						
Source-Follower Output (Demodulated Output): Offset Voltage ($VCO_{IN}-V_{DEM}$)	$R_S > 10\ k\Omega$	5 10 15	– – –	1.8 1.8 1.8	2.5 2.5 2.5	V
Linearity	R_S=100 kΩ, VCO_{IN} = 2.5±0.3 V = 300 kΩ, = 5±2.5 V = 500 kΩ, = 7.5± 5 V	5 10 15	– – –	0.3 0.7 0.9	– – –	%
Zener Diode Voltage (V_Z)	I_Z = 50 μA		4.45	5.5	6.15	V
Zener Dynamic Resistance, R_Z	I_Z = 1 mA		–	40	–	Ω
Phase Comparator Section						
Term. 14 (SIGNAL IN) Input Resistance R_{14}		5 10 15	1 0.2 0.1	2 0.4 0.2	– – –	MΩ
AC Coupled Signal Input Voltage Sensitivity* (peak-to-peak)	f_{IN} = 100 kHz, sine wave	5 10 15	– – –	180 330 900	360 660 1800	mV
Propagation Delay Times, Terms. 14 to 13: High to Low Level, t_{PHL}		5 10 15	– – –	225 100 65	450 200 130	ns
Low to High Level, t_{PLH}		5 10 15	– – –	350 150 100	700 300 200	ns
3-State Propagation Delay Times, Terms. 14 to 13: High Level to High Impedance, t_{PHZ}		5 10 15	– – –	225 100 95	450 200 190	ns
Low Level to High Impedance, t_{PLZ}		5 10 15	– – –	285 130 95	570 260 190	ns
Input Rise or Fall Times, t_r, t_f Comparator Input, Term. 3	See Fig. 5 for Phase Comp. II output loading	5 10 15	– – –	– – –	50 1 0.3	μs
Signal Input, Term. 14		5 10 15	– – –	– – –	500 20 2.5	μs
Output Transition Times, t_{THL}, t_{TLH}		5 10 15	– – –	100 50 40	200 100 80	ns

*For sine wave, the frequency must be greater than 10 kHz for Phase-Comparator II.

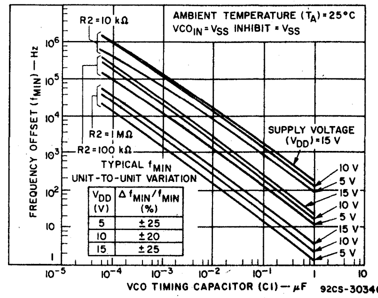


Fig. 6 – Typical frequency offset as a function of C1 and R2 for V_{DD} = 5 V, 10 V, and 15 V.

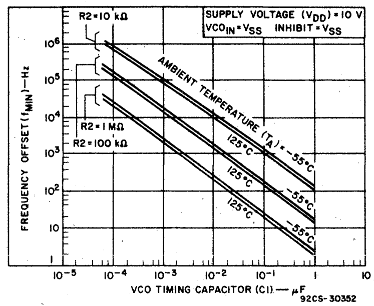


Fig. 7 – Frequency offset as a function of C1 and R2 for ambient temperatures of –55°C to 125°C.

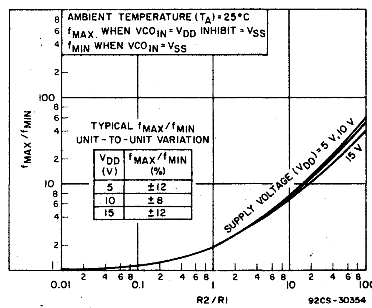


Fig. 8 – Typical f_{MAX}/f_{MIN} as a function of R2/R1.

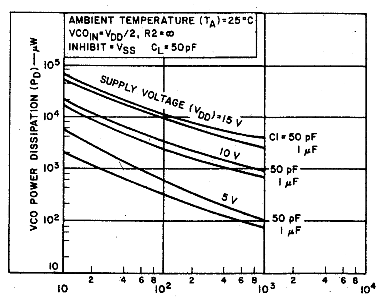


Fig. 9 – Typical VCO power dissipation at center frequency as a function of R1.

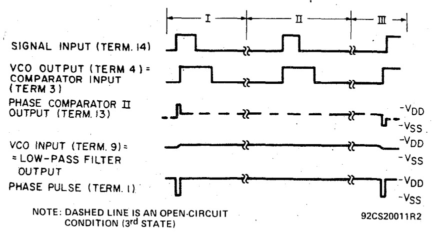


Fig. 10 – Typical waveforms for COS/MOS phase-locked loop employing phase comparator II in locked condition.

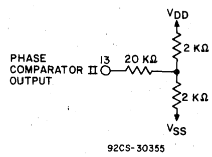


Fig. 11 – Phase comparator II output loading circuit.

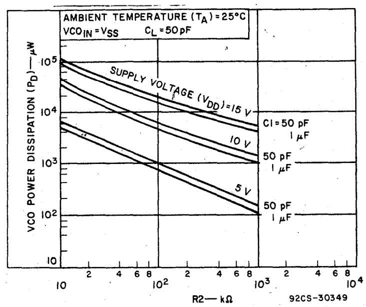


Fig. 12 – Typical VCO power dissipation at f_{MIN} as a function of R2.

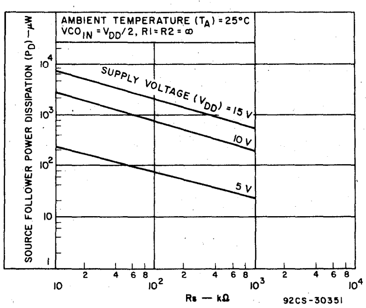


Fig. 13 – Typical source follower power dissipation as a function of Rs.

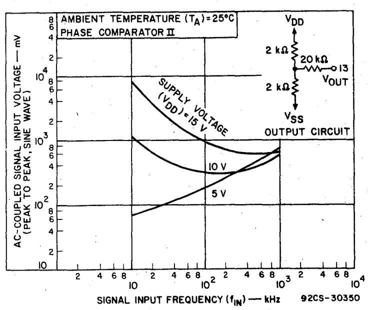


Fig. 14 – AC-coupled signal input voltage as a function of signal input frequency.

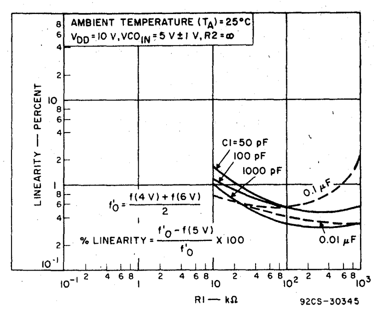


Fig. 15 – Typical VCO linearity as a function of R1 and C1 at V_{DD} = 10 V.

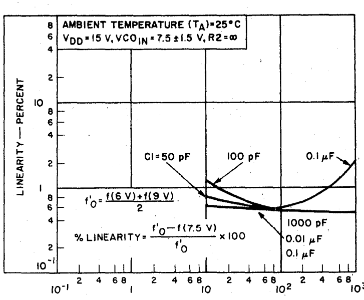
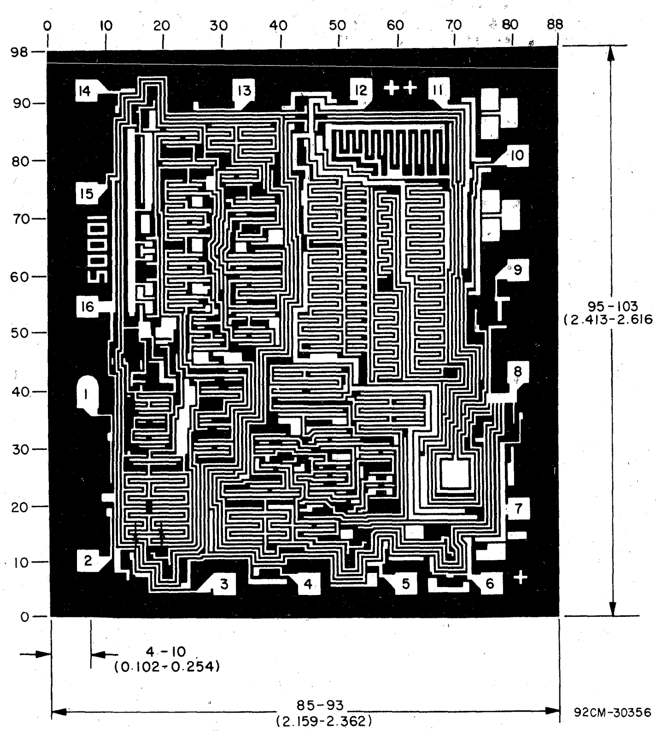


Fig. 16 – Typical VCO linearity as a function of R1 and C1 at V_{DD} = 15 V.



Dimensions and pad layout for CD4046BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Low-Power Monostable/Astable Multivibrator

High Voltage Types (20-Volt Rating)

The RCA-CD4047B consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options.

Inputs include +TRIGGER, −TRIGGER, ASTABLE, $\overline{ASTABLE}$, RETRIGGER, and EXTERNAL RESET. Buffered outputs are Q, Q, and OSCILLATOR. In all modes of operation, and external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.

Astable operation is enabled by a high level on the ASTABLE input or a low level on the $\overline{ASTABLE}$ input, or both. The period of the square wave at the Q and $\overline{Q}$ Outputs in this mode of operation is a function of the external components employed. "True" input pulses on the ASTABLE input or "Complement" pulses on the $\overline{ASTABLE}$ input allow the circuit to be used as a gatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output.

The CD4047B triggers in the monostable mode when a positive-going edge occurs on the +TRIGGER-input while the −TRIGGER is held high. Input pulses may be of any duration relative to the output pulse.

If retrigger capability is desired, the RETRIGGER input is pulsed. The retriggerable mode of operation is limited to positive-going edge. The CD4047B will retrigger as long as the RETRIGGER-input is high, with or without transitions (See Fig. 34).

An external countdown option can be implemented by coupling "Q" to an external "N" counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{ASTABLE}$ input and has a duration equal to N times the period of the multivibrator.

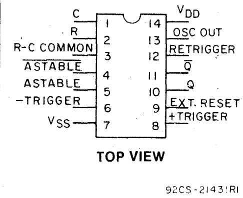
A high level on the EXTERNAL RESET input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time, for monostable operation, whenever V_{DD} is applied, an internal power-on reset circuit will clock the Q output low within one output period (t_M).

The CD4047B-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:
- *Low power consumption: special COS/MOS oscillator configuration*
- *Monostable (one-shot) or astable (free-running) operation*
- *True and complemented buffered outputs*
- *Only one external R and C required*
- *Buffered inputs*
- *100% tested for quiescent current at 20 V*
- *Standardized, symmetrical output characteristics*
- *5-V, 10-V, and 15-V parametric ratings*
- *Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"*

Monostable Multivibrator Features:
- *Positive- or negative-edge trigger*
- *Output pulse width independent of trigger pulse duration*
- *Retriggerable option for pulse width expansion*
- *Internal power-on reset circuit*
- *Long pulse widths possible using small RC components by means of external counter provision*
- *Fast recovery time essentially independent of pulse width*
- *Pulse-width accuracy maintained at duty cycles approaching 100%*

Astable Multivibrator Features:
- *Free-running or gatable operating modes*
- *50% duty cycle*
- *Oscillator output available*
- *Good astable frequency stability:*
  Frequency deviation:
  = ±2% + 0.03%/°C @ 100 kHz
  = ±0.5% +0.015%/°C @ 10 kHz
  (circuits "trimmed" to frequency V_{DD} = 10 V ± 10%)



Terminal Diagram

Applications:

Digital equipment where low-power dissipation and/or high noise immunity are primary design requirements:
- *Envelope detection*
- *Frequency multiplication*
- *Frequency division*
- *Frequency discriminators*
- *Timing circuits*
- *Time-delay applications*

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V
NOTE: IF AT 15 V OPERATION A 10 MΩ RESISTOR IS USED THE OPERATING TEMPERATURE SHOULD BE BETWEEN −25°C and 100°C			

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal) .... −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT .... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D,F) .... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) .... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D,F,H .... −55 to +125°C
PACKAGE TYPE E .... −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max .... +265°C

CD4047B FUNCTIONAL TERMINAL CONNECTIONS
NOTE: IN ALL CASES EXTERNAL RESISTOR BETWEEN TERMINALS 2 AND 3▲
EXTERNAL CAPACITOR BETWEEN TERMINALS 1 AND 2▲

FUNCTION	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
	TO V_{DD}	TO V_{SS}	INPUT TO		
Astable Multivibrator:					
Free Running	4,5,6,14	7,8,9,12	—	10,11,13	t_A (10,11) = 4.40 RC
True Gating	4,6,14	7,8,9,12	5	10,11,13	t_A (13) = 2.20 RC#
Complement Gating	6,14	5,7,8,9,12	4	10,11,13	
Monostable Multivibrator:					
Positive-Edge Trigger	4,14	5,6,7,9,12	8	10,11	
Negative-Edge Trigger	4,8,14	5,7,9,12	6	10,11	t_M (10,11) = 2.48 RC
Retriggerable	4,14	5,6,7,8,9	12	10,11	
External Countdown*	14	5,6,7,8,9,12	—	10,11	

▲ See Text.

First positive ½ cycle pulse-width = 2.48 RC, see Note on Page 10.

* Input Pulse to Reset of External Counting Chip External Counting Chip Output To Terminal 4

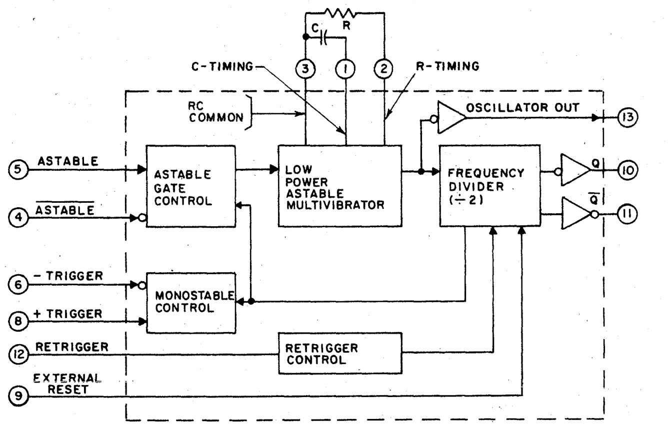


Fig. 1—CD4047B logic block diagram.

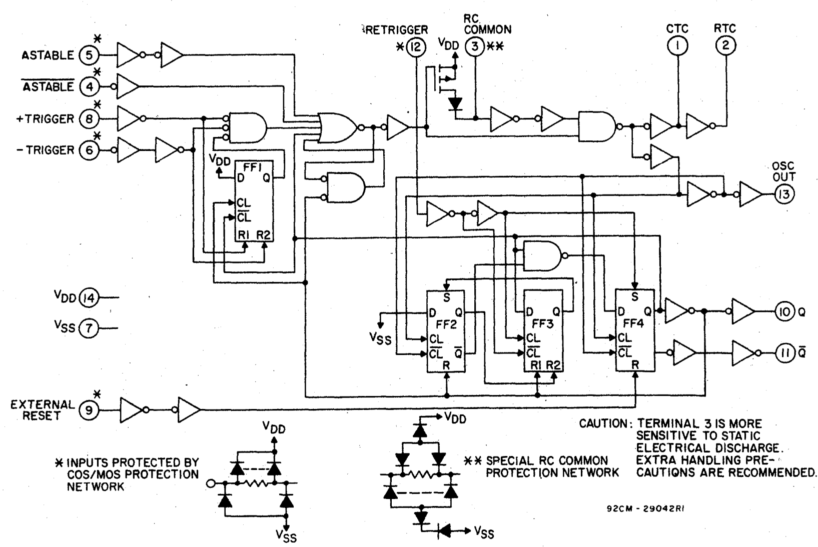


Fig. 2—CD4047B logic diagram.

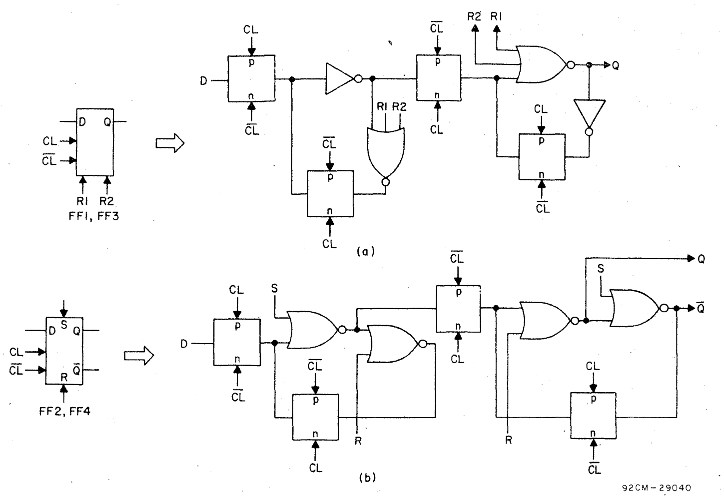


Fig. 3—Detail logic diagram for flip-flops FF1 and FF3 (a) and for flip-flops FF2 and FF4 (b).

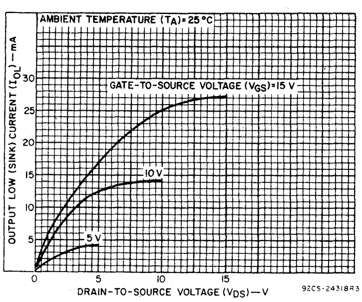


Fig. 4—Typical output low (sink) current characteristics.

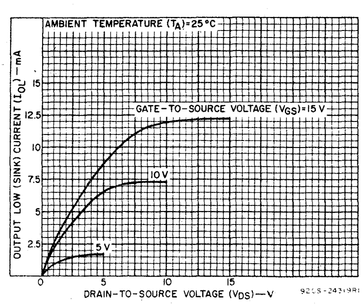


Fig. 5—Minimum output low (sink) current characteristics.

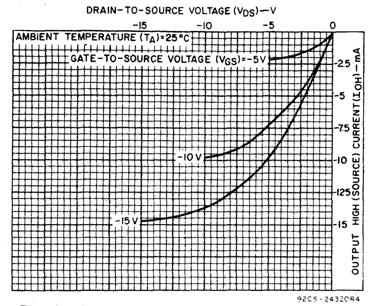


Fig. 6—Typical output high (source) current characteristics.

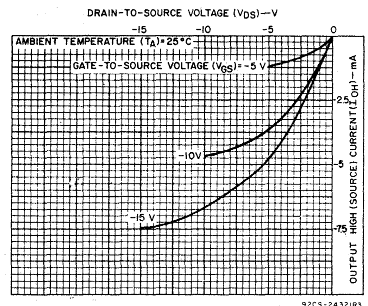


Fig. 7—Minimum output high (source) current characteristics.

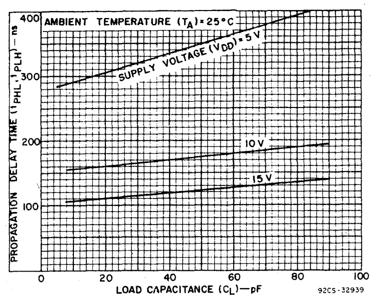


Fig. 8—Typical propagation delay time as a function of load capacitance (Astable, $\overline{\text{Astable}}$ to Q, $\overline{Q}$).

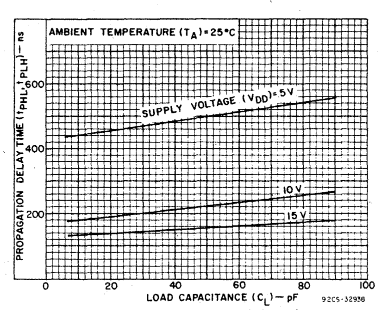


Fig. 9—Typical propagation delay time as a function of load capacitance (+ or – trigger to Q, $\overline{Q}$).

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D,F,H Packages Values at -40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	—	0,5	5	1	1	30	30	—	0.02	1	μA
	—	0,10	10	2	2	60	60	—	0.02	2	
	—	0,15	15	4	4	120	120	—	0.02	4	
	—	0,20	20	20	20	600	600	—	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	—	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	—	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	—	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	—	
Output Voltage: Low-Level V_{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	

STATIC ELECTRICAL CHARACTERISTICS (CONTINUED)

CHARACTERISTICS	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D,F,H Packages Values at -40, +25, +85 Apply to E Package −55	−40	+85	+125	+25 Min.	Typ.	Max.	UNITS
Output Voltage: High-Level, V_{OH} Min.	—	0.5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V_{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I_{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	$\pm 10^{5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25°C$, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ*

CHARACTERISTICS		V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time: Astable, $\overline{Astable}$ to Osc. Out	t_{PHL}, t_{PLH}	5	—	200	400	ns
		10	—	100	200	
		15	—	80	160	
Astable, $\overline{Astable}$ to Q, $\overline{Q}$		5	—	350	700	
		10	—	175	350	
		15	—	125	250	
+ or − Trigger to Q, $\overline{Q}$		5	—	500	1000	
		10	—	225	450	
		15	—	150	300	
Retrigger to Q, $\overline{Q}$		5	—	300	600	
		10	—	150	300	
		15	—	100	200	
External Reset to Q, $\overline{Q}$		5	—	250	500	
		10	—	100	200	
		15	—	70	140	
Transition Time: Osc. Out, Q, $\overline{Q}$	t_{THL}, t_{TLH}	5	—	100	200	
		10	—	50	100	
		15	—	40	80	
Minimum Input Pulse Width: + Trigger, − Trigger	t_W	5	—	200	400	
		10	—	80	160	
		15	—	50	100	
Reset		5	—	100	200	
		10	—	50	100	
		15	—	30	60	
Retrigger		5	—	300	600	
		10	—	115	230	
		15	—	75	150	
Input Rise and Fall Time: All Inputs	t_r, t_f	5, 10, 15	Unlimited			μs
Q or $\overline{Q}$ Deviation from 50% Duty Factor		5	—	±0.5	±1	%
		10	—	±0.5	±1	
		15	—	±0.1	±0.5	
Input Capacitance,	C_{IN}	Any Input	—	5	7.7	pF

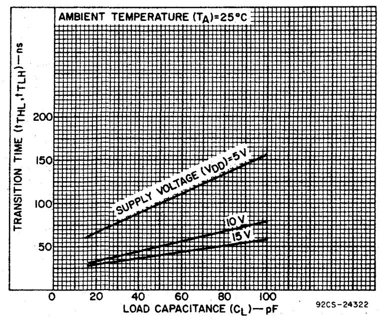


Fig. 10—Typical transition time as a function of load capacitance.

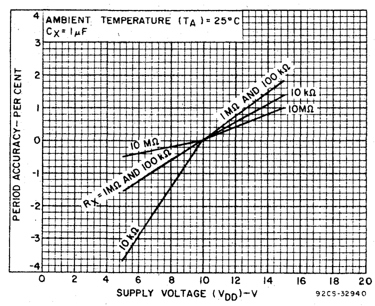


Fig. 11—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. supply voltage.

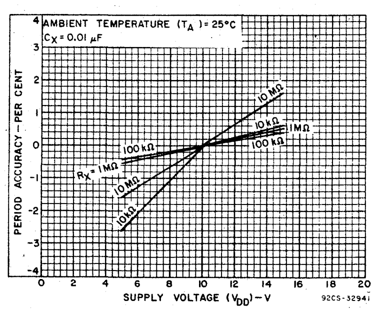


Fig. 12—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. supply voltage.

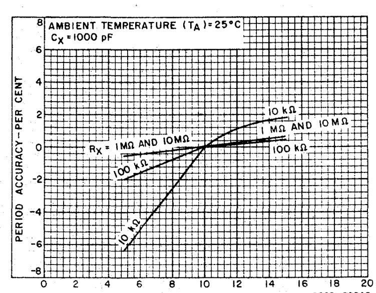


Fig. 13—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. supply voltage.

CD4047B Types

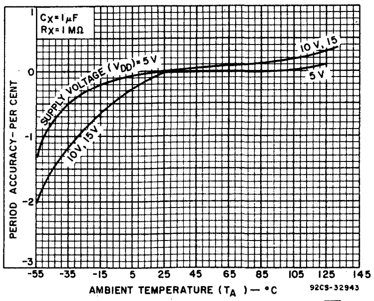


Fig. 14—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature (ultra-low frequency).

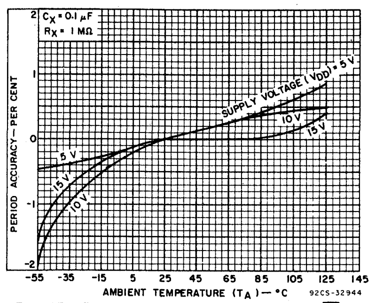


Fig. 15—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature (low frequency).

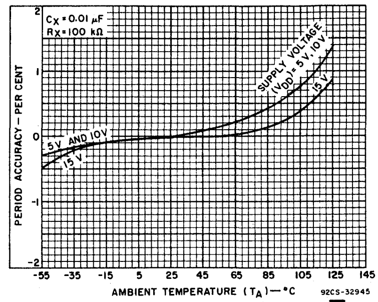


Fig. 16—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature (medium frequency).

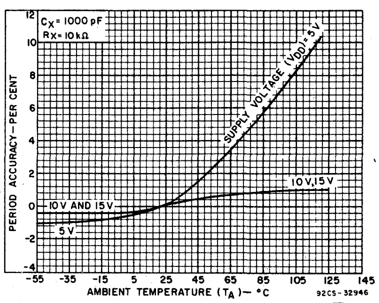


Fig. 17—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature (high-frequency).

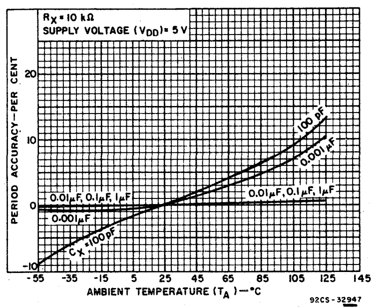


Fig. 18—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature.

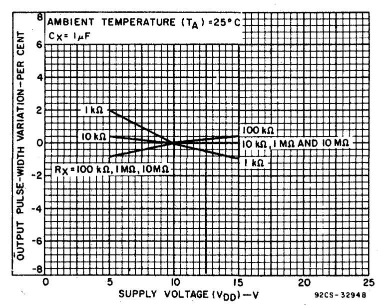


Fig. 19—Typical output pulse-width variations vs. supply voltage.

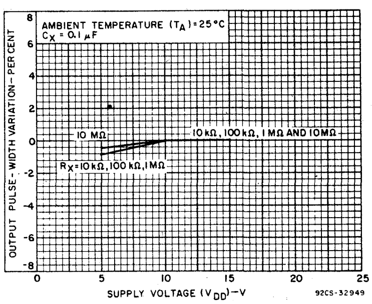


Fig. 20—Typical output pulse-width variations vs. supply voltage.

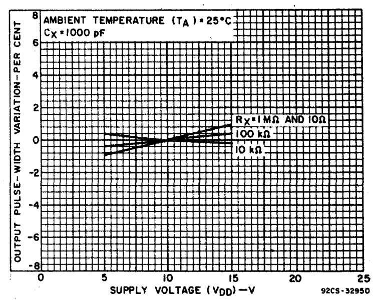


Fig. 21—Typical output pulse-width variations vs. supply voltage.

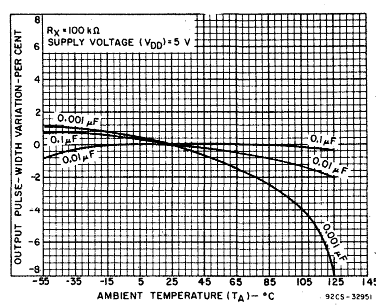


Fig. 22—Typical output pulse-width variations vs. ambient temperature.

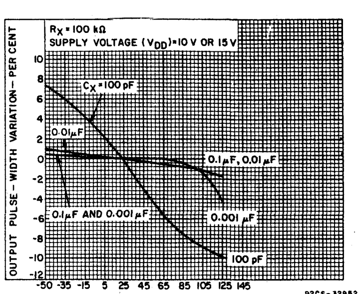


Fig. 23—Typical output pulse-width variations vs. ambient temperature.

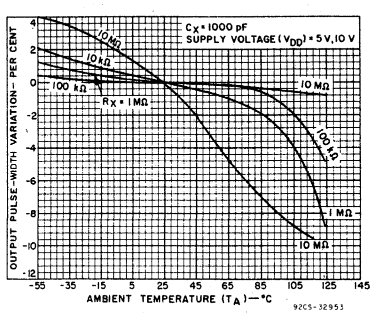


Fig. 24—Typical output-pulse-width variations vs. ambient temperature.

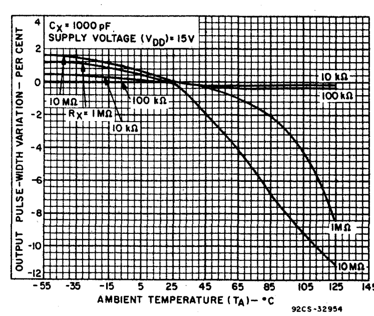


Fig. 25—Typical output pulse-width variations vs. ambient temperature.

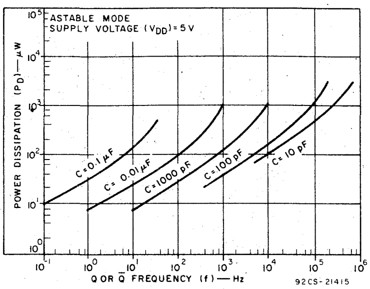


Fig. 26—Typical power dissipation vs. output frequency (V_{DD} = 5 V).

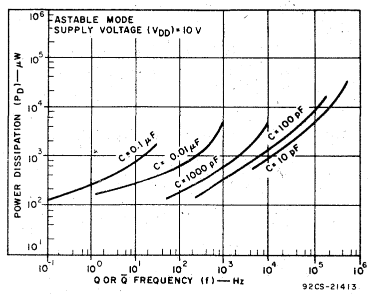


Fig. 27—Typical power dissipation vs. output frequency (V_{DD} = 10 V).

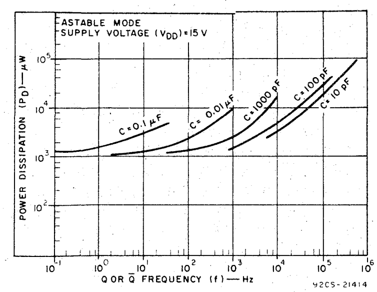


Fig. 28—Typical power dissipation vs. output frequency (V_{DD} = 15 V).

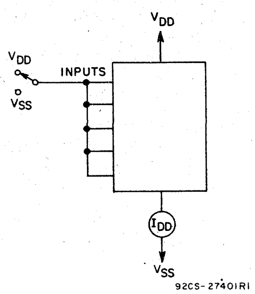


Fig. 29—Quiescent device current test circuit.

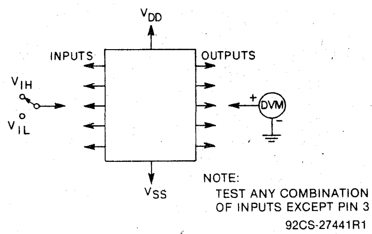


Fig. 30—Input-voltage test circuit.

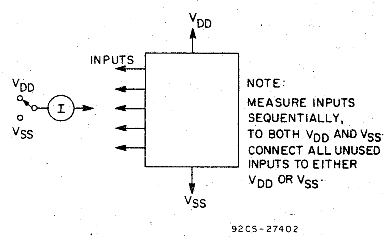


Fig. 31—Input-leakage-current test circuit.

1. Astable Mode Design Information

A. Unit-to-Unit Transfer-Voltage Variations — The following analysis presents variations from unit to unit as a function of transfer-voltage (V_{TR}) shift (33%—67% V_{DD}) for free-running (astable) operation.

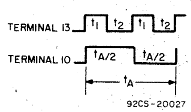


Fig. 32—Astable mode waveforms.

$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}};$$

typically, t_1 = 1.1 RC

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}};$$

typically, t_2 = 1.1 RC

$$t_A = 2(t_1 + t_2)$$

$$= -2\,RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})}$$

Typ: $V_{TR} = 0.5\ V_{DD}$ $t_A = 4.40$ RC
Min: $V_{TR} = 0.33\ V_{DD}$ $t_A = 4.62$ RC
Max: $V_{TR} = 0.67\ V_{DD}$ $t_A = 4.62$ RC

thus if $t_A = 4.40$ RC is used, the variation will be +5%, −0% due to variations in transfer voltage.

B. Variations Due to V_{DD} and Temperature Changes — In addition to variations from unit to unit, the astable period varies with V_{DD} and temperature. Typical variations are presented in graphical form in Figs. 11 to 18 with 10 V as reference for voltage variations curves and 25°C as reference for temperature variations curves.

II. Monostable Mode Design Information

The following analysis presents variations from unit to unit as a function of transfer-voltage (V_{TR}) shift (33% — 67% V_{DD}) for one-shot (monostable) operation.

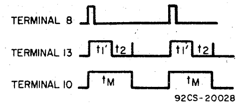


Fig. 33—Monostable waveforms.

$$t_1' = -RC \ln \frac{V_{TR}}{2V_{DD}};$$

typically, t_1' = 1.38 RC

$$t_M = (t_1' + t_2)$$

$$t_M = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})(2V_{DD})}$$

where t_M = Monostable mode pulse width. Values for t_M are as follows:

Typ: $V_{TR} = 0.5\ V_{DD}$ $t_M = 2.48$ RC
Min: $V_{TR} = 0.33\ V_{DD}$ $t_M = 2.71$ RC
Max: $V_{TR} = 0.67\ V_{DD}$ $t_M = 2.48$ RC

thus is $t_M = 2.48$ RC is used, the variation will be +9.3%, −0% due to variations in transfer voltage.

Note:

In the astable mode, the first positive half cycle has a duration of t_M; succeeding durations are $t_A/2$.

In addition to variations from unit to unit, the monostable pulse width varies with V_{DD} and temperature. These variations are presented in graphical form in Fig. 19 to 26 with 10 V as reference for voltage-variation curves and 25°C as reference for temperature-variation curves.

III. Retrigger Mode Operation

The CD4047B can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminal 12, and the output is taken from terminal 10 or 11. As shown in Fig. 34 normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied.

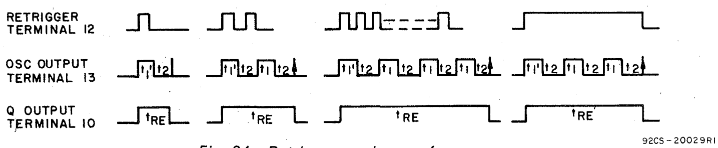


Fig. 34—Retrigger-mode waveforms.

For two input pulses, $t_{RE} = t_1' + t_1 + 2t_2$. For more than two pulses, the output pulse width is an integral number of time periods, with the first time period being $t_1' + t_2$, typically, 2.48RC, and all subsequent time periods being $t_1 + t_2$, typically, 2.2RC.

IV. External Counter Option

Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Fig. 35. The pulse duration at the output is

$$t_{ext} = (N - 1)(t_A) + (t_M + t_A/2)$$

where t_{ext} = pulse duration of the circuitry, and N is the number of counts used.

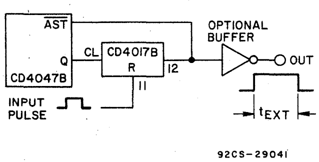


Fig. 35—Implementation of external counter option.

V. Timing-Component Limitations

The capacitor used in the circuit should be non-polarized and have low leakage (i.e. the parallel resistance of the capacitor should be at least an order of magnitude greater than the external resistor used). There is no upper or lower limit for either R or C value to maintain oscillation.

However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the COS/MOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted.

The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be:

C ⩾ 100 pF, up to any practical value, for astable modes;

C ⩾ 1000 pF, up to any practical value for monostable modes.

10 kΩ ⩽ R ⩽ 1 MΩ

VI. Power Consumption

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formulae:

Astable Mode:

$P = 2CV^2f$. (Output at terminal No. 13)

$P = 4CV^2f$. (Output at terminal Nos. 10 and 11)

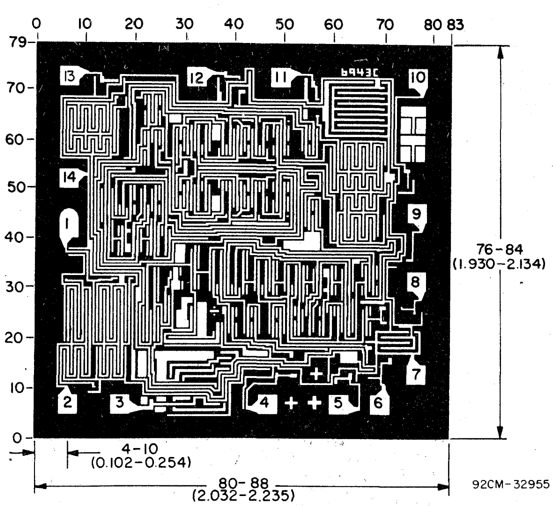
Monostable Mode:

$$P = \frac{(2.9CV^2)\,(\text{Duty Cycle})}{T}$$

(Output at terminal Nos. 10 and 11)

The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.

Because the power dissipation does not depend on R, a design for minimum power dissipation would be a small value of C. The value of R would depend on the desired period (within the limitations discussed above). See Figs. 27, 28, and 29 for typical power consumption in astable mode.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for CD4047B.

COS/MOS Multifunction Expandable 8-Input Gate

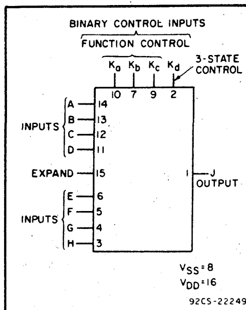
High-Voltage Types (20-Volt Rating)

The RCA-CD4048B is an 8-input gate having four control inputs. Three binary control inputs — Ka, Kb, and Kc — provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR and AND/NOR.

A fourth control input, Kd, provides the user with a 3-state output. When control input Kd is high, the output is either a logic 1 or a logic 0 depending on the inner states. When control input Kd is low, the output is an open circuit. This feature enables the user to connect this device to a common bus line.

In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs into a CD4048B (see Fig. 2). For example, two CD4048B's can be cascaded to provide a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to V_{SS}.

The CD4048B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



Functional Diagram

Features:
- Three-state output
- Many logic functions available in one package
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V (full package-temperature range), 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at V_{DD}=5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD}=15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

Applications:
- Selection of up to 8 logic functions
- Digital control of logic
- General-purpose gating logic
  - Decoding
  - Encoding

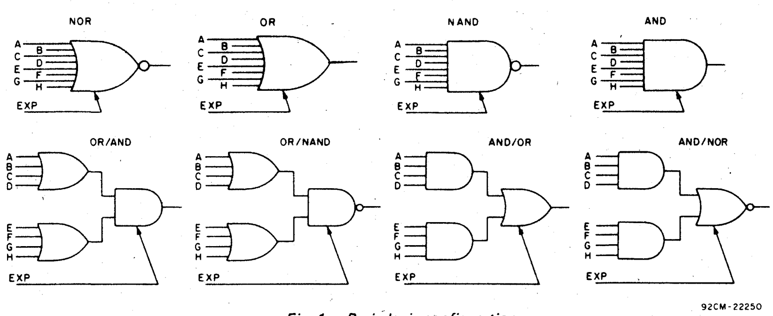
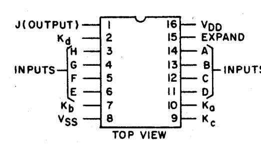


Fig. 1 — Basic logic configurations.



TERMINAL ASSIGNMENT

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

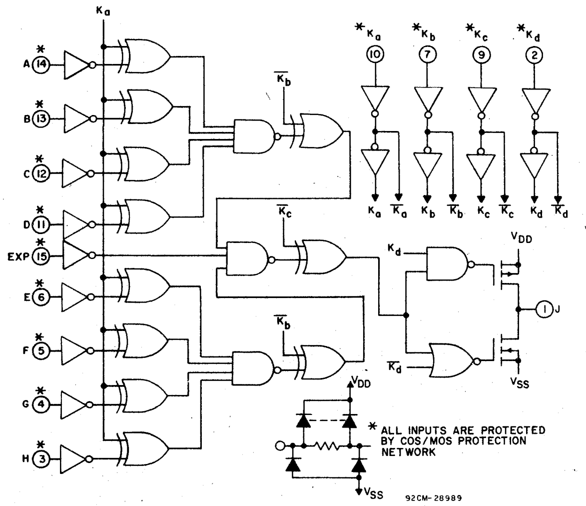


Fig. 2 – Logic diagram.

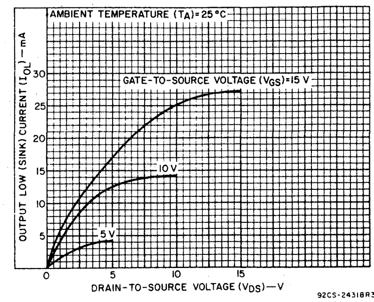


Fig. 6 – Typical output low (sink) current characteristics.

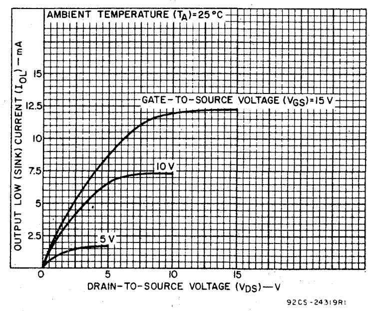


Fig. 7 – Minimum output low (sink) current characteristics.

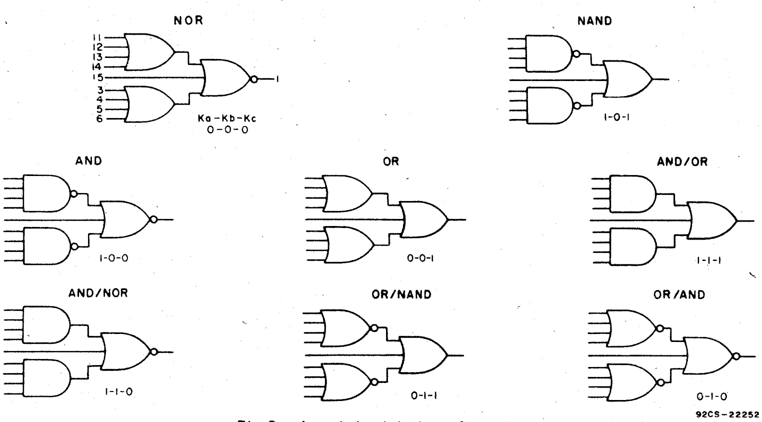


Fig. 3 – Actual-circuit logic configurations.

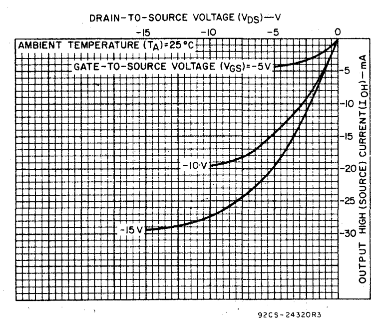


Fig. 8 – Typical output high (source) current characteristics.

APPLICATIONS OF EXPAND INPUT

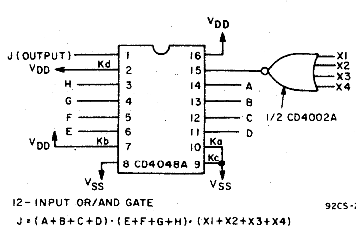


Fig. 4 – 12-input OR/AND gate.

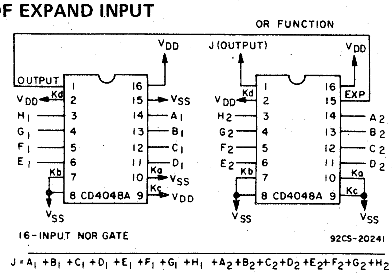


Fig. 5 – 16-input NOR gate.

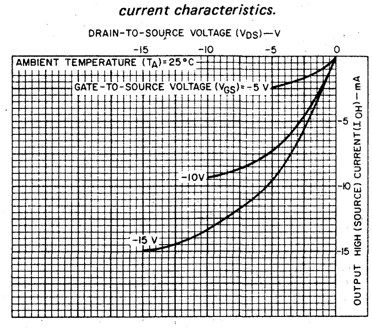


Fig. 9 – Minimum output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages Values at −40, +25, +85 Apply to E Package −55	−40	+85	+125	+25 Min.	Typ.	Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA
3-State Output Current, I_{OUT}	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm10^{-4}$	±0.4	μA

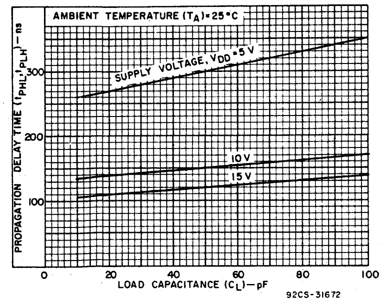


Fig. 10 – Typical propagation delay time (logic inputs to output) as a function of load capacitance.

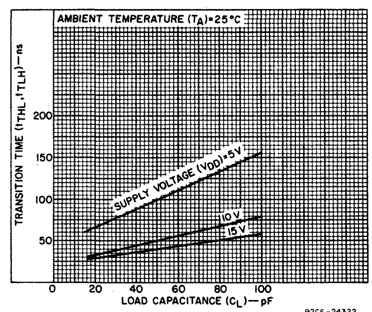


Fig. 11 – Typical transition time vs. load capacitance.

IMPLEMENTATION OF EXPAND INPUT FOR 9 OR MORE INPUTS

OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	$J=\overline{(A+B+C+D+E+F+G+H)+(EXP)}$
OR	OR	$J=(A+B+C+D+E+F+G+H)+(EXP)$
AND	NAND	$J=(ABCDEFGH)\cdot\overline{(EXP)}$
NAND	NAND	$J=\overline{(ABCDEFGH)\cdot\overline{(EXP)}}$
OR/AND	NOR	$J=(A+B+C+D)\cdot(E+F+G+H)\cdot\overline{(EXP)}$
OR/NAND	NOR	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)\cdot\overline{(EXP)}}$
AND/NOR	AND	$J=\overline{(ABCD)+(EFGH)+(EXP)}$
AND/OR	AND	$J=(ABCD)+(EFGH)+(EXP)$

Note: (EXP) designates the EXPAND function (i.e., $X_1+X_2+\ldots X_N$).

NOTE:
Refer to FUNCTION TRUTH TABLE for connection of unused inputs.

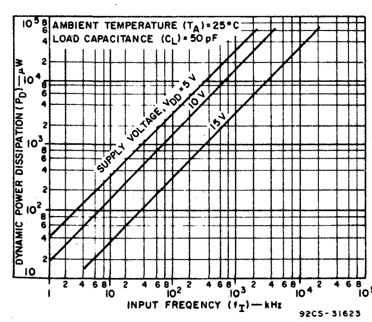


Fig. 12 – Typical power dissipation as a function of input frequency.

CD4048B Types

DYNAMIC CHARACTERISTICS at T_A=25°C, C_L=50 pF, Input t_r,t_f=20 ns, R_L=200 kΩ unless otherwise specified

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
		V_{DD} V	All Package Types Typ.	All Package Types Max.	
Propagation Delay: t_{PHL},t_{PLH} Inputs to Output and Ka to Output		5	300	600	ns
		10	150	300	
		15	120	240	
Kb to Output		5	225	450	
		10	85	170	
		15	55	110	
Kc to Output		5	140	280	
		10	50	100	
		15	40	80	
Expand Input to Output		5	190	380	
		10	90	180	
		15	65	130	
3-State Propagation Delay: Kd to Output t_{PHZ},t_{PLZ} t_{PZH},t_{PZL}	R_L=1 kΩ See Fig.21	5	80	160	
		10	35	70	
		15	25	50	
Transition Time: t_{THL},t_{TLH}		5	100	200	
		10	50	100	
		15	40	80	
Input Capacitance: C_I	Any Input		5	7	pF
3-State Output Capacitance			5	10	

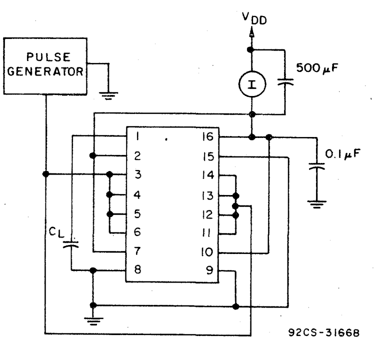


Fig. 13 – Dynamic power dissipation test circuit.

FUNCTION TRUTH TABLE

OUTPUT FUNCTION	BOOLEAN EXPRESSION	K_a	K_b	K_c	UNUSED INPUT*
NOR	$J=\overline{A+B+C+D+E+F+G+H}$	0	0	0	V_{SS}
OR	$J=A+B+C+D+E+F+G+H$	0	0	1	V_{SS}
OR/AND	$J=(A+B+C+D)\cdot(E+F+G+H)$	0	1	0	V_{SS}
OR/NAND	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)}$	0	1	1	V_{SS}
AND	$J=ABCDEFGH$	1	0	0	V_{DD}
NAND	$J=\overline{ABCDEFGH}$	1	0	1	V_{DD}
AND/NOR	$J=\overline{ABCD+EFGH}$	1	1	0	V_{DD}
AND/OR	$J=ABCD+EFGH$	1	1	1	V_{DD}
K_d=1 Normal Inverter Action					
K_d=0 High Impedance Output					

EXPAND Input=0

* See Figs. 1,2,3,4, and 5.

TEST CIRCUITS - STATIC MEASUREMENTS

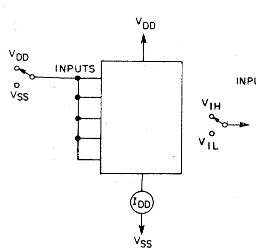


Fig. 14 – Quiescent device current test circuit.

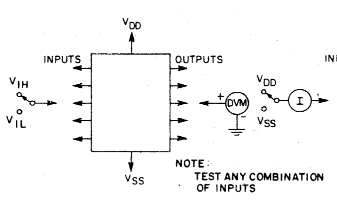


Fig. 15 – Input voltage test circuit.

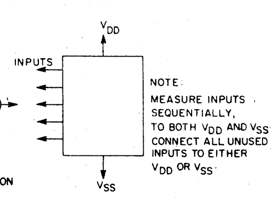


Fig. 16 – Input current test circuit.

TEST CIRCUITS - DYNAMIC MEASUREMENTS

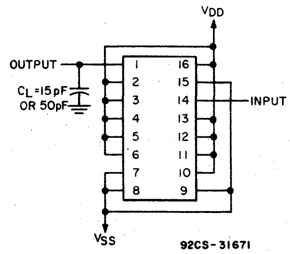


Fig. 17 – Test circuit for t_{PHL}, t_{THL}, and t_{TLH} (AND) measurements.

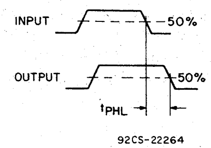


Fig. 18 – Waveforms for t_{PHL} and t_{PHL} (AND).

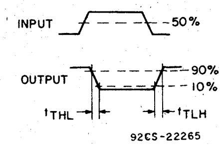


Fig. 19 – Waveforms for t_{THL} and t_{TLH} (AND).

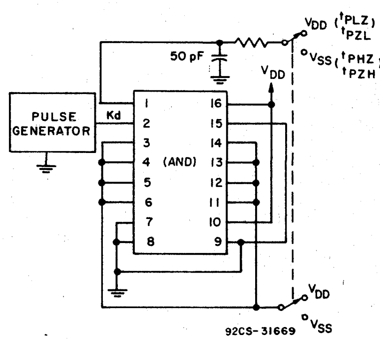


Fig. 20 – Test circuit for t_{PZL}, t_{PZH}, t_{PLZ}, and t_{PHZ} (AND).

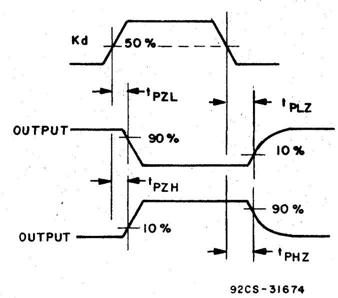
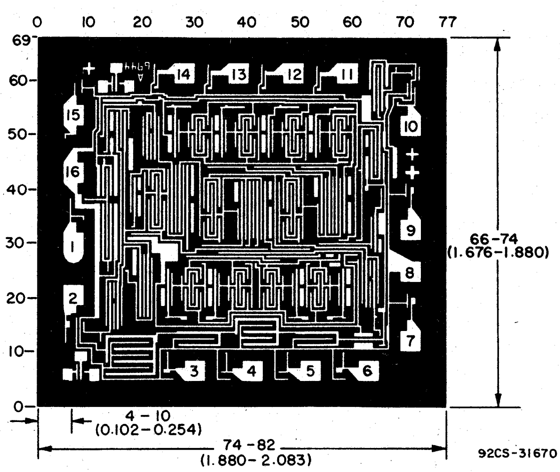


Fig. 21 – Waveforms for t_{PZL}, t_{PZH}, t_{PLZ}, and t_{PHZ} (AND).



Dimensions and pad layout for CD4048BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4049UB, CD4050B Types

COS/MOS Hex Buffer/Converters

High-Voltage Types (20-Volt Rating)

CD4049UB—Inverting Type

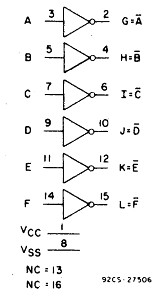
CD4050B—Non-Inverting Type

Features:

- **High sink current for driving 2 TTL loads**
- **High-to-low level logic conversion**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **5-, 10-, and 15-volt parametric ratings**

Applications:

- **COS/MOS to DTL/TTL hex converter**
- **COS/MOS current "sink" or "source" driver**
- **COS/MOS high-to-low logic-level converter**



CD4049UB FUNCTIONAL DIAGRAM

The RCA-CD4049UB and CD4050B are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC}=5 V, $V_{OL} \leq$ 0.4 V, and $I_{OL} \geq$ 3.2 mA.)

The CD4049UB and CD4050B are designated as replacements for CD4009UB and CD4010B, respectively. Because the CD4049UB and CD4050B require only one power supply, they are preferred over the CD4009UB and CD4010B and should be used in place of the CD4009UB and CD4010B in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049UB and CD4050B are pin compatible with the CD4009UB and CD4010B respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049UB or CD4050B, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069UB Hex Inverter is recommended.

The CD4049UB and CD4050B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

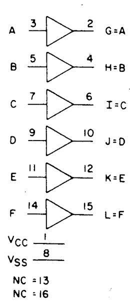
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to +20.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (V_{CC}) (For T_A=Full Package-Temperature Range)	3	18	V
Input Voltage Range (V_{IN})	V_{CC}*	18	V

*The CD4049 and CD4050 have high-to-low-level voltage conversion capability but not low-to-high-level; therefore it is recommended that $V_{IN} \geq V_{CC}$.



CD4050B FUNCTIONAL DIAGRAM

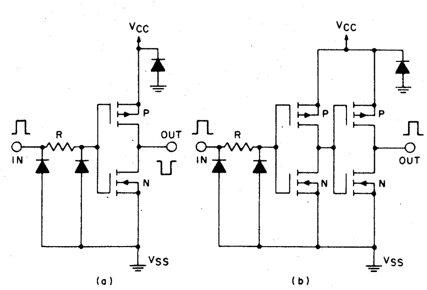


Fig. 1—a) Schematic diagram of CD4049UB, 1 of 6 identical units; b) Schematic diagram of CD4050B, 1 of 6 identical units.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{CC} (V)	Limits At Indicated Temperatures (°C) Values at −55,+25,+125 Apply to D,F,H Pkgs. Values at −40,+25,+85 Apply to E Package −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	4.5	3.3	3.1	2.1	1.8	2.6	5.2	–	mA
	0.4	0,5	5	4	3.8	2.9	2.4	3.2	6.4	–	
	0.5	0,10	10	10	9.6	6.6	5.6	8	16	–	
	1.5	0,15	15	26	25	20	18	24	48	–	
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	−0.81	−0.73	−0.58	−0.48	−0.65	−1.2	–	
	2.5	0,5	5	−2.6	−2.4	−1.9	−1.55	−2.1	−3.9	–	
	9.5	0,10	10	−2.0	−1.8	−1.35	−1.18	−1.65	−3.0	–	
	13.5	0,15	15	−5.2	−4.8	−3.5	−3.1	−4.3	−8.0	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05					0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage: V_{IL} Max. CD4049UB	4.5	–	5	1				–	–	1	V
	9	–	10	2				–	–	2	
	13.5	–	15	2.5				–	–	2.5	
Input Low Voltage: V_{IL} Max. CD4050B	0.5	–	5	1.5				–	–	1.5	
	1	–	10	3				–	–	3	
	1.5	–	15	4				–	–	4	
Input High Voltage: V_{IH} Min. CD4049UB	0.5	–	5	4				4	–	–	
	1	–	10	8				8	–	–	
	1.5	–	15	12.5				12.5	–	–	
Input High Voltage: V_{IH} Min. CD4050B	4.5	–	5	3.5				3.5	–	–	
	9	–	10	7				7	–	–	
	13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

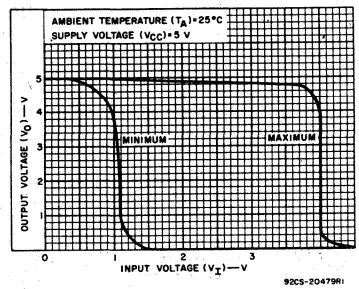


Fig. 2—Minimum and maximum voltage transfer characteristics for CD4049UB.

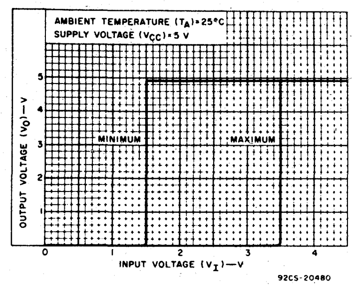


Fig. 3—Minimum and maximum voltage transfer characteristics for CD4050B.

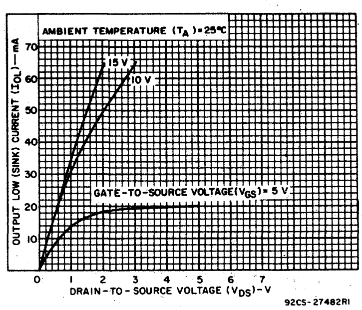


Fig. 4 – Typical output low (sink) current characteristics.

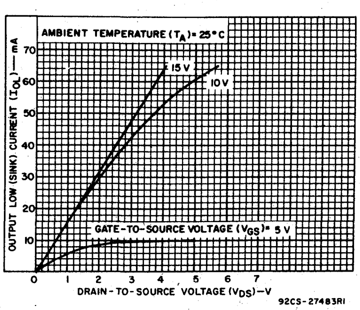


Fig. 5 – Minimum output low (sink) current drain characteristics.

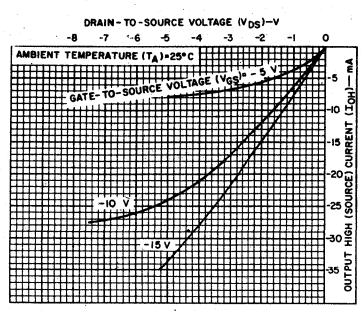


Fig. 6 – Typical output high (source) current characteristics.

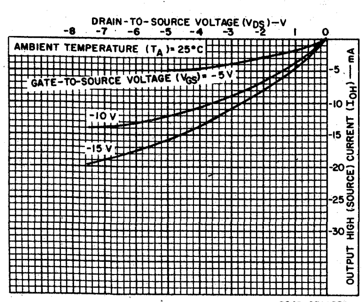


Fig. 7 – Minimum output high (source) current characteristics.

CD4049UB, CD4050B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; Input t_r,t_f=20 ns, C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC	CONDITIONS V_{IN}	CONDITIONS V_{CC}	LIMITS ALL PKGS. Typ.	LIMITS ALL PKGS. Max.	UNITS
Propagation Delay Time: Low-to-High, t_{PLH} CD4049UB	5	5	60	120	ns
	10	10	32	65	
	10	5	45	90	
	15	15	25	50	
	15	5	45	90	
CD4050B	5	5	70	140	
	10	10	40	80	
	10	5	45	90	
	15	15	30	60	
	15	5	40	80	
High-to-Low, t_{PHL} CD4049UB	5	5	32	65	ns
	10	10	20	40	
	10	5	15	30	
	15	15	15	30	
	15	5	10	20	
CD4050B	5	5	55	110	
	10	10	22	55	
	10	5	50	100	
	15	15	15	30	
	15	5	50	100	
Transition Time: Low-to-High, t_{TLH}	5	5	80	160	ns
	10	10	40	80	
	15	15	30	60	
High-to-Low, t_{THL}	5	5	30	60	
	10	10	20	40	
	15	15	15	30	
Input Capacitance, C_{IN} CD4049UB	–	–	15	22.5	pF
CD4050B	–	–	5	7.5	

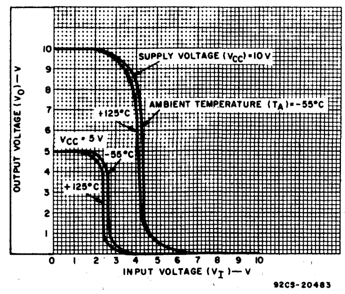


Fig. 8 – Typical voltage transfer characteristics as a function of temperature for CD4049UB.

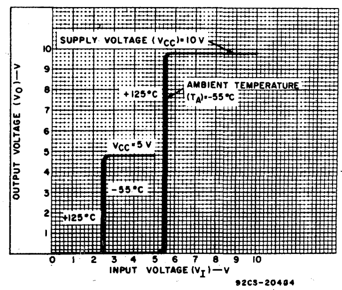


Fig. 9 – Typical voltage transfer characteristics as a function of temperature for CD4050B.

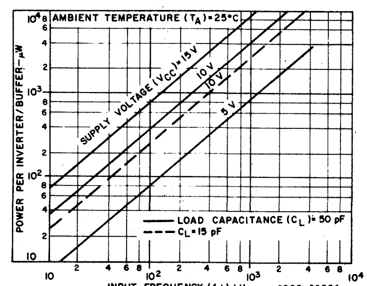


Fig. 10 – Typical power dissipation vs. frequency characteristics.

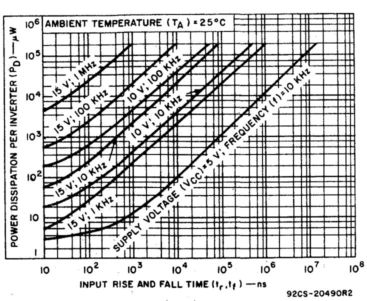


Fig. 11 – Typical power dissipation vs. input rise and fall times per inverter for CD4049UB.

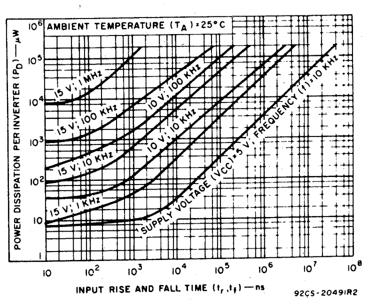


Fig. 12 – Typical power dissipation vs. input rise and fall times per inverter for CD4050B.

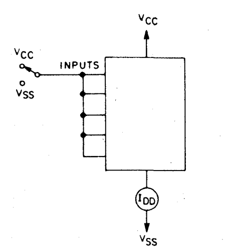


Fig. 13 – Quiescent device current test circuit.

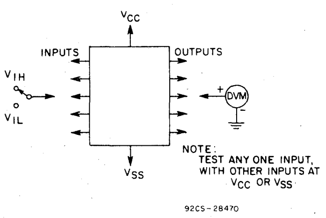


Fig. 14 – Input voltage test circuit.

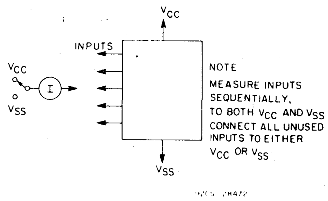


Fig. 15 – Input current test circuit.

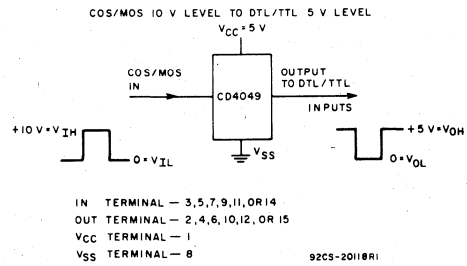
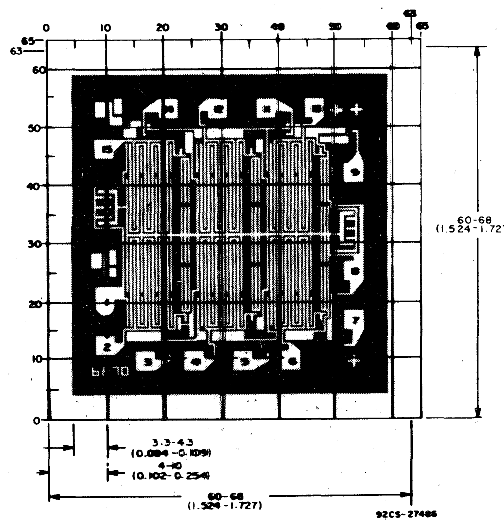


Fig. 16 – Logic-level conversion application.

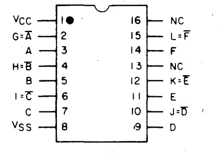


Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

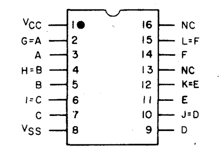
Photograph of chip for CD4049UB. Dimensions and pad layout for CD4050B are identical.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

TERMINAL ASSIGNMENTS



CD4049UB



CD4050B

CD4051B, CD4052B, CD4053B Types

COS/MOS Analog Multiplexers/Demultiplexers*

With Logic-Level Conversion

High-Voltages Types (20-Volt Rating)

CD4051B – Single 8-Channel
CD4052B – Differential 4-Channel
CD4053B – Triple 2-Channel

RCA-CD4051B, CD4052B, and CD4053B analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20 V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20 V (if V_{DD}-V_{SS} = 3 V, a V_{DD}-V_{EE} of up to 13 V can be controlled; for V_{DD}-V_{EE} level differences above 13 V, a V_{DD}-V_{SS} of at least 4.5 V is required). For example, if V_{DD} = +4.5V, V_{SS} = 0, and V_{EE} = –13.5 V, analog signals from –13.5 V to +4.5 V can be controlled by digital inputs of 0 to 5 V. These multiplexer circuits dissipate extremely low quiescent power over the full V_{DD}-V_{SS} and V_{DD}-V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal all channels are off.

The CD4051B is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

The CD4051B, CD4052B, and CD4053B are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead plastic dual-in-line packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

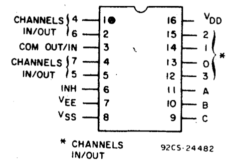
* When these devices are used as demultiplexers, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminals are the inputs.

Applications:

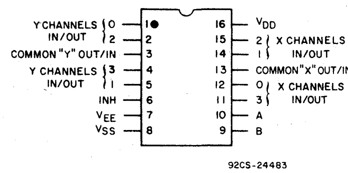
- **Analog and digital multiplexing and demultiplexing**
- **A/D and D/A conversion**
- **Signal gating**

Features:

- **Wide range of digital and analog signal levels: digital 3 to 20 V, analog to 20 V_{p-p}**
- **Low ON resistance: 125 Ω (typ.) over 15 V_{p-p} signal-input range for V_{DD}-V_{EE} = 15 V**
- **High OFF resistance: channel leakage of ±100 pA (typ.) @ V_{DD}-V_{EE} = 18 V**
- **Logic-level conversion for digital addressing signals of 3 to 20 V (V_{DD}-V_{SS} = 3 to 20 V) to switch analog signals to 20 V p-p (V_{DD}-V_{EE} = 20 V); see introductory text**
- **Matched switch characteristics: R_{ON} = 5 Ω (typ.) for V_{DD}-V_{EE} = 15 V**
- **Very low quiescent power dissipation under under all digital-control input and supply conditions: 0.2 μW (typ.) @ V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10 V**
- **Binary address decoding on chip**
- **5-, 10-, and 15-V parametric ratings**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**



CD4051B
Terminal Assignment



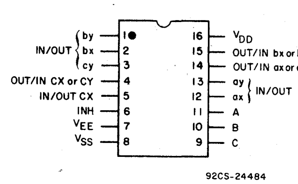
CD4052B
Terminal Assignment

RECOMMENDED OPERATING CONDITIONS AT T_A =25°C (Unless Otherwise Specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted.

CHARACTERISTIC	V_{DD}	Min.	Max.	Units
Supply-Voltage Range (T_A = Full Package-Temp. Range)	–	3	18	V
Multiplexer Switch Input Current Capability*	–	–	25	mA
Output Load Resistance	–	100	–	Ω

* In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 3 on the CD4051; terminals 3 and 13 on the CD4052; terminals 4,14, and 15 on the CD4053.



CD4053B
Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltages referenced to V_{SS} or V_{EE}, whichever is more negative)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

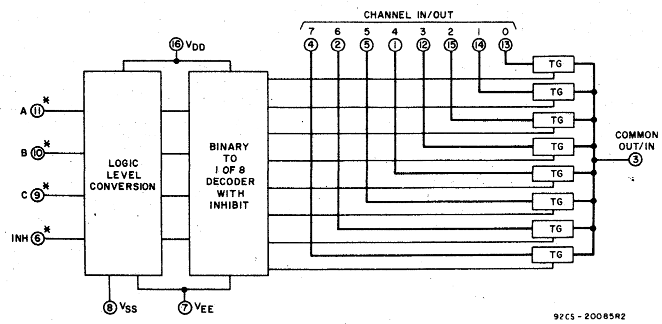


Fig. 1 – Functional diagram of CD4051B.

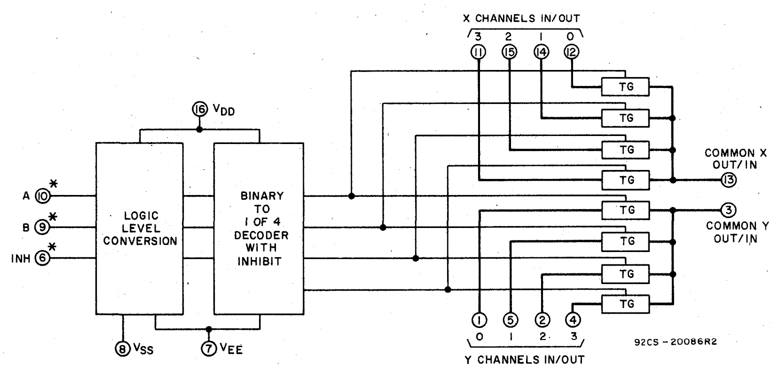


Fig. 2 – Functional diagram of CD4052B.

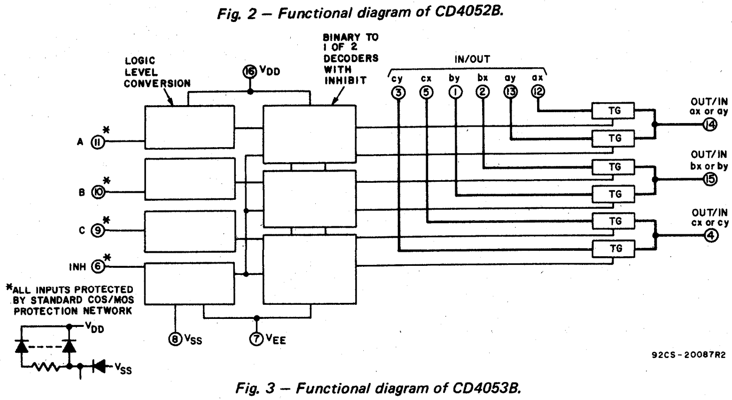


Fig. 3 – Functional diagram of CD4053B.

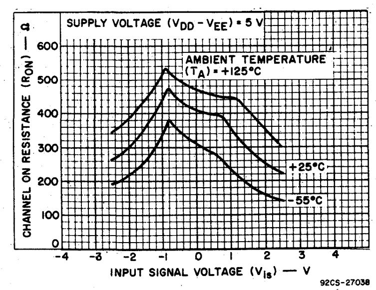


Fig.4 – Typical channel ON resistance vs input signal voltage (all types).

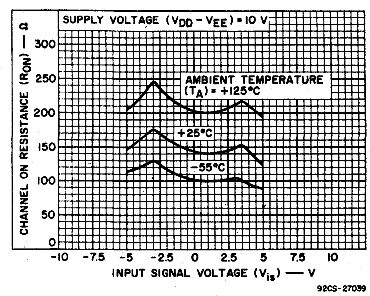


Fig.5 – Typical channel ON resistance vs. input signal voltage (all types).

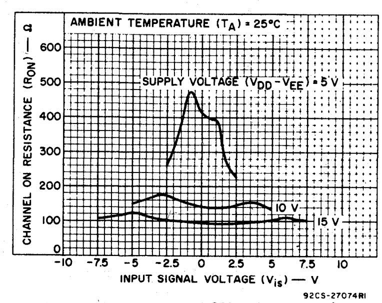


Fig.6 – Typical channel ON resistance vs. input signal voltage (all types).

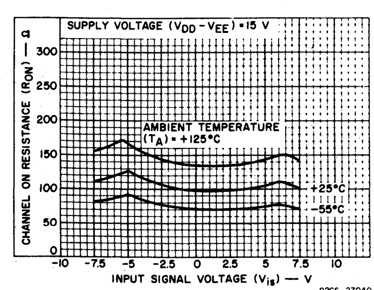


Fig.7 – Typical channel ON resistance vs. input signal voltage (all types).

CD4051B, CD4052B, CD4053B Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_{is} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS at Indicated Temperature (°C) Values at −55,+25,+125, apply to D,F,H pkg Values at −40,+25,+85, apply to E pkgs −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	Units
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{OS})												
Quiescent Device Current, I_{DD} Max.				5	5	5	150	150	–	0.04	5	μA
				10	10	10	300	300	–	0.04	10	
				15	20	20	600	600	–	0.04	20	
				20	100	100	3000	3000	–	0.08	100	
On-State Resistance $0 \leqslant V_{is} \leqslant V_{DD}$ r_{on} Max.		0	0	5	800	850	1200	1300	–	470	1050	Ω
		0	0	10	310	330	520	550	–	180	400	
		0	0	15	200	210	300	320	–	125	240	
Change in On-State Resistance (Between Any Two Channels) Δr_{on}		0	0	5	–	–	–	–	–	15	–	Ω
		0	0	10	–	–	–	–	–	10	–	
		0	0	15	–	–	–	–	–	5	–	
OFF Channel Leakage Current: Any Channel OFF Max. or All Channels OFF (Common OUT/IN) Max.		0	0	18	±100*		±1000*		–	±0.01	±100*	nA
Capacitance: Input, C_{is}					–	–	–	–	–	5	–	pF
Output, C_{os} CD4051		−5	−5	5	–	–	–	–	–	30	–	
CD4052					–	–	–	–	–	18	–	
CD4053					–	–	–	–	–	9	–	
Feedthrough, C_{ios}					–	–	–	–	–	0.2	–	
Propagation Delay Time (Signal Input to Output)	V_{DD} (pulse)	$R_L = 200\,k\Omega$, $C_L = 50$ pF, $t_r, t_f = 20$ ns		5	–	–	–	–	–	30	60	ns
				10	–	–	–	–	–	15	30	
				15	–	–	–	–	–	10	20	

* Determined by minimum feasible leakage measurement for automatic testing.

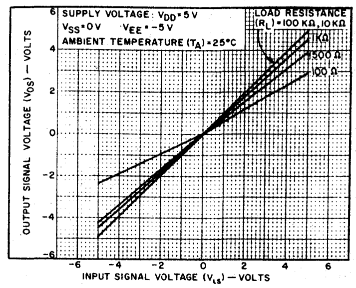


Fig.8 — Typical ON characteristics for 1 of 8 channels (CD4051B).

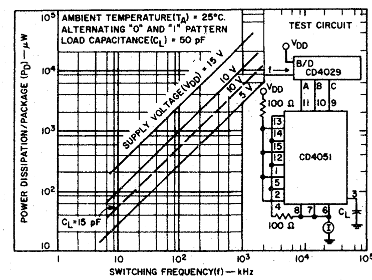


Fig.9 — Typical dynamic power dissipation vs. switching frequency (CD4051B).

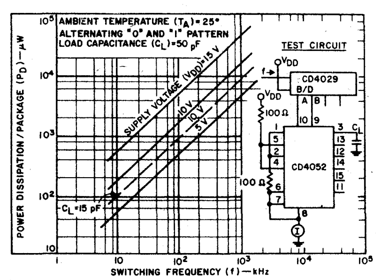


Fig.10 — Typical dynamic power dissipation vs. switching frequency (CD4052B).

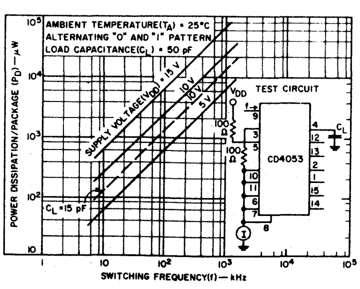
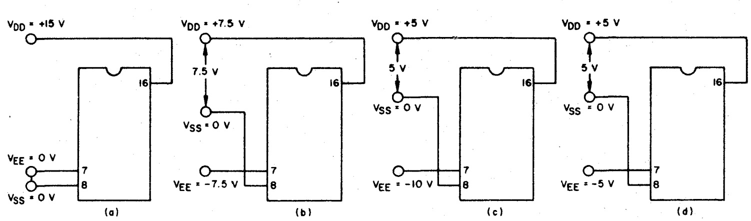


Fig.11 — Typical dynamic power dissipation vs. switching frequency (CD4053B).



The ADDRESS (digital-control inputs) and INHIBIT logic levels are: "0" = V_{SS} and "1" = V_{DD}. The analog signal (through the TG) may swing from V_{EE} to V_{DD}.

Fig.12 — Typical bias voltages.

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	CONDITIONS V_{is} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS at Indicated Temperature (°C) Values at –55,+25,+125, apply to D,F,H pkg Values at –40,+25,+85, apply to E pkgs –55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	Units
CONTROL (ADDRESS or INHIBIT) V_C												
Input Low Voltage, V_{IL} Max.	$=V_{DD}$ thru 1 kΩ	$V_{EE}=V_{SS}$ R_L=1 kΩ to V_{SS} $I_{IS}<2\ \mu A$ on all OFF Channels		5	1.5				–	–	1.5	V
				10	3				–	–	3	V
				15	4				–	–	4	V
Input High Voltage, V_{IH} Min.				5	3.5				3.5	–	–	V
				10	7				7	–	–	V
				15	11				11	–	–	V
Input Current, I_{IN} Max.	V_{IN} = 0,18			18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	µA
Propagation Delay Time:	t_r,t_f = 20 ns, C_L = 50 pF											
Address-to-Signal OUT (Channels ON or OFF) See Figs.14,15,18		0	0	5	–	–	–	–	–	360	720	ns
		0	0	10	–	–	–	–	–	160	320	ns
		0	0	15	–	–	–	–	–	120	240	ns
		–5	0	5	–	–	–	–	–	225	450	ns
Inhibit-to-Signal OUT (Channel turning ON)	R_L=10 kΩ, C_L=50 pF t_r,t_f = 20 ns	0	0	5	–	–	–	–	–	360	720	ns
		0	0	10	–	–	–	–	–	160	320	ns
		0	0	15	–	–	–	–	–	120	240	ns
		–10	0	5	–	–	–	–	–	200	400	ns
Inhibit-to-Signal OUT (Channel turning OFF)	R_L=300Ω, C_L=50 pF t_r,t_f = 20 ns	0	0	5	–	–	–	–	–	200	450	ns
		0	0	10	–	–	–	–	–	90	210	ns
		0	0	15	–	–	–	–	–	70	160	ns
		–10	0	5	–	–	–	–	–	130	300	ns
Input Capacitance, C_{IN} (Any Address or Inhibit Input)					–	–	–	–	–	5	7.5	pF

INPUT STATES INHIBIT	C	B	A	"ON" CHANNEL(S)
CD4051B				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	NONE
CD4052B				
INHIBIT		B	A	
0		0	0	0x, 0y
0		0	1	1x, 1y
0		1	0	2x, 2y
0		1	1	3x, 3y
1		X	X	NONE
CD4053B				
INHIBIT	A or B or C			
0	0			ax or bx or cx
0	1			ay or by or cy
1	X			NONE

X = Don't care

Fig. 13 – Truth tables.

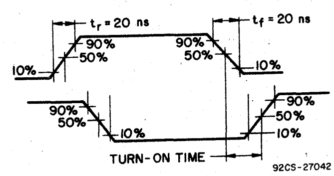


Fig. 14 – Waveforms, channel being turned ON (R_L = 10 kΩ).

TEST CIRCUITS

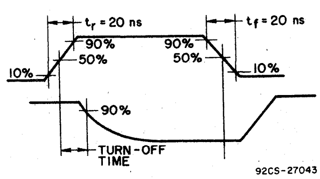


Fig. 15 – Waveforms, channel being turned OFF (R_L = 300 Ω).

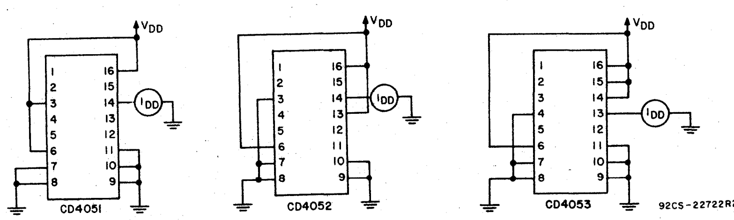


Fig. 16 – OFF channel leakage current – any channel OFF.

CD4051B, CD4052B, CD4053B Types

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS: V_{is} (V)	V_{DD} (V)	R_L (kΩ)			LIMITS: TYPICAL VALUE	UNITS
Cutoff (−3-dB) Frequency Channel ON (Sine Wave Input)	5•	10	1	V_{OS} at Common OUT/IN	CD4053	30	MHz
	$V_{EE} = V_{SS}$, $20 \log \frac{V_{OS}}{V_{is}} = -3$ dB				CD4052	25	
					CD4051	20	
				V_{OS} at Any Channel		60	
Total Harmonic Distortion, THD	2•	5	10			0.3	%
	3•	10				0.2	
	5•	15				0.12	
	$V_{EE} = V_{SS}$, f_{is} = 1 kHz sine wave						
−40-dB Feedthrough Frequency (All Channels OFF)	5•	10	1	V_{OS} at Common OUT/IN	CD4053	8	MHz
	$V_{EE} = V_{SS}$, $20 \log \frac{V_{OS}}{V_{is}} = -40$dB				CD4052	10	
					CD4051	12	
				V_{OS} at Any Channel		8	
−40-dB Signal Crosstalk Frequency	5•	10	1	Between Any 2 Channels		3	MHz
	$V_{EE} = V_{SS}$, $20 \log \frac{V_{OS}}{V_{is}} = -40$dB			Between Sections CD4052 Only	Measured on Common	6	
					Measured on Any Channel	10	
				Between Any 2 Sections CD4053 Only	In Pin 2, Out Pin 14	2.5	
					In Pin 15, Out Pin 14	6	
Address-or-Inhibit-to Signal Crosstalk	–	10	10#			65	mV (Peak)
	V_{EE}=0, V_{SS}=0, t_r,t_f =20 ns, $V_C = V_{DD} - V_{SS}$ (Square Wave)						

• Peak-to-peak voltage symmetrical about $\frac{V_{DD} - V_{EE}}{2}$

Both ends of channel

TEST CIRCUITS (Cont'd)

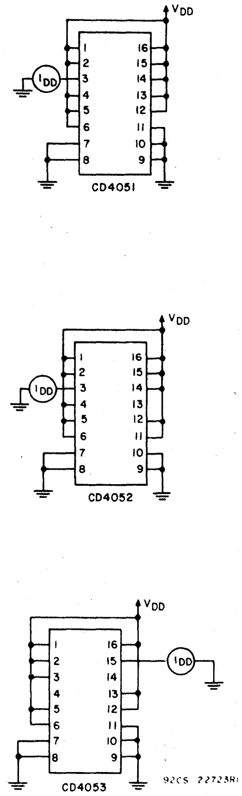


Fig.17 – OFF channel leakage current – all channels OFF.

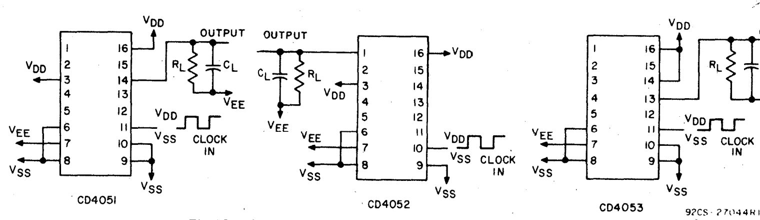


Fig.18 – Propagation delay – address input to signal output.

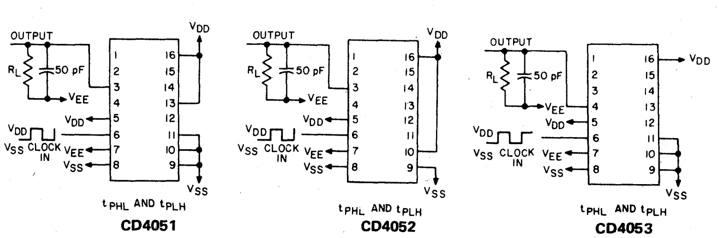
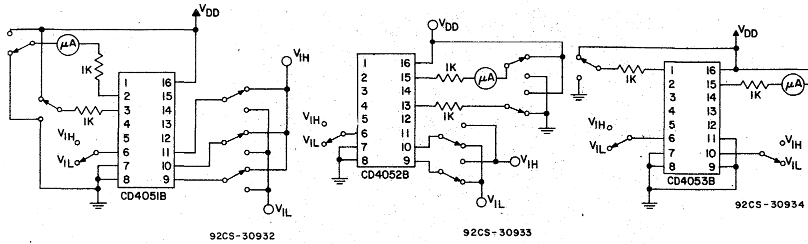


Fig.19 – Propagation delay – inhibit input to signal output.

TEST CIRCUITS (Cont'd)



MEASURE < 2 μA ON ALL "OFF" CHANNELS (e.g. CHANNEL 6)

MEASURE < 2 μA ON ALL "OFF" CHANNELS (e.g. CHANNEL 2x)

MEASURE < 2 μA ON ALL "OFF" CHANNELS (e.g. CHANNEL by)

Fig. 20 – Input voltage test circuits (noise immunity).

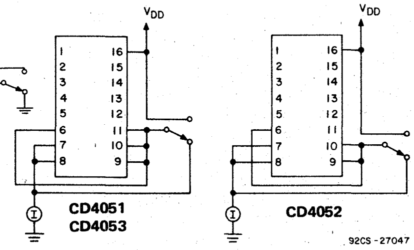


Fig.21 – Quiescent device current.

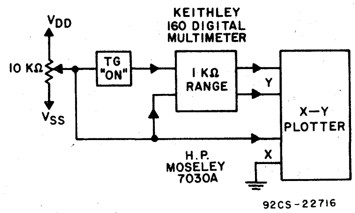


Fig.22 – Channel ON resistance measurement circuit.

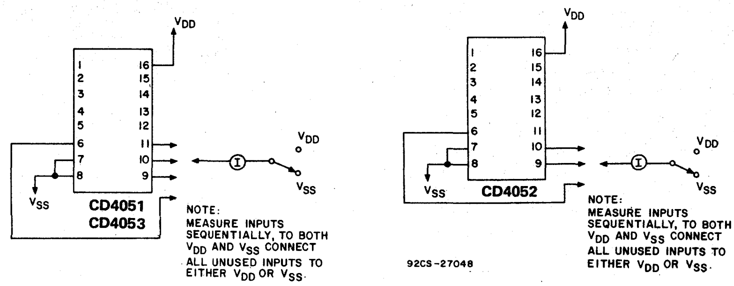


Fig. 23 – Input current.

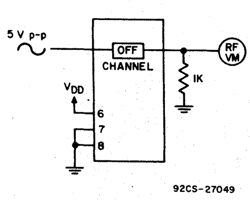


Fig.24 – Feedthrough (all types).

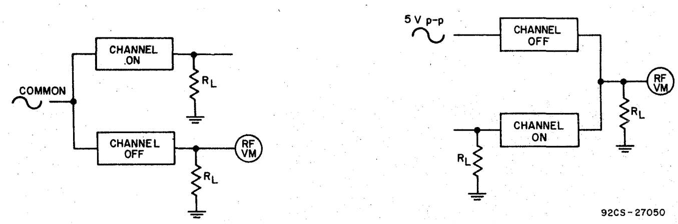


Fig.25 – Crosstalk between any two channels (all types).

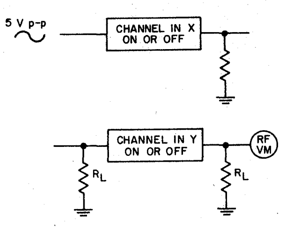


Fig.26 – Crosstalk between duals or triplets (CD4052B, CD4053B).

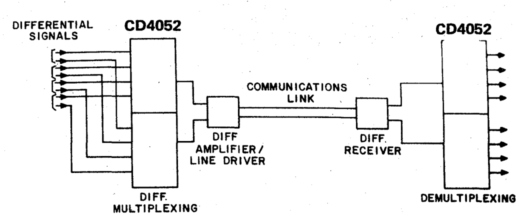


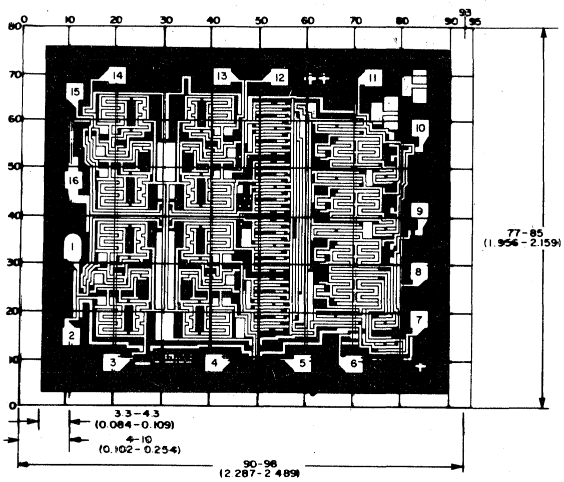
Fig.27 – Typical time-division application of the CD4052B.

SPECIAL CONSIDERATIONS

In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4051B, CD4052B, or CD4053B.

When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned ON or OFF by an address input, there is a momentary conductive path from the channel to V_{EE}, which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning ON a channel will similarly dump some charge to V_{EE}.

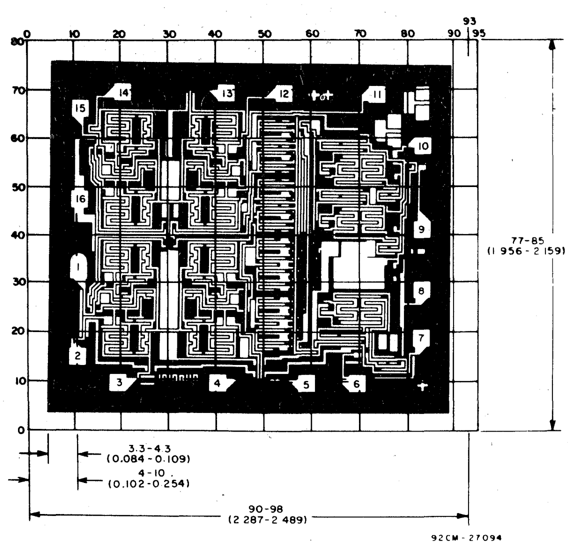
The amount of charge dumped is mostly a function of the signal level above V_{EE}. Typically, at V_{DD}-V_{EE} = 10 V, a 100 pF capacitor connected to the input or output of the channel will lose 3-4 % of its voltage at the moment the channel turns ON or OFF. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1-2 µs. When the inhibit signal turns a channel OFF, there is no charge dumping to V_{EE}. Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.



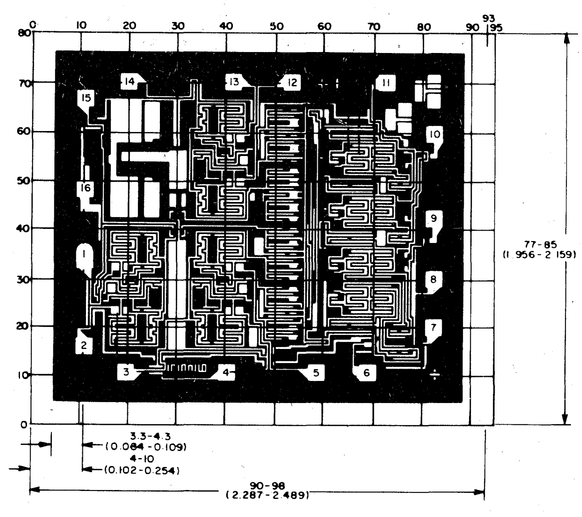
Dimensions and pad layout for CD4051BH. 92CM-27093

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid Graduations are in Mils (10^{-3} inch).



Dimensions and pad layout for CD4052BH.



Dimensions and pad layout for CD4053BH.

COS/MOS Liquid-Crystal Display Drivers

High-Voltage Types (20-Volt Rating)

CD4054B – 4-Segment Display Driver
CD4055B – BCD to 7-Segment Decoder/Driver with "Display-Frequency" Output
CD4056B – BCD to 7-Segment Decoder/Driver with Strobed-Latch Function

The RCA CD4055B and CD4056B types are single-digit BCD-to-7-segment decoder/driver circuits that provide level-shifting functions on the chip. This feature permits the BCD input-signal swings (V_{DD} to V_{SS}) to be the same as or different from the 7-segment output-signal swings (V_{DD} to V_{EE}). For example, the BCD input-signal swings (V_{DD} to V_{SS}) may be as small as 0 to –3 V, whereas the output-display drive-signal swing (V_{DD} to V_{EE}) may be as large as from 0 to –15V. If V_{DD} to V_{EE} exceeds 15 V, V_{DD} to V_{SS} should be at least 4V (0 to –4V).

The 7-segment outputs are controlled by the DISPLAY-FREQUENCY (DF) input which causes the selected segment outputs to be low, high, or a square-wave output (for liquid-crystal displays). When the DF input is low the output segments will be high when selected by the BCD inputs. When the DF input is high, the output segments will be low when selected by the BCD inputs. When a square-wave is present at the DF input, the selected segments will have a square-wave output that is 180° out of phase with the DF input. Those segments which are not selected will have a square-wave output that is in phase with the input. DF square-wave repetition rates for liquid-crystal displays usually range from 30 Hz (well above flicker rate) to 200 Hz (well below the upper limit of the liquid-crystal frequency response). The CD4055B provides a level-shifted high-amplitude DF output which is required for driving the common electrode in liquid-crystal displays. The CD4056B provides a strobed-latch function at the BCD inputs. Decoding of all input combinations on the CD4055B and CD4056B provides displays of 0 to 9 as well as L, P, H, A, –, and a blank position.

The CD4054B provides level shifting similar to the CD4055B and CD4056B independently strobed latches, and common DF control on 4 signal lines. The CD4054B is intended to provide drive-signal compatibility with the CD4055B and CD4056B 7-segment decoder types for the decimal point, colon, polarity, and similar display lines. A level-shifted high-amplitude DF output can be obtained from any CD4054B output line by connecting the corresponding input and strobe lines to a low and high level, respectively and applying a square wave to DF_{IN}. The CD4054B may also be utilized for logic-level "up conversion" or "down conversion". For example, input-signal swings (V_{DD} to V_{SS}) from +5 to 0 V can be converted to output-signal swings (V_{DD} to V_{EE}) of +5 to –5 V. The level-shifted function on all three types permits the use of different input- and output-signal swings. The input swings from a low level of V_{SS} to a high level of V_{DD} while the output swings from a low level of V_{EE} to the same high level of V_{DD}. Thus, the input and output swings can be selected independently of each other over a 3-to-18 V range. V_{SS} may be connected to V_{EE} when no level-shift function is required.

For the CD4054B and CD4056B, data are transferred from input to output by placing a high voltage level at the strobe input. A low voltage level at the strobe input latches the data input and the corresponding output segments remain selected (or non-selected) while the strobe is low.

Whenever the level-shifting function is required, the CD4055B can be used by itself to drive a liquid-crystal display (Fig.16 and Fig.20). The CD4056B, however, must be used together with a CD4054B to provide the common DF output (Fig.19). The capability of extending the voltage swing on the negative end (this voltage cannot be extended on the positive end) can be used to advantage in the setup of Fig.18. Fig.17 is common to all three types.

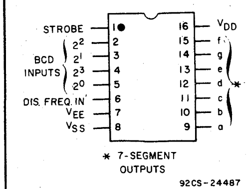
The CD4054B-, CD4055B-, and CD4056B-series types are available in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

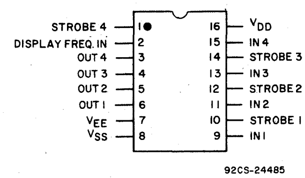
- **Operation of liquid crystals with COS/MOS circuits provides ultra-low-power displays**
- **Equivalent ac output drive for liquid-crystal displays – no external capacitor required**
- **Voltage doubling across display, e.g. $V_{DD} - V_{EE}$ = 18 V results in effective 36 V p-p drive across selected display segments**
- **Low- or high-output level dc drive for other types of displays**
- **On-chip logic-level conversion for different input- and output-level swings**
- **Full decoding of all input combinations: 0-9, L, H, P, A,–, and blank positions**
- **Strobed-latch function–CD4054B Series and CD4056B Series**
- **DISPLAY-FREQUENCY (DF) output for liquid-crystal common-line drive signal– CD4055B Series (CD4054B Series also: see introductory text)**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package temperature range):**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **5-V, 10-V, and 15-V parametric ratings**

Applications

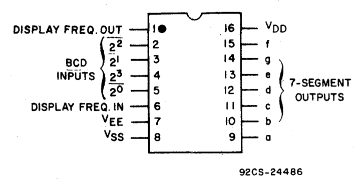
- **General-purpose displays**
- **Calculators and meters**
- **Wall and table clocks**
- **Industrial control panels**
- **Portable lab instruments**
- **Panel meters**
- **Auto dashboard displays**
- **Appliance control panels**



CD4056B Terminal Assignment



CD4054B Terminal Assignment



CD4055B Terminal Assignment

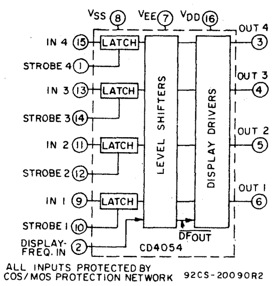
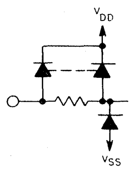


Fig.1 — CD4054B functional diagram.



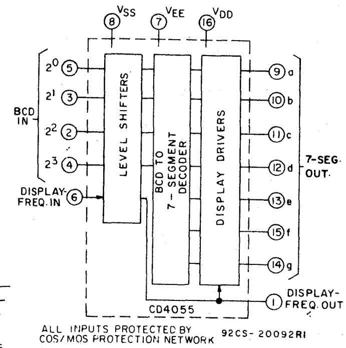


Fig.2 — CD4055B functional diagram.

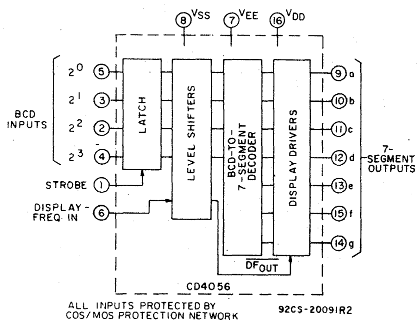


Fig.3 — CD4056B functional diagram.

TRUTH TABLE FOR CD4055B and CD4056B

INPUT CODE				OUTPUT STATE							DISPLAY CHARACTER
2^3	2^2	2^1	2^0	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	
0	0	0	1	0	1	1	0	0	0	0	
0	0	1	0	1	1	0	1	1	0	1	
0	0	1	1	1	1	1	1	0	0	1	
0	1	0	0	0	1	1	0	0	1	1	
0	1	0	1	1	0	1	1	0	1	1	
0	1	1	0	1	0	1	1	1	1	1	
0	1	1	1	1	1	1	0	0	0	0	
1	0	0	0	1	1	1	1	1	1	1	
1	0	0	1	1	1	1	1	0	1	1	
1	0	1	0	0	0	0	1	1	1	0	
1	0	1	1	0	1	1	0	1	1	1	
1	1	0	0	1	1	0	0	1	1	1	
1	1	0	1	1	1	1	0	1	1	1	
1	1	1	0	0	0	0	0	0	0	1	—
1	1	1	1	0	0	0	0	0	0	0	BLANK

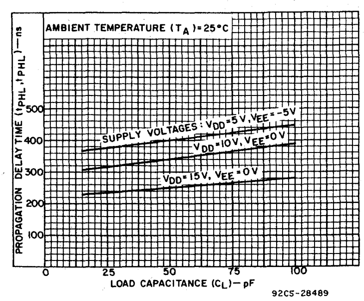


Fig.4 — Typical propagation delay time vs. load capacitance for CD4054B.

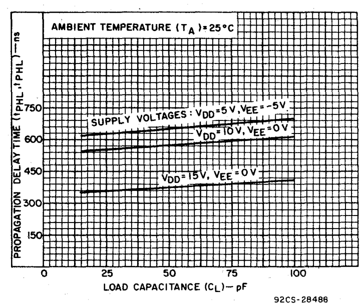


Fig.5 — Typical propagation delay time vs. load capacitance for CD4055 and CD4056B.

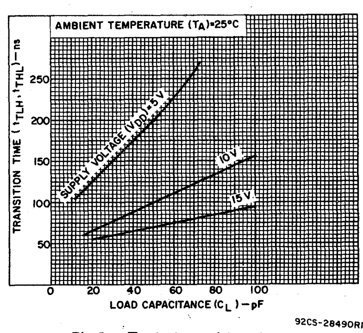


Fig.6 — Typical transition time vs. load capacitance.

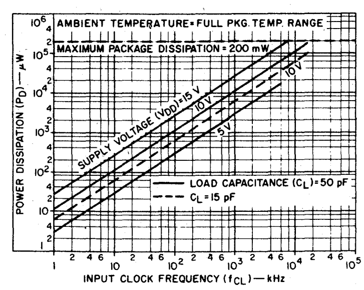


Fig.7 — Typical input clock frequency vs. power dissipation.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

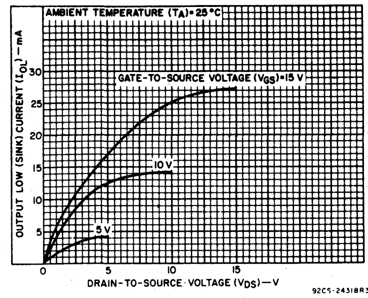


Fig.8 — Typical n-channel output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	CONDITIONS V_{EE} (V)	V_{SS} (V)	V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS Values at −55°,+25°,+125°C Apply to D,F,H Packages; Values at −40°,+25°,+85°C Apply to E Package −55°	−40°	+85°	+125°	+25°C Min.	Typ.	Max.	Units
Quiescent Device Current, I_{DD} MAX.	−5	0			5	5		150	150	–	0.04	5	μA
	0	0			10	10		300	300	–	0.04	10	
	0	0			15	20		600	600	–	0.04	20	
	0	0			20	100		3000	3000	–	0.08	100	
Output Voltage: Low Level, V_{OL} MAX.	0	0		0,5	5	0.05				–	0	0.05	V
	0	0		0,10	10	0.05				–	0	0.05	
	0	0		0,15	15	0.05				–	0	0.05	
High Level, V_{OH} MIN.	0	0		0,5	5	4.95				4.95	5	–	
	0	0		0,10	10	9.95				9.95	10	–	
	0	0		0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} MAX.	0	0	0.5, 4.5		5	1.5				–	–	1.5	V
	0	0	1,9		10	3				–	–	3	
	0	0	1.5,13.5		15	4				–	–	4	
Input High Voltage, V_{IH} MIN.	−5	0	0.5,4.5		5	3.5				3.5	–	–	
	0	0	1,9		10	7				7	–	–	
	0	0	1.5,13.5		15	11				11	–	–	
Output Low (Sink) Current, I_{OL}	5	0	4.5		5	0.98	0.92	0.67	0.55	0.8	1.6	–	mA
	0	0	0.5		10	0.98	0.92	0.67	0.55	0.8	1.6	–	
	0	0	1.5		15	3.6	3.4	2.4	2	2.9	5.8	–	
Output High (Source) Current, I_{OH}	−5	0	4.5		5	−0.6	−0.55	−0.35	−0.3	−0.45	−0.9	–	
	0	0	9.5		10	−0.6	−0.55	−0.35	−0.3	−0.45	−0.9	–	
	0	0	13.5		15	−1.9	−1.8	−1.2	−1.1	−1.5	−3	–	
Input Current, I_{IN}	0	0	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

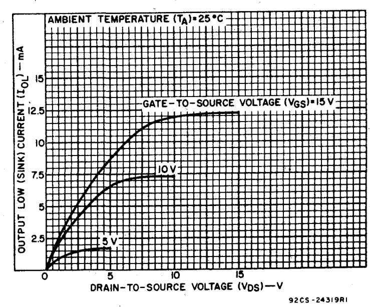


Fig.9 — Minimum n-channel output low (sink) current characteristics.

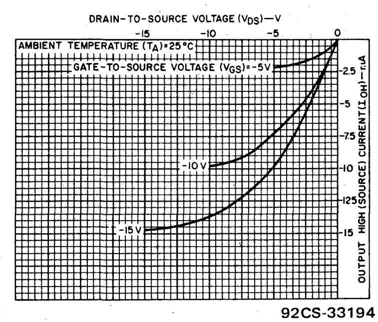


Fig.10 — Typical p-channel output high (source) current characteristics.

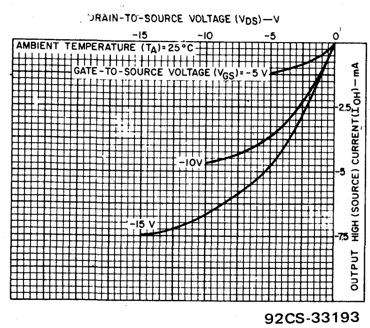


Fig. 13 — Minimum p-channel output high (source) current characteristics.

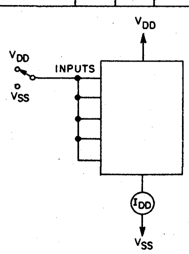


Fig. 11 — Quiescent-device-current test circuit.

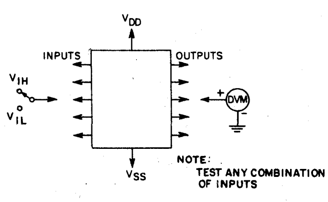


Fig. 12 — Input-voltage test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, $C_L = 50$ pF, Input $t_r, t_f = 20$ ns, $R_L = 200$ kΩ

CHARACTERISTIC	CONDITIONS V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS ALL PACKAGE TYPES CD4054 Typ.	CD4054 Max.	CD4055,CD4056 Typ.	CD4055,CD4056 Max.	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH} (Any Input to Any Output)	–5	0	5	400	800	650	1300	ns
	0	0	10	340	680	575	1150	
	0	0	15	250	500	375	750	
Transition Time, t_{THL}, t_{TLH} (Any Output)	–5	0	5	100	200	100	200	ns
	0	0	10	100	200	100	200	
	0	0	15	75	150	75	150	
Minimum Data Setup Time, t_S*	–5	0	5	110	220	110	220	ns
	0	0	10	50	100	50	100	
			15	35	70	35	70	
Minimum Strobe Pulse Width, t_W*	–5	0	5	110	220	110	220	ns
	0	0	10	50	100	50	100	
	0	0	15	35	70	35	70	
Input Capacitance, C_{IN} (Any Input)	–	–	–	5	7.5	5	7.5	pF

* CD4054 and CD4056 only.

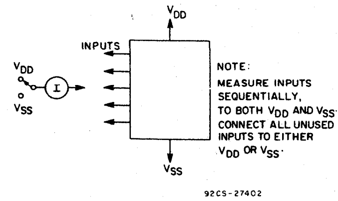


Fig. 14 – Input-current test circuit.

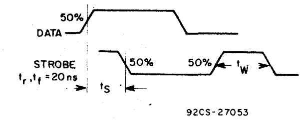


Fig. 15 – Data setup time and strobe pulse duration.

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^oC$ (Unless otherwise specified)
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply Voltage Range: (At T_A = Full Package Temperature Range)				3	18	V
Setup Time (t_s)●	–5	0	5	220	–	ns
	0	0	10	100	–	
	0	0	15	70	–	
Strobe Pulse Width (t_W)●	–5	0	5	220	–	ns
	0	0	10	100	–	
	0	0	15	70	–	

● For CD4054 and CD4056 only.

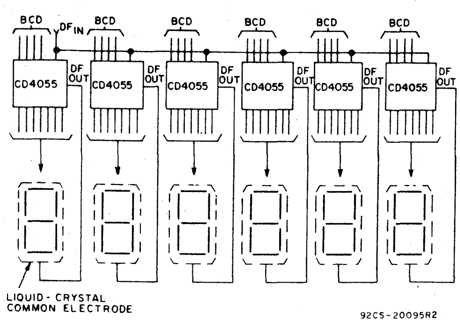


Fig. 16 – Clock display: $V_{DD} = 0$ V, $V_{SS} = -5$ V, $V_{EE} = -15$ V, $DF_{IN} = 30$ Hz square wave.

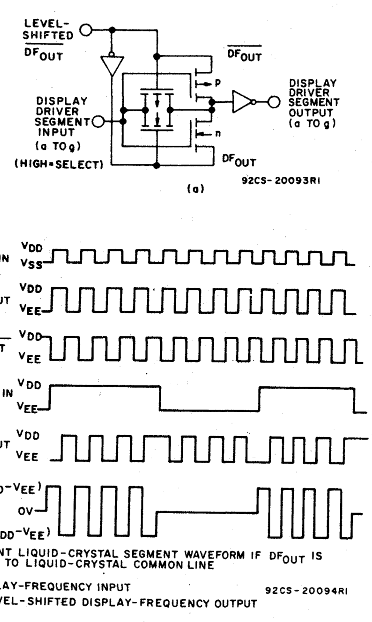


Fig. 17 – Display-driver circuit for one segment line and waveforms.

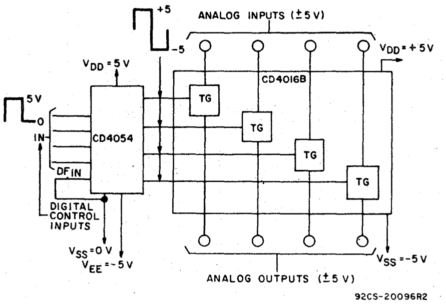


Fig.18 – Digital (0 to +5 V) to bidirectional analog control (+5 to –5 V) level shifter.

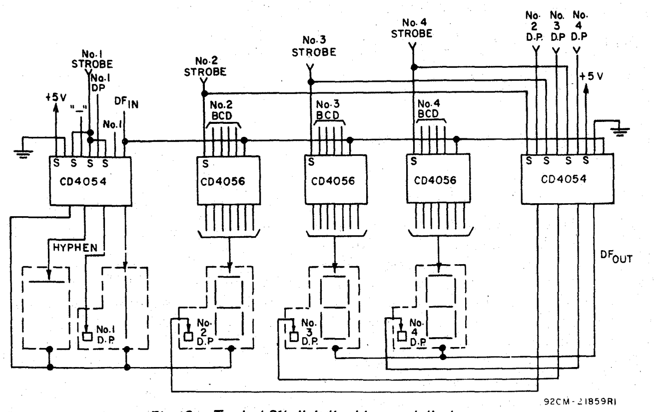
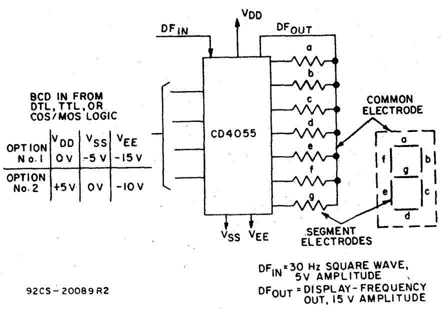


Fig.19 – Typical 3½-digit liquid-crystal display: V_{DD} = +5 V, V_{SS} = 0 V, V_{EE} = –10 V, DF_{IN} = 30 Hz square wave.



OPTION	V_{DD}	V_{SS}	V_{EE}
No. 1	0 V	-5 V	-15 V
No. 2	+5 V	0 V	-10 V

Fig.20 – Single-digit liquid-crystal display.

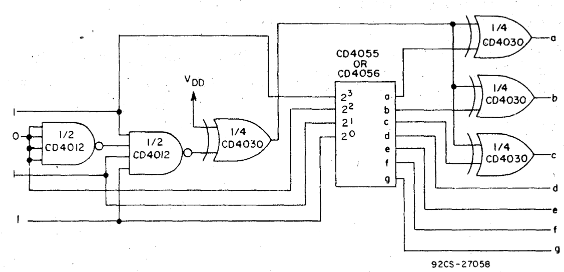


Fig.21 – Conversion of "H" display to "F" display.

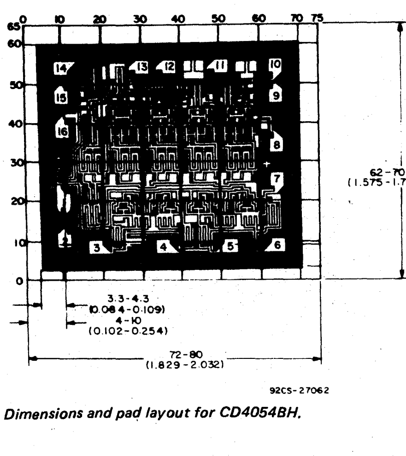
The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

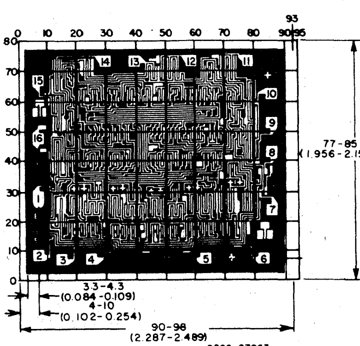
In addition to the letters L, H, P, and A (See the truth table), five other letters can be displayed through the use of simple logic circuits preceding and following the CD4055B or CD4056B devices. Fig.21 is an example of a circuit that converts an "H" display (code 1011) to an "F" display. One condition that must be met is that $V_{EE}=V_{SS}$. If $V_{EE} \neq V_{SS}$, the CD4054B must be used to level shift in the appropriate places.

In a similar manner the letters C, E, J, and U can be displayed. These circuits can also be used to drive LED displays provided the exclusive-OR gates have sufficient output-current drive.

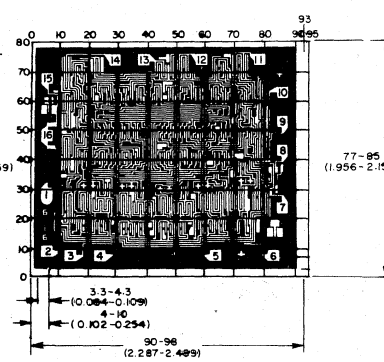
The letters B, D, G, I, O, and S may be represented by the codes for numbers 8, 0, 6, 1, 0, and 5, respectively, when there is pre-knowledge that only letters are to be displayed.



Dimensions and pad layout for CD4054BH.



Dimensions and pad layout for CD4055BH



Dimensions and pad layout for CD4056BH

CD4060B Types

COS/MOS 14-Stage Ripple-Carry Binary Counter/Divider and Oscillator

High-Voltage Types (20-Volt Rating)

The RCA-CD4060B consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which resets the counter to the all-O's state and disables the oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of ϕ_I (and ϕ_O). All inputs and outputs are fully buffered. Schmitt trigger action on the input-pulse line permits unlimited input-pulse rise and fall times.

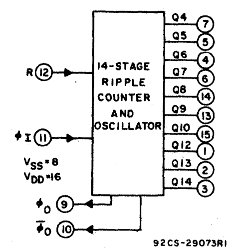
The CD4060B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **12 MHz clock rate at 15 V**
- **Common reset**
- **Fully static operation**
- **Buffered inputs and outputs**
- **Schmitt trigger input-pulse line**
- **100% tested for quiescent current at 20 V**
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for description of "B" Series CMOS Devices"**

Oscillator Features:

- **All active components on chip**
- **RC or crystal oscillator configuration**
- **RC oscillator frequency of 690 kHz min. at 15 V**



FUNCTIONAL DIAGRAM

Applications

- **Control counters**
- **Timers**
- **Frequency dividers**
- **Time-delay circuits**

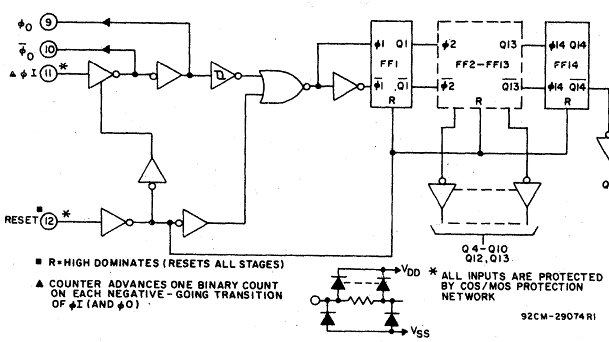


Fig. 1 – Logic diagram.

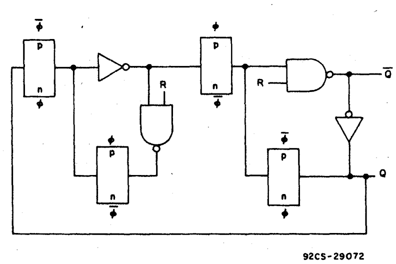


Fig. 2 – Detail of typical flip-flop stage.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	–0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	–55 to +125°C
PACKAGE TYPE E	–40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	–65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

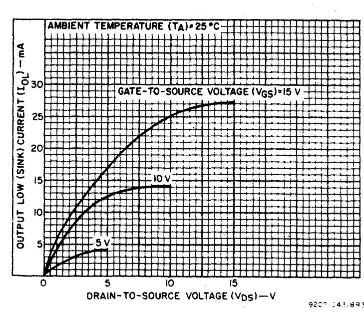


Fig. 3 – Typical n-channel output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages Values at –40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	µA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current*, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current*, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	µA

*Data not applicable to terminal 9 or 10.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

CHARACTERISTIC	V_{DD}	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	18	V
Input-Pulse Width, t_W (f = 100 kHz)	5 10 15	100 40 30	– – –	ns
Input-Pulse Rise Time and Fall Time, $t_{r\phi}$, $t_{f\phi}$	5 10 15	Unlimited		
Input-Pulse Frequency, $f_{\phi I}$ (External pulse source)	5 10 15	– – –	3.5 8 12	MHz
Reset Pulse Width, t_W	5 10 15	120 60 40	– – –	ns

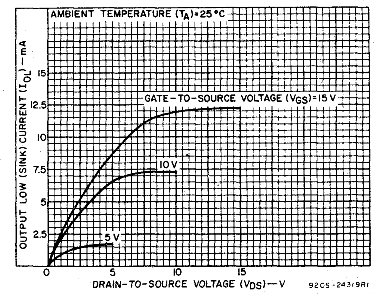


Fig. 4 – Minimum n-channel output low (sink) current characteristics.

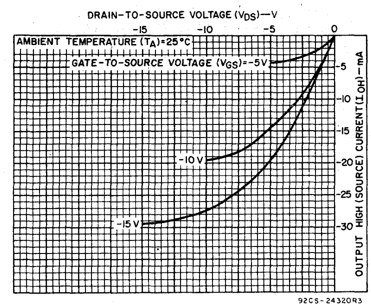


Fig. 5 – Typical p-channel output high (source) current characteristics.

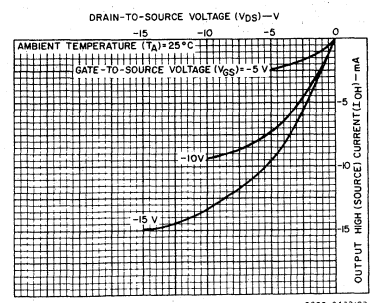


Fig. 6 – Minimum p-channel output high (source) current characteristics.

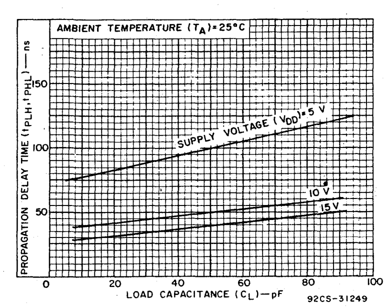


Fig. 7 – Typical propagation delay time (Q_n to Q_n+1) as a function of load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Input-Pulse Operation						
Propagation Delay Time, ϕ_I to Q4 Out; t_{PHL}, t_{PLH}		5	–	370	740	ns
		10	–	150	300	
		15	–	100	200	
Propagation Delay Time, Q_n to Q_{n+1}; t_{PHL}, t_{PLH}		5	–	100	200	
		10	–	50	100	
		15	–	40	80	
Transition Time, t_{THL}, t_{TLH}		5	–	100	200	
		10	–	50	100	
		15	–	40	80	
Min. Input-Pulse Width, t_W	f = 100 kHz	5	–	50	100	
		10	–	20	40	
		15	–	15	30	
Input-Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$		5	Unlimited			
		10				
		15				
Max. Input-Pulse Frequency, $f_{\phi I}$ (External pulse source)		5	3.5	7	–	MHz
		10	8	16	–	
		15	12	24	–	
Input Capacitance, C_I	Any Input		–	5	7.5	pF
Reset Operation						
Propagation Delay Time, t_{PHL}		5	–	180	360	ns
		10	–	80	160	
		15	–	50	100	
Minimum Reset Pulse Width, t_W		5	–	60	120	
		10	–	30	60	
		15	–	20	40	

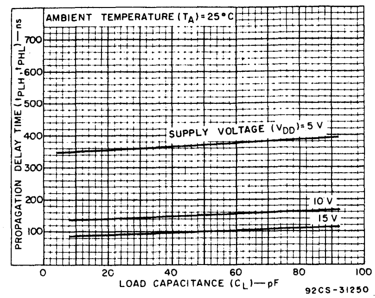


Fig. 8 — Typical propagation delay time (ϕ_I to Q_4 Output) as a function of load capacitance.

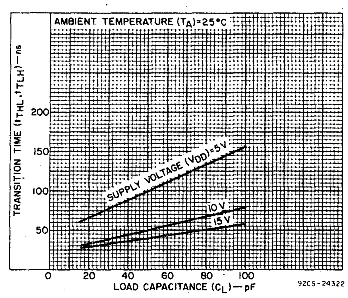


Fig. 9 — Typical transition time as a function of load capacitance.

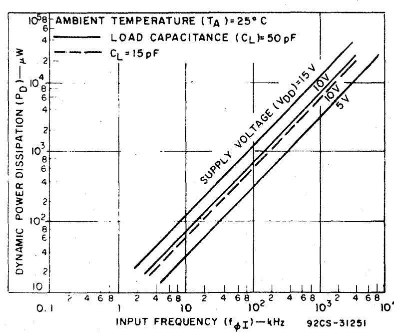


Fig. 10 — Typical dynamic power dissipation as a function of input frequency.

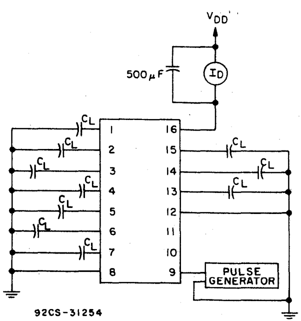


Fig. 11 — Dynamic power dissipation test circuit.

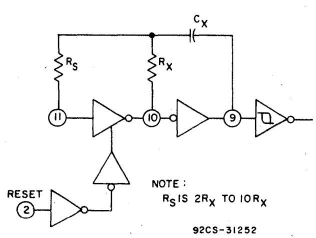


Fig. 12 — Typical RC circuit.

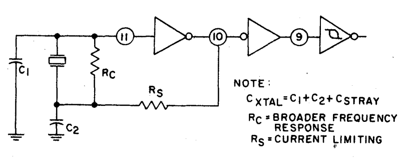


Fig. 13 — Typical crystal circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ [cont'd]

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
RC Operation						
Variation of Frequency (Unit-to-Unit)	C_X = 200 pF, R_S = 560 kΩ, R_X = 50 kΩ	5	18	21.5	25	kHz
		10	20	23	26	
		15	21.1	24	27	
Variation of Frequency with voltage change (Same Unit)	C_X = 200 pF, R_S = 560 kΩ, R_X = 50 kΩ	5V to 10 V	–	–	2	
		10V to 15V	–	–	1	
R_X max.	C_X = 10 μF	5	–	–	20	MΩ
	= 50 μF	10	–	–	20	
	= 10 μF	15	–	–	10	
C_X max.	R_X = 500 kΩ	5	–	–	1000	μF
	= 300 kΩ	10	–	–	50	
	= 300 kΩ	15	–	–	50	
Maximum Oscillator Frequency*	R_X = 5 kΩ, C_X = 15 pF	10	530	650	810	kHz
		15	690	800	940	
Drive Current at Pin 9 (For Oscillator Design) I_{OL}	V_O = 0.4 V	5	–	0.35	–	mA
	= 0.5 V	10	–	0.8	–	
	= 1.5 V	15	–	3	–	
I_{OH}	V_O = 4.6 V	5	–	–0.35	–	
	= 9.5 V	10	–	–0.8	–	
	= 13.5 V	15	–	–3	–	

* RC oscillator applications are not recommended at supply voltages below 7 V for R_X = 50 kΩ.

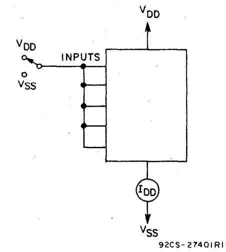


Fig. 14 – Quiescent device current.

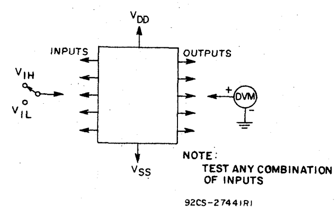


Fig. 15 – Input voltage.

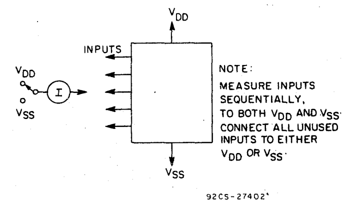
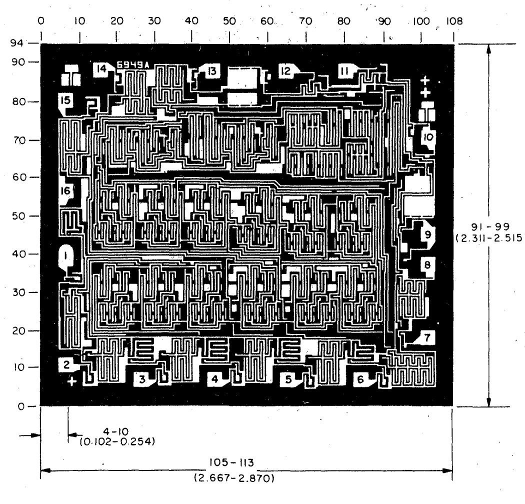


Fig. 16 – Input current.

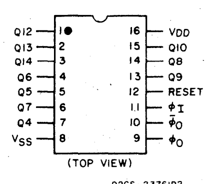


Dimensions and pad layout for CD4060B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

TERMINAL DIAGRAM



CD4063B Types

COS/MOS 4-Bit Magnitude Comparator

High Voltage Types (20-Volt Rating)

The RCA-CD4063B is a 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to", or "greater than" a second 4-bit word.

The CD4063B has eight comparing inputs (A3, B3, through A0, B0), three outputs (A < B, A = B, A > B) and three cascading inputs (A < B, A = B, A > B) that permit systems designers to expand the comparator function to 8, 12, 16 . . . 4N bits. When a single CD4063B is used, the cascading inputs are connected as follows: (A < B) = low, (A = B) = high, (A > B) = low.

For words longer than 4 bits, CD4063B devices may be cascaded by connecting the outputs of the less-significant comparator to the corresponding cascading inputs of the more-significant comparator. Cascading inputs (A < B, A = B, and A > B) on the least significant comparator are connected to a low, a high, and a low level, respectively.

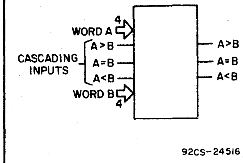
The CD4063B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix). This device is pin-compatible with the standard 7485 TTL type.

Features:

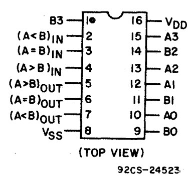
- **Expansion to 8, 12, 16....4N bits by cascading units**
- **Medium-speed operation:**
  compares two 4-bit words in 250 ns (typ.) at 10 V
- **100% tested for quiescent current at 20 V**
- **Standardized symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package temperature range)**
  range) = 1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Servo motor controls**
- **Process controllers**



FUNCTIONAL DIAGRAM



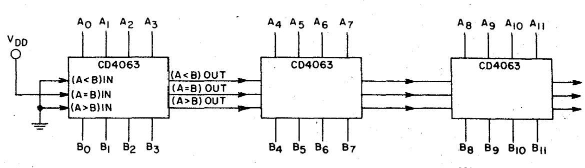
TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V



$t_{P\,TOTAL} = t_P \binom{COMPARE}{INPUTS} + 2 \times t_P \binom{CASCADE}{INPUTS}$, AT V_{DD} = 10V
(3 STAGES)

= 250 + (2 × 200) = 650 ns (TYP.)

Fig. 1 — Typical speed characteristics of a 12-bit comparator.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages; Values at −40, +25, +85 Apply to E Package: −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

TRUTH TABLE

INPUTS: COMPARING A3, B3	A2, B2	A1, B1	A0, B0	CASCADING A < B	A = B	A > B	OUTPUTS A < B	A = B	A > B
A3 > B3	X	X	X	X	X	X	0	0	1
A3 = B3	A2 > B2	X	X	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	0	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	0	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	1	0	0
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	1	0	0
A3 = B3	A2 < B2	X	X	X	X	X	1	0	0
A3 < B3	X	X	X	X	X	X	1	0	0

X = Don't Care Logic 1 ≡ High Level Logic 0 ≡ Low Level

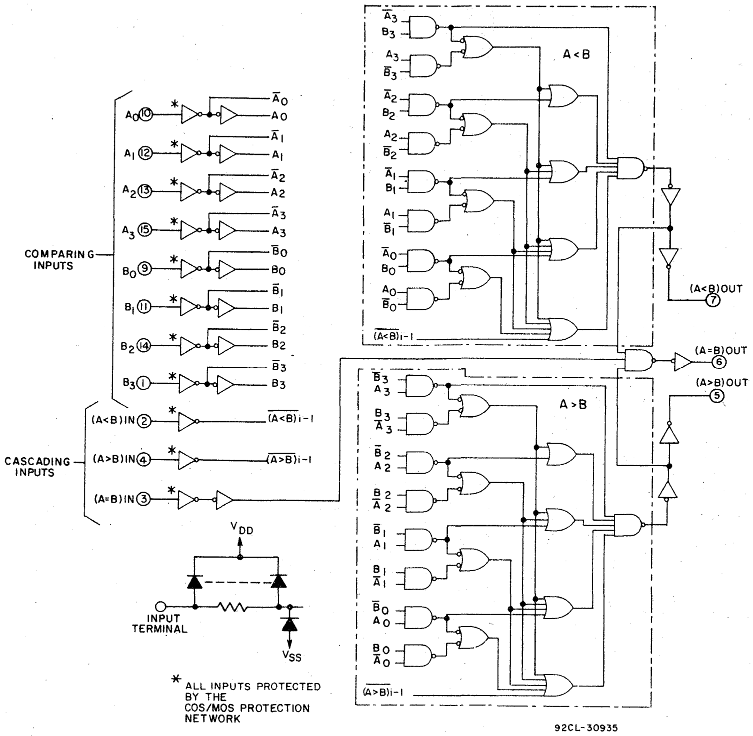


Fig. 2 – Logic diagram for CD4063B.

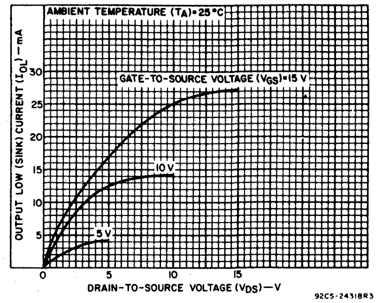


Fig. 3 – Typical output low (sink) current characteristics.

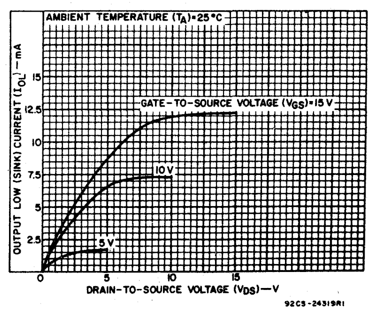


Fig. 4 – Minimum output low (sink) current characteristics.

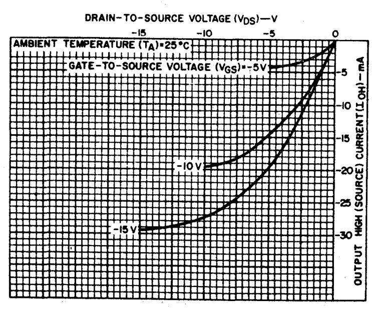


Fig. 5 – Typical output high (source) current characteristics.

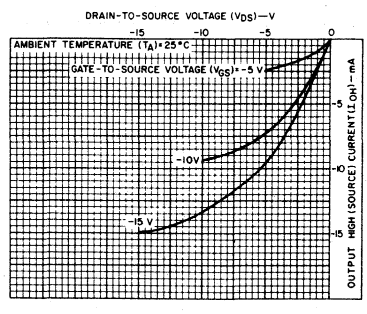


Fig. 6 – Minimum output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$; Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200k\Omega$

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} Volts	Typ.	Max.	
Propagation Delay Time: Comparing Inputs to Outputs, t_{PHL}, t_{PLH}		5	625	1250	ns
		10	250	500	
		15	175	350	
Cascading Inputs to Outputs, t_{PHL}, t_{PLH}		5	500	1000	
		10	200	400	
		15	140	280	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

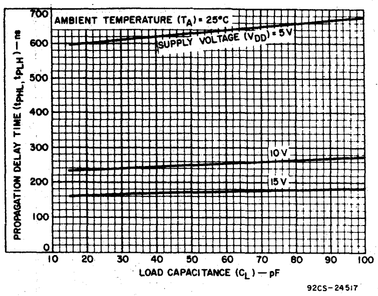


Fig. 7 — Typical propagation delay time vs. load capacitance ("comparing inputs" to outputs).

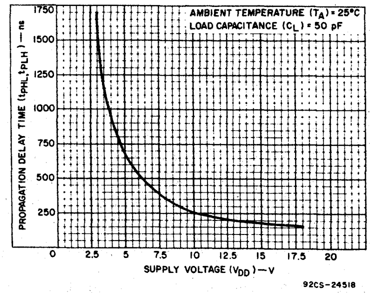


Fig. 8 — Typical propagation delay time vs. supply voltage ("comparing inputs" to outputs).

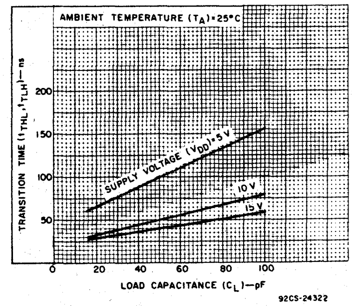


Fig. 9 — Typical transition time vs. load capacitance.

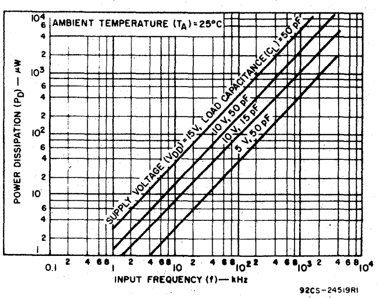


Fig. 10 — Typical power dissipation vs. frequency (see Fig. 12 — dynamic power dissipation test circuit).

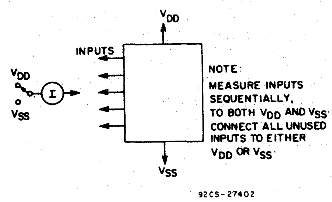


Fig. 11 — Input current test circuit.

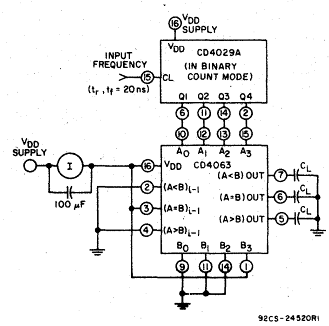


Fig. 12 — Dynamic power dissipation test circuit.

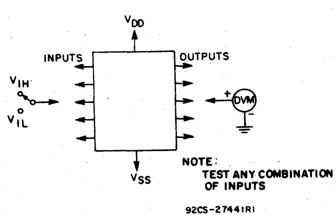


Fig. 13 — Input-voltage test circuit.

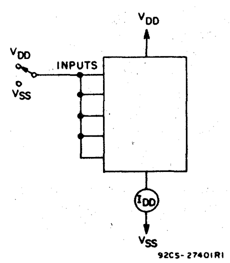
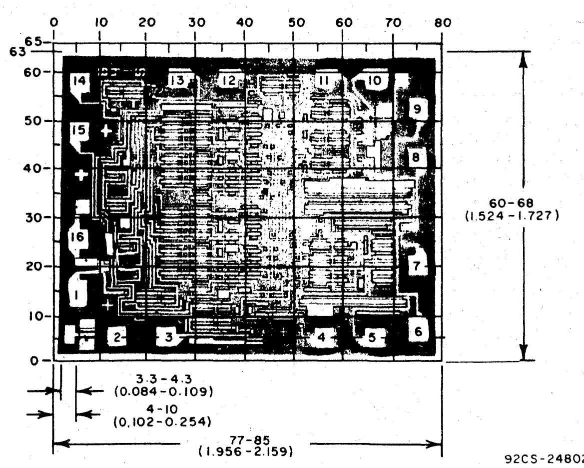


Fig. 14 — Quiescent-device-current test circuit.



Dimensions and pad layout for CD4063BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4066B Types

COS/MOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

High-Voltage Types (20-Volt Rating)

The RCA-CD4066B is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with RCA-CD4016B, but exhibits a much lower on-state resistance. In addition, the on-state resistance is relatively constant over the full input-signal range.

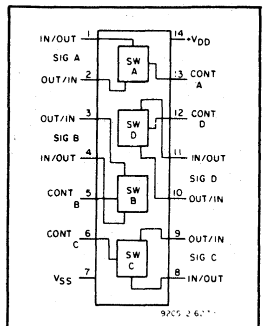
The CD4066B consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased on or off simultaneously by the control signal. As shown in Fig.1, the well of the n-channel device on each switch is either tied to the input when the switch is on or to V_{SS} when the switch is off. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the on-state resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant on-state impedance over the input-signal range. For sample-and-hold applications, however, the CD4016B is recommended.

The CD4066B is available in 14-lead ceramic dual-in-line packages (D and F suffixes), 14-lead plastic dual-in-line packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **15-V digital or ±7.5-V peak-to-peak switching**
- **125Ω typical on-state resistance for 15-V operation**
- **Switch on-state resistance matched to within 5 Ω over 15-V signal-input range**
- **On-state resistance flat over full peak-to-peak signal range**
- **High on/off output-voltage ratio: 80 dB typ. @ f_{is} = 10 kHz, R_L = 1 kΩ**
- **High degree of linearity: <0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 Vp-p, $V_{DD} - V_{SS} \geqslant 10$ V, R_L = 10 kΩ**
- **Extremely low off-state switch leakage resulting in very low offset current and high effective off-state resistance: 10 pA typ. @ $V_{DD} - V_{SS}$ = 10 V, T_A = 25°C**
- **Extremely high control input impedance (control circuit isolated from signal circuit): 10^{12} Ω typ.**
- **Low crosstalk between switches: –50 dB typ. @ f_{is} = 8 MHz, R_L = 1 kΩ**
- **Matched control-input to signal-output capacitance: Reduces output signal transients**
- **Frequency response, switch on = 40 MHz (typ.)**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of "B" Series CMOS Devices"**



FUNCTIONAL DIAGRAM

Applications:

- **Analog signal switching/multiplexing**
  - **Signal gating** **Modulator**
  - **Squelch control** **Demodulator**
  - **Chopper** **Commutating switch**
- **Digital signal switching/Multiplexing**
- **Transmission-gate logic implementation**
- **Analog-to-digital & digital-to-analog conversion**
- **Digital control of frequency, impedance, phase, and analog-signal gain**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT (except for TRANSMISSION GATE which is 25 mA) . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D, F) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . . +265°C

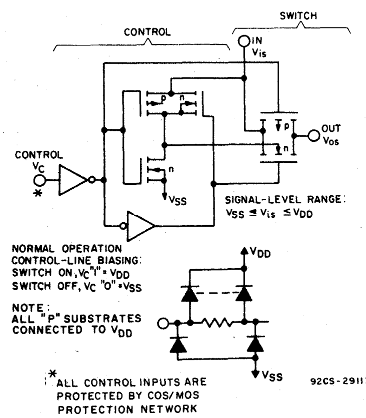


Fig. 1 – Schematic diagram of 1 of 4 identical switches and its associated control circuitry.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

ELECTRICAL CHARACTERISTICS

Characteristic	Test Conditions	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages. Values at −40, +25, +85 Apply to E Package: −55	−40	+85	+125	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD}		0,5	5	0.25	0.25	7.5	7.5	0.01	0.25	μA
		0,10	10	0.5	0.5	15	15	0.01	0.5	μA
		0,15	15	1	1	30	30	0.01	1	μA
		0,20	20	5	5	150	150	0.02	5	μA
Signal Inputs (V_{is}) and Output (V_{os})										
On-State Resistance, r_{on} Max.	$V_C = V_{DD}$, $R_L = 10\ k\Omega$ returned to $\frac{V_{DD} - V_{SS}}{2}$, $V_{is} = V_{SS}$ to V_{DD}		5	800	850	1200	1300	470	1050	Ω
			10	310	330	500	550	180	400	Ω
			15	200	210	300	320	125	240	Ω
ΔOn-State Resistance Between Any 2 Switches, Δr_{on}	$R_L = 10\ k\Omega$, $V_C = V_{DD}$		5	–	–	–	–	15	–	Ω
			10	–	–	–	–	10	–	Ω
			15	–	–	–	–	5	–	Ω
Total Harmonic Distortion, THD	$V_C = V_{DD} = 5\ V$, $V_{SS} = -5\ V$, $V_{is(p\text{-}p)} = 5\ V$ (Sine wave centered on 0 V) $R_L = 10\ k\Omega$, $f_{is} = 1$ kHz sine wave			–	–	–	–	0.4	–	%
−3dB Cutoff Frequency (Switch on)	$V_C = V_{DD} = 5\ V$, $V_{SS} = -5\ V$, $V_{is(p\text{-}p)} = 5\ V$ (Sine wave centered on 0 V $R_L = 1\ k\Omega$,			–	–	–	–	40	–	MHz
−50dB Feed-through Frequency (Switch off)	$V_C = V_{SS} = -5\ V$, $V_{is(p\text{-}p)} = 5\ V$ Sine wave centerd on 0 V $R_L = 1\ k\Omega$			–	–	–	–	1	–	MHz
Input/Output Leakage Current (Switch off) I_{is} Max.	$V_C = 0\ V$ $V_{is} = 18\ V$; $V_{os} = 0\ V$, $V_{is} = 0V$; $V_{os} = 18\ V$		18	±0.1	±0.1	±1	±1	$\pm10^{-5}$	±0.1	μA
−50 dB Crosstalk Frequency	$V_C(A) = V_{DD} = +5\ V$, $V_C(B) = V_{SS} = -5\ V$, $V_{is}(A) = 5\ V_{p\text{-}p}$, 50 Ω source $R_L = 1\ k\Omega$			–	–	–	–	8	–	MHz
Propagation Delay (Signal Input to Signal Output) t_{pd}	$R_L = 200\ k\Omega$ $V_C = V_{DD}$, $V_{SS} = GND$, $C_L = 50\ pF$ $V_{is} = 10\ V$ (Square wave centered on 5 V t_r, $t_f = 20$ ns		5	–	–	–	–	20	40	ns
			10	–	–	–	–	10	20	ns
			15	–	–	–	–	7	15	ns
Capacitance: Input, C_{is}	$V_{DD} = +5\ V$ $V_C = V_{SS} = -5\ V$			–	–	–	–	8	–	pF
Output, C_{os}				–	–	–	–	8	–	pF
Feedthrough, C_{ios}				–	–	–	–	0.5	–	pF

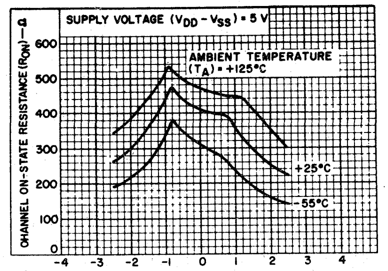


Fig. 2— Typical on-state resistance vs. input signal voltage (all types).

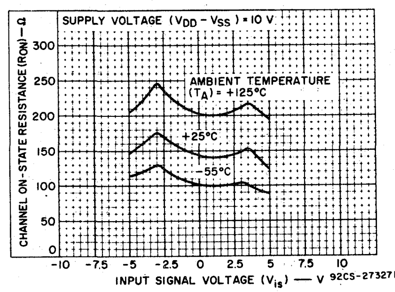


Fig. 3— Typical on-state vs. input signal voltage (all types).

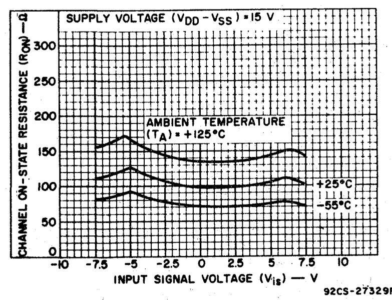


Fig. 4— Typical on-state resistance vs. input signal voltage (all types).

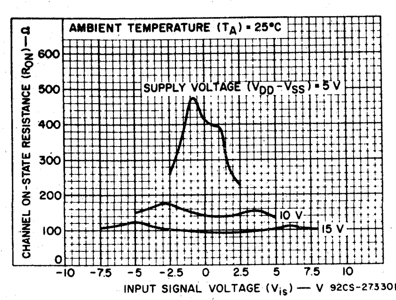


Fig. 5— on-state resistance vs. input signal voltage (all types).

ELECTRICAL CHARACTERISTICS (cont'd)

Characteristic	Test Conditions	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D, F, H Packages Values at –40, +25, +85 Apply to E Package –55	–40	+85	+125	+25 Typ.	+25 Max.	UNITS
Control (V_C)									
Control Input Low Voltage, V_{ILC} Max.	$\|I_{is}\| < 10 \mu A$ $V_{is} = V_{SS}, V_{OS} = V_{DD}$ and $V_{is} = V_{DD}, V_{OS} = V_{SS}$	5	1	1	1	1	–	1	V
		10	2	2	2	2	–	2	
		15	2	2	2	2	–	2	
Control Input High Voltage, V_{IHC}	See Fig. 2	5	3.5 (Min.)						V
		10	7 (Min.)						
		15	11 (Min.)						
Input Current, I_{IN} Max.	$V_{is} \leq V_{DD}$ $V_{DD} - V_{SS} = 18\ V$ $V_{CC} \leq V_{DD} - V_{SS}$	18	±0.1	±0.1	±1	±1	$\pm 10^{-5}$	±0.1	µA
Crosstalk (Control Input to Signal Output)	$V_C = 10\ V$ (Sq. Wave) $t_r, t_f = 20$ ns $R_L = 10\ k\Omega$	10	–	–	–	–	50	–	mV
Turn-On Propagation Delay	$V_{IN} = V_{DD}$ $t_r, t_f = 20$ ns $C_L = 50$ pF $R_L = 1\ k\Omega$	5	–	–	–	–	35	70	ns
		10	–	–	–	–	20	40	
		15	–	–	–	–	15	30	
Maximum Control Input Repetition Rate	$V_{is} = V_{DD}, V_{SS} = GND$, $R_L = 1\ k\Omega$ to gnd, $C_L = 50$ pF, $V_C = 10$ V(Square wave centered on 5 V) $t_r, t_f = 20$ ns, $V_{os} = ½ V_{os}$ @ 1 kHz	5	–	–	–	–	6	–	MHz
		10	–	–	–	–	9	–	
		15	–	–	–	–	9.5	–	
Input Capacitance, C_{IN}			–	–	–	–	5	7.5	µF

V_{DD} (V)	V_{is} (V)	Switch Input I_{is} (mA) –55°C	–40°C	+25°C	+85°C	+125°C	Switch Output, V_{os} (V) Min.	Max.
5	0	0.64	0.61	0.51	0.42	0.36	–	0.4
5	5	–0.64	–0.61	–0.51	–0.42	–0.36	4.6	–
10	0	1.6	1.5	1.3	1.1	0.9	–	0.5
10	10	–1.6	–1.5	–1.3	–1.1	–0.9	9.5	–
15	0	4.2	4	3.4	2.8	2.4	–	1.5
15	15	–4.2	–4	–3.4	–2.8	–2.4	13.5	–

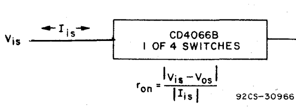


Fig. 6— Determination of r_{on} as a test condition for control input high voltage (V_{IHC}) specification.

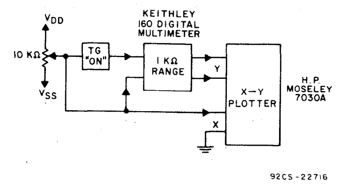


Fig. 7 – Channel on-state resistance measurement circuit.

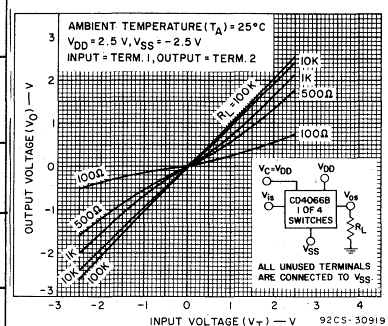


Fig. 8 – Typical r_{on} characteristics for 1 of 4 channels.

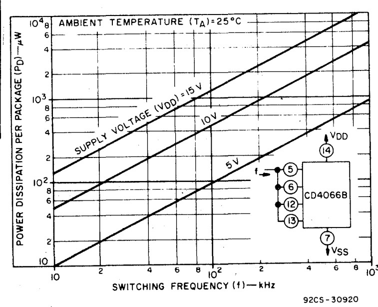


Fig. 9 – Power dissipation per package vs. switching frequency.

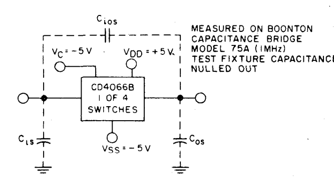


Fig. 10 – Capacitance test circuit.

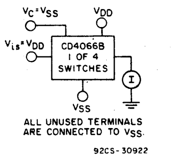


Fig. 11 – Off-switch input or output leakage.

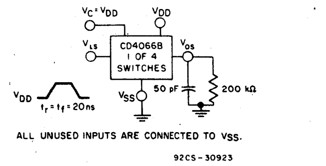


Fig. 12 – Propagation delay time signal input (V_{is}) to signal output (V_{os}).

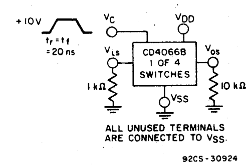


Fig. 13 – Crosstalk-control input to signal output.

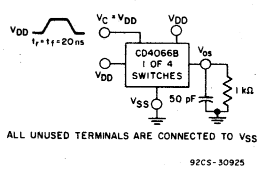


Fig. 14 – Propagation delay t_{PLH}, t_{PHL} control-signal output. Delay is measured at V_{os} level of +10% from ground (turn-on) or on-state output level (turn-off).

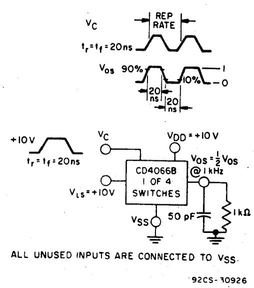


Fig. 15 – Maximum allowable control input repetition rate.

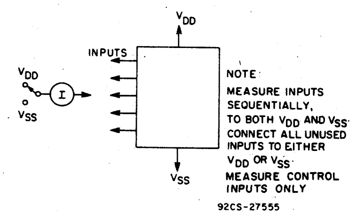


Fig. 16 – Input leakage current test circuit.

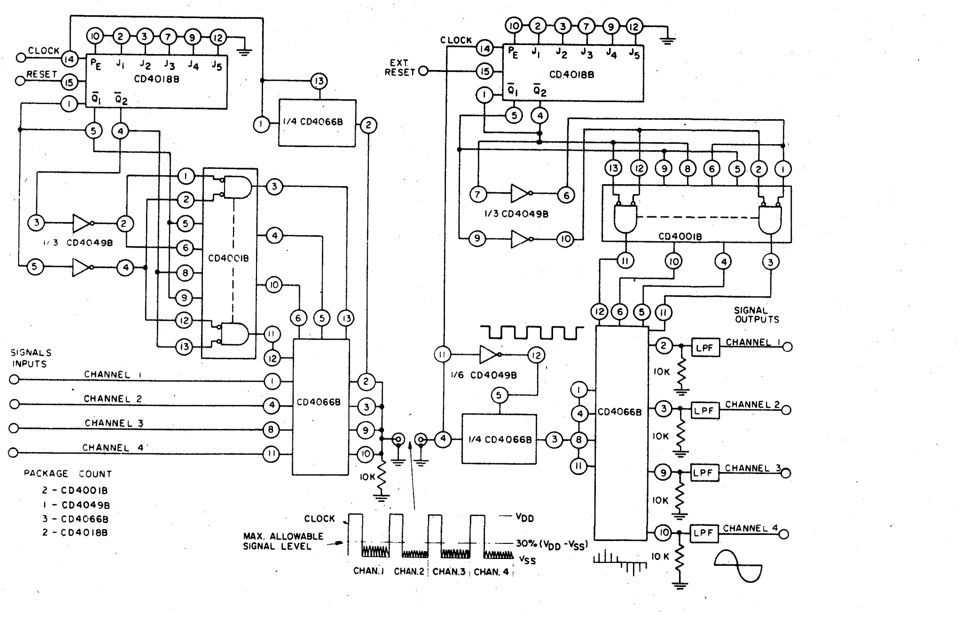


Fig. 17– 4-channel PAM multiplex system diagram.

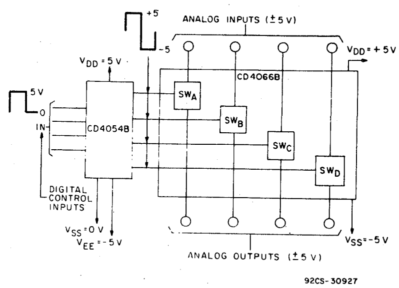
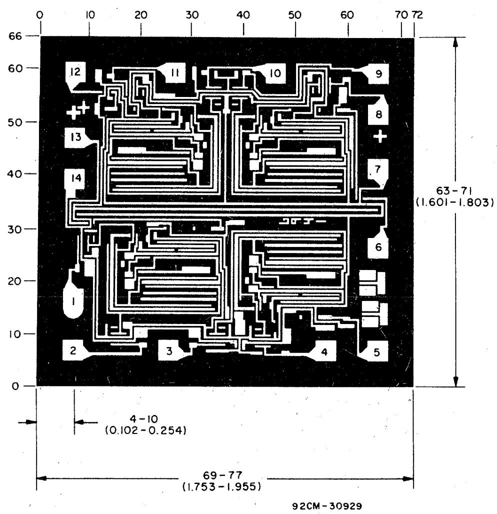


Fig. 18 — Bidirectional signal transmission via digital control logic.



CD4066BH
CHIP PHOTOGRAPH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

SPECIAL CONSIDERATIONS — CD4066B

1. In applications that employ separate power sources to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the four CD4066B bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4066B.

2. In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1,4,8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volts (calculated from R_{ON} values shown).
   No V_{DD} current will flow through R_L if the switch current flows into terminals 2,3,9, or 10.

COS/MOS Analog Multiplexers/Demultiplexers

High-Voltage Types (20-Volt Rating)

CD4067B – Single 16-Channel Multiplexer/Demultiplexer

CD4097B – Differential 8-Channel Multiplexer/Demultiplexer

The RCA-CD4067B and CD4097B COS/MOS analog multiplexers/demultiplexers* are digitally controlled analog switches having low ON impedance, low OFF leakage current, and internal address decoding. In addition, the ON resistance is relatively constant over the full input-signal range.

The CD4067B is a 16-channel multiplexer with four binary control inputs, A,B,C,D, and an inhibit input, arranged so that any combination of the inputs selects one switch.

The CD4097B is a differential 8-channel multiplexer having three binary control inputs A, B, C, and an inhibit input. The inputs permit selection of one of eight pairs of switches.

A logic "1" present at the inhibit input turns all channels off.

The CD4067 and CD4097 are supplied in 24-lead dual-in-line welded-seal ceramic packages (D suffix), 24-lead dual-in-line frit-seal ceramic packages (F suffix), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

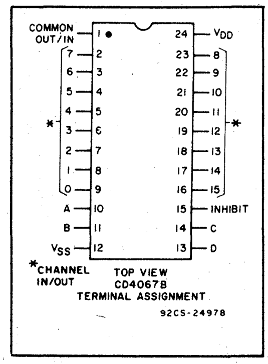
*When these devices are used as demultiplexers, the channel in/out terminals are the outputs and the common out/in terminals are the inputs.

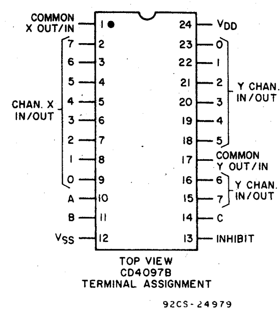
Features:

- Low ON resistance: 125 Ω (typ.) over 15 $V_{p\text{-}p}$ signal-input range for $V_{DD}-V_{SS}$=15 V
- High OFF resistance: channel leakage of ±10 pA (typ.) @ $V_{DD}-V_{SS}$=10 V
- Matched switch characteristics: R_{ON}=5 Ω (typ.) for $V_{DD}-V_{SS}$=15 V
- Very low quiescent power dissipation under all digital-control input and supply conditions: 0.2 μW (typ.) @ $V_{DD}-V_{SS}$=10 V
- Binary address decoding on chip
- 5-V, 10-V, and 15-V parametric ratings
- 100% tested for quiescent current at 20 V
- Standardized symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Analog and digital multiplexing and demultiplexing
- A/D and D/A conversion
- Signal gating





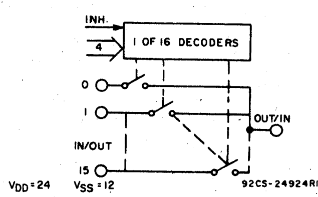


Fig. 1 – CD4067 functional diagram.

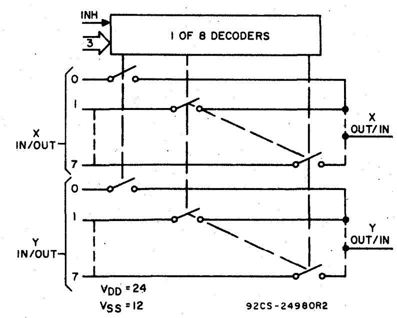


Fig. 2–CD4097 functional diagram.

Recommended Operating Conditions at T_A = 25°C (Unless Otherwise Specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted.

Characteristic	Min.	Max.	Units
Supply-Voltage Range (T_A=Full Package-Temp. Range)	3	18	V
Multiplexer Switch Input Current Capability	–	25	mA
Output Load Resistance	100	–	Ω

NOTE:

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 1 on the CD4067; terminals 1 and 17 on the CD4097.

CD4067 TRUTH TABLE

A	B	C	D	Inh	Selected Channel
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

CD4097 TRUTH TABLE

A	B	C	Inh	Selected Channel
X	X	X	1	None
0	0	0	0	0X, 0Y
1	0	0	0	1X, 1Y
0	1	0	0	2X, 2Y
1	1	0	0	3X, 3Y
0	0	1	0	4X, 4Y
1	0	1	0	5X, 5Y
0	1	1	0	6X, 6Y
1	1	1	0	7X, 7Y

CD4067B, CD4097B Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_{is} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS at Indicated Temperature (°C) Values at −55,+25,+125,apply to D,H pkg Values at −40,+25,+85,apply to E pkg −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	Units
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{OS})											
Quiescent Device Current, I_{DD} Max.			5	5	5	150	150	–	0.04	5	µA
			10	10	10	300	300	–	0.04	10	
			15	20	20	600	600	–	0.04	20	
			20	100	100	3000	3000	–	0.08	100	
ON-state Resistance $V_{SS} \leq V_{is} \leq V_{DD}$ r_{on} Max.		0	5	800	850	1200	1300	–	470	1050	Ω
		0	10	310	330	520	550	–	180	400	
		0	15	200	210	300	320	–	125	240	
Change in on-state Resistance (Between Any Two Channels) Δr_{on}		0	5	–	–	–	–	–	15	–	Ω
		0	10	–	–	–	–	–	10	–	
		0	15	–	–	–	–	–	5	–	
OFF Channel Leakage Current: Any Channel OFF Max. or All Channels OFF (Common OUT/IN) Max.		0	18	±100*		±1000*		–	±0.1	±100*	nA
Capacitance: Input, C_{is}		−5	5	–	–	–	–	–	5	–	pF
Output, C_{os} CD4067				–	–	–	–	–	55	–	
CD4097				–	–	–	–	–	35		
Feed-through, C_{ios}				–	–	–	–	–	0.2		
Propagation Delay Time (Signal Input to Output)	V_{DD} (pulse)	R_L = 200 KΩ, C_L=50 pF, t_r,t_f=20 ns	5	–	–	–	–	–	30	60	ns
			10	–	–	–	–	–	15	30	
			15	–	–	–	–	–	10	20	
CONTROL (ADDRESS or INHIBIT) V_C											
Input Low Voltage, V_{IL} Max.	=V_{DD} thru 1 KΩ	R_L=1 KΩ to V_{SS}, I_{IS}<2 µA on all OFF Channels	5	1.5				–	–	1.5	V
			10	3				–	–	3	
			15	4				–	–	4	
Input High Voltage, V_{IH} Min.			5	3.5				3.5	–	–	
			10	7				7	–	–	
			15	11				11	–	–	

* Determined by minimum feasible leakage measurement for automatic testing.

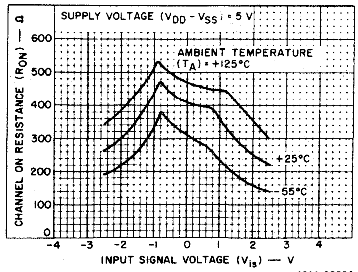


Fig. 3—Typical ON resistance vs. input signal voltage (all types).

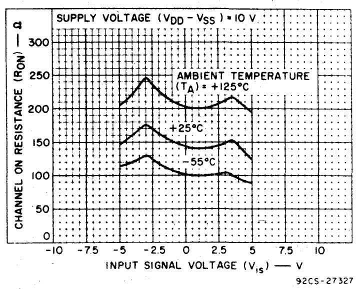


Fig. 4—Typical ON resistance vs. input signal voltage (all types).

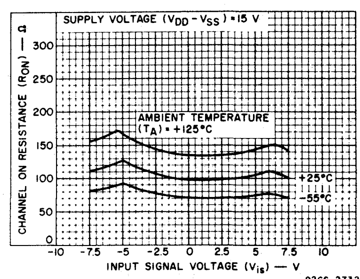


Fig. 5—Typical ON resistance vs. input signal voltage (all types).

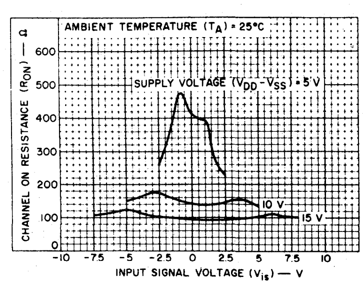


Fig. 6—Typical ON resistance vs. input signal voltage (all types).

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	CONDITIONS			LIMITS at Indicated Temperature (°C) Values at −55,+25,+125,apply to D,H pkg Values at −40,+25,+85,apply to E pkg							Units
	V_{is} (V)	V_{SS} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Input Current, I_{IN} Max.	V_{IN} = 0, 18 V		18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA
Propagation Delay Time: Address or Inhibit-to-Signal OUT (Channel turning ON)	R_L=10 KΩ,C_L=50 pF, t_r,t_f=20 ns										ns
		0	5	–	–	–	–	–	325	650	
		0	10	–	–	–	–	–	135	270	
		0	15	–	–	–	–	–	95	190	
Address or Inhibit-to-Signal OUT (Channel turning OFF)	R_L=300 Ω,C_L=50 pF, t_r,t_f=20 ns										ns
		0	5	–	–	–	–	–	220	440	
		0	10	–	–	–	–	–	90	180	
		0	15	–	–	–	–	–	65	130	
Input Capacitance, C_{IN}	Any Address or Inhibit Input			–	–	–	–	–	5	7.5	pF

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F). . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

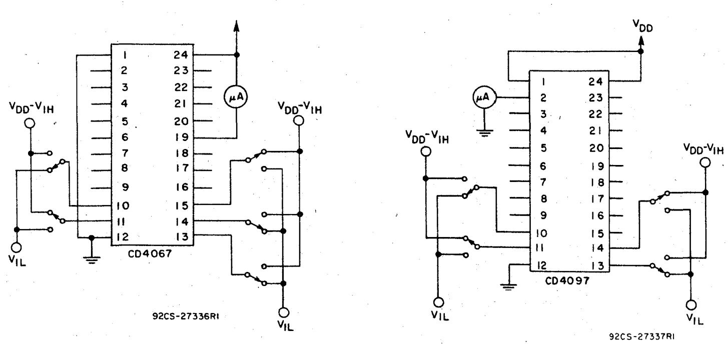


Fig. 8– Input voltage–measure <2 μA on all OFF channels (e.g., channel 12).

TEST CIRCUITS

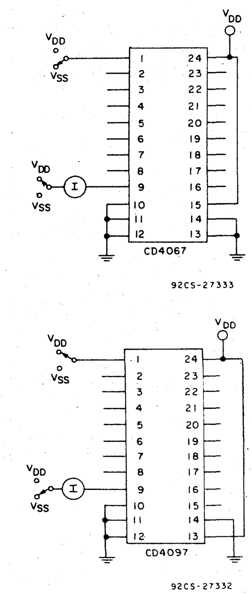


Fig. 7–OFF channel leakage current–any channel OFF.

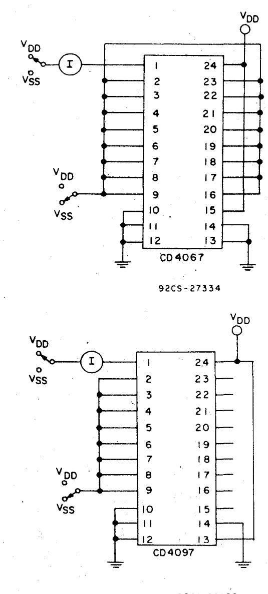


Fig. 9–OFF channel leakage current–all channels OFF.

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	V_{is} (V)	V_{DD} (V)	R_L (KΩ)	TEST CONDITIONS		TYPICAL VALUES	UNITS
Cutoff (−3-dB) Frequency Channel ON (Sine Wave Input)	5●	10	1	V_{os} at Common OUT/IN	CD4067	14	MHz
	$20 \log \frac{V_{os}}{V_{is}} = -3$ dB				CD4097	20	
				V_{os} at Any Channel		60	
Total Harmonic Distortion, THD	2●	5	10			0.3	%
	3●	10				0.2	
	5●	15				0.12	
	f_{is} = 1 kHz sine wave						
−40-dB Feedthrough Frequency (All Channels OFF	5●	10	1	V_{os} at Common OUT/IN	CD4067	20	MHz
	$20 \log \frac{V_{os}}{V_{is}} = -40$ dB				CD4097	12	
				V_{os} at Any Channel		8	
Signal Cross-talk (Frequency at −40 dB)	5●	10	1	Between Any 2 Channels▲		1	MHz
	$20 \log \frac{V_{os}}{V_{is}} = -40$ dB			Between Sections CD4097 Only	Measured on Common	10	
					Measured on Any Channel	18	
Address-or-Inhibit-to-Signal Crosstalk	–	10	10*			75	mV (Peak)
	V_{SS}=0, t_r,t_f=20 ns, $V_C=V_{DD}-V_{SS}$ (Square Wave)						

● Peak-to-peak voltage symmetrical about $\frac{V_{DD}-V_{SS}}{2}$.

▲ Worst case.

* Both ends of channel.

TEST CIRCUITS (Cont'd)

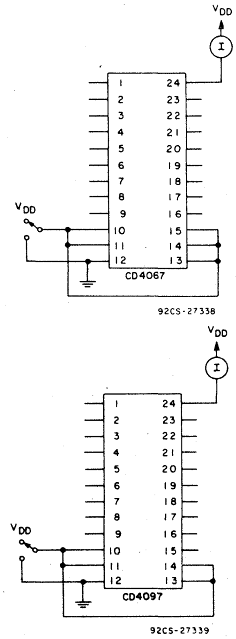


Fig. 10— Quiescent device current.

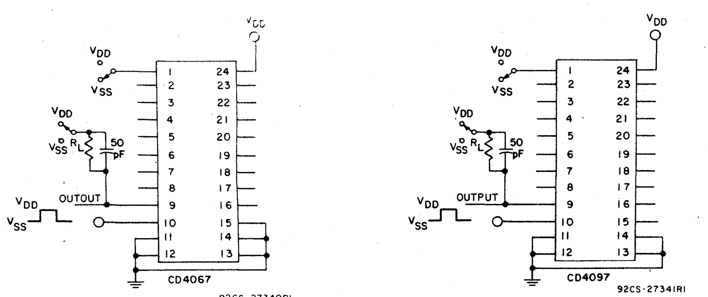


Fig. 11— Turn-on and turn-off propagation delay—address select input to signal output (e.g. measured on channel 0).

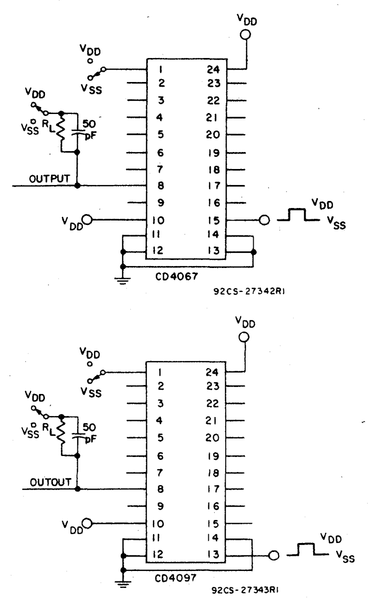


Fig. 12— Turn-on and turn-off propagation delay—inhibit input to signal output (e.g. measured on channel 1).

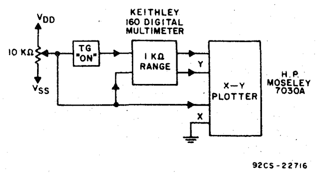


Fig. 13—Channel ON resistance measurement circuit.

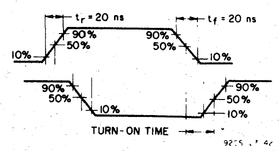


Fig. 14—Propagation delay waveform channel being turned ON (R_L=10 KΩ, C_L= 50 pF).

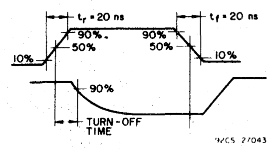


Fig. 15—Propagation delay waveform, channel being turned OFF (R_L = 300 Ω, C_L = 50 pF).

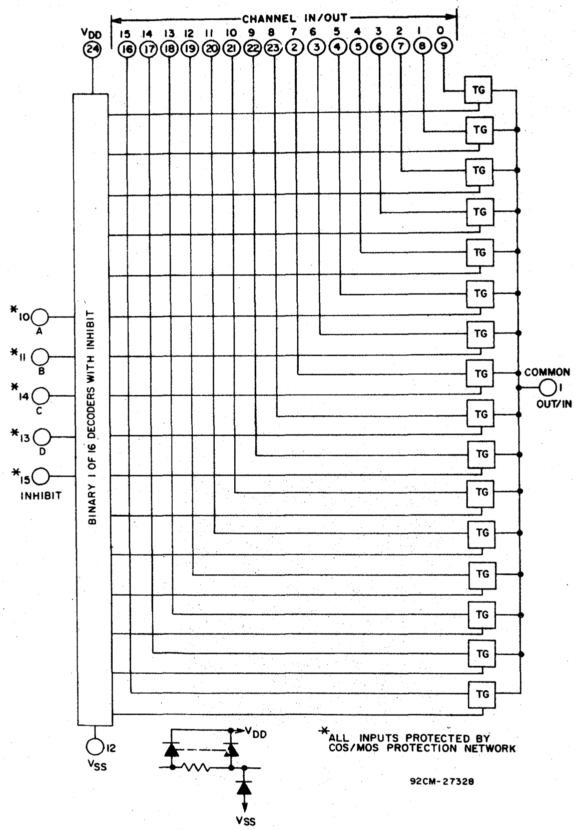


Fig. 16—CD4067 logic diagram.

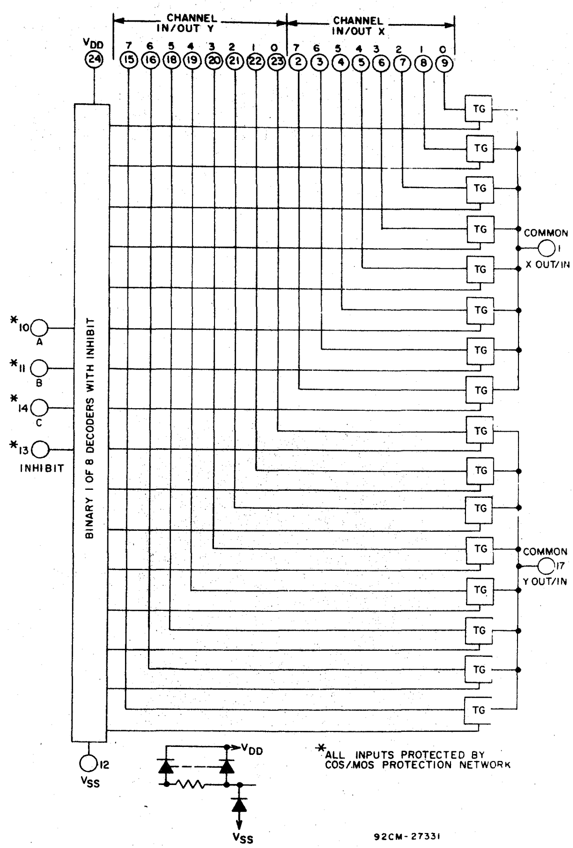


Fig. 17—CD4097 logic diagram.

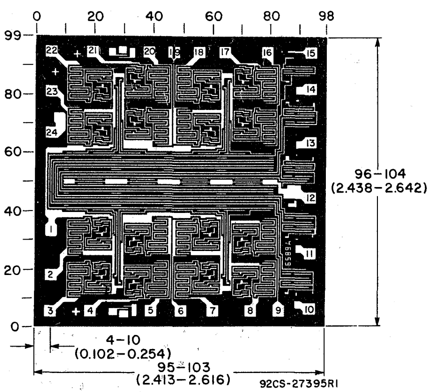
SPECIAL CONSIDERATIONS

In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L=effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4067B or CD4097B.

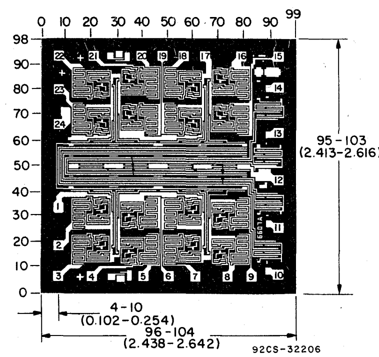
When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned on or off by an address input, there is a momentary conductive path from the channel to V_{SS}, which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning on a channel will similarly dump some charge to V_{SS}.

The amount of charge dumped is mostly a function of the signal level above V_{SS}. Typically, at $V_{DD}-V_{SS}$=10 V, a 100-pF capacitor connected to the input or output of the channel will lose 3-4% of its voltage at the moment the channel turns on or off. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1-2 μs. When the inhibit signal turns a channel off, there is no charge dumping to V_{SS}. Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 1 on the CD4067B, terminals 1 and 17 on the CD4097B.



Dimensions and pad layout for CD4067BH.



Dimensions and pad layout for CD4097BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

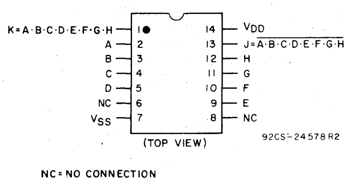
The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS 8-Input NAND/AND Gate

High-Voltage Types (20-Volt Rating)

The RCA-CD4068B NAND/AND gate provides the system designer with direct implementation of the positive-logic 8-input NAND and AND functions and supplements the existing family of COS/MOS gates.

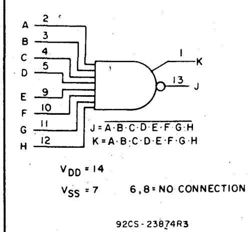
The CD4068B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).



TERMINAL ASSIGNMENT

Features:

- Medium-Speed Operation: t_{PHL}, t_{PLH} = 75 ns (typ.) at V_{DD} = 10 V
- Buffered inputs and outputs
- 5-V, 10-V, and 15-V parametric ratings
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	Min.	Max.	Units
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

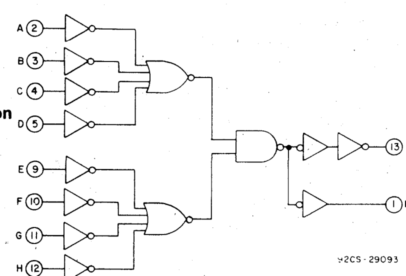


Fig. 1 — Logic diagram.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages; Values at −40, +25, +85 Apply to E Package: −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

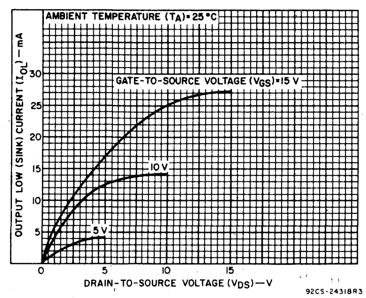


Fig. 2 — Typical output low (sink) current characteristics.

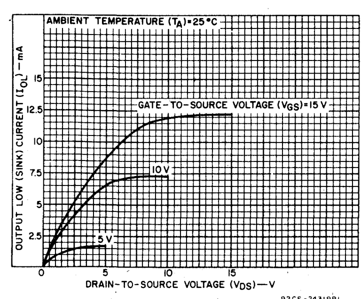


Fig. 3 — Minimum output low (sink) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,) . . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F,) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS
At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200kΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	150	300	ns
		10	75	150	
		15	55	110	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

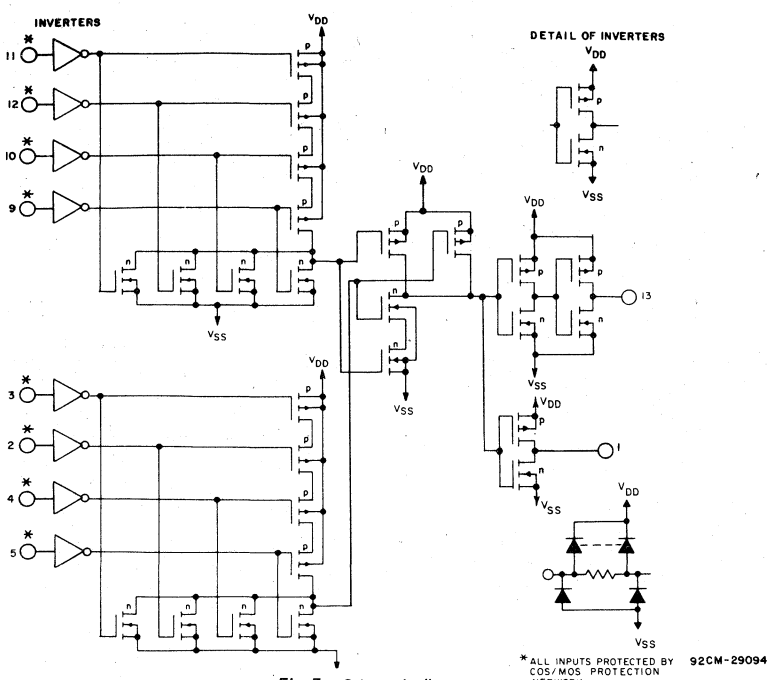


Fig. 7 – Schematic diagram.

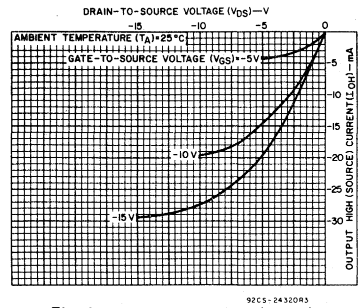


Fig. 4 – Typical output high (source) current characteristics.

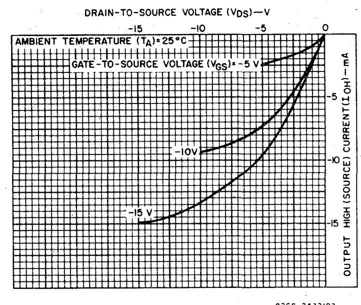


Fig. 5 – Minimum output high (source) current characteristics.

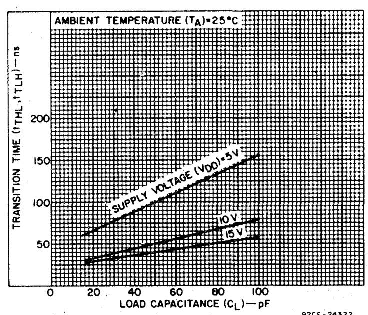


Fig. 6 – Typical transition time as a function of load capacitance.

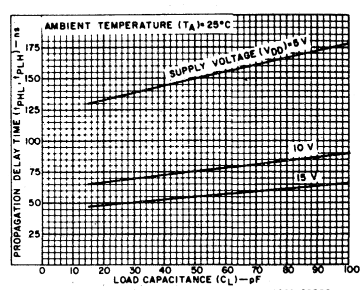


Fig. 8 – Typical propagation delay time as a function of load capacitance.

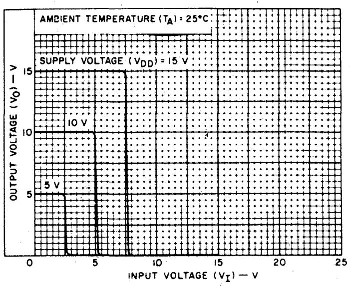


Fig. 9 – Typical voltage transfer characteristics (NAND output).

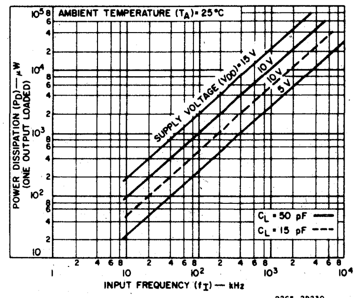


Fig. 10 – Typical dynamic power dissipation as a function of frequency.

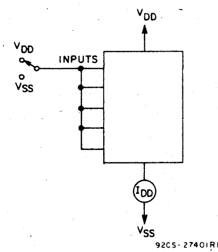


Fig. 11 – Quiescent-device-current test circuit.

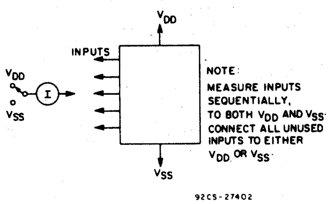


Fig. 12 – Input current test circuit.

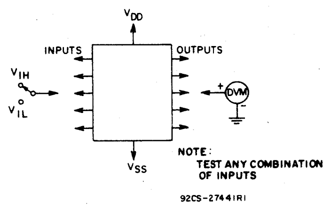


Fig. 13 – Input-voltage test circuit.

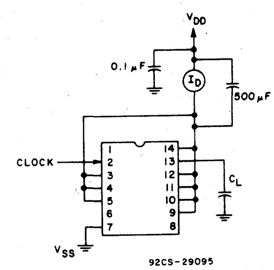
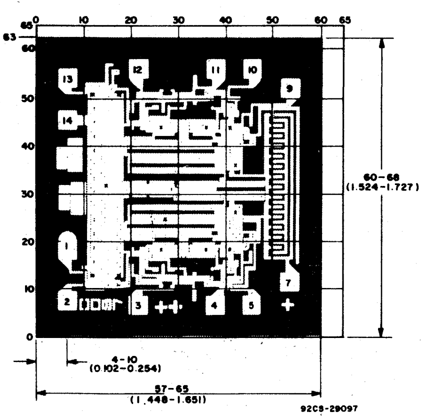


Fig. 14 – Dynamic power dissipation test circuit.



Dimensions and pad layout for CD4068BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4069UB Types

COS/MOS Hex Inverter

High-Voltage Types (20-Volt Rating)

The RCA-CD4069UB types consist of six COS/MOS inverter circuits. These devices are intended for all general-purpose inverter applications where the medium-power TTL-drive and logic-level-conversion capabilities of circuits such as the CD4009 and CD4049 Hex Inverter/Buffers are not required.

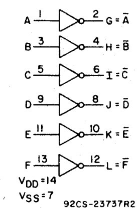
The CD4069UB-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **Standardized symmetrical output characteristics**
- **Medium Speed Operation—t_{PHL},t_{PLH}=30 ns (typ.) at 10 V**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Logic inversion**
- **Pulse shaping**
- **Oscillators**
- **High-input-impedance amplifiers**



CD4069UB FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A=Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		CONDITIONS V_{DD} V	ALL TYPES LIMITS Typ.	ALL TYPES LIMITS Max.	UNITS
Propagation Delay Time;	t_{PLH}, t_{PHL}	5	55	110	ns
		10	30	60	
		15	25	50	
Transition Time;	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance;	C_{IN}	Any Input	10	15	pF

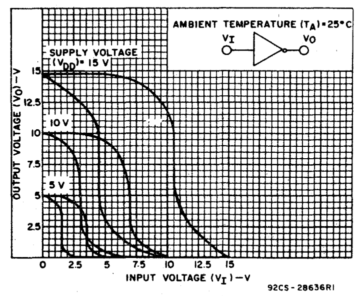


Fig. 1 — Minimum and maximum voltage transfer characteristics.

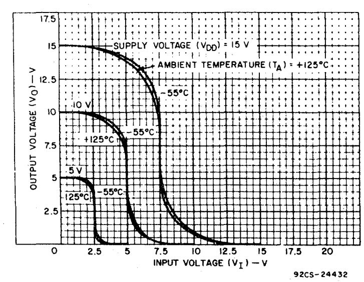


Fig. 2 — Typical voltage transfer characteristics as a function of temperature.

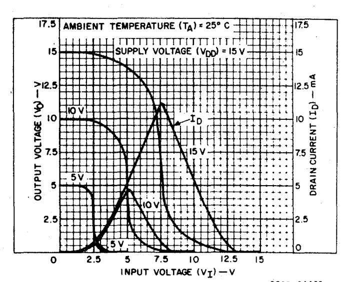


Fig. 3 — Typical current and voltage transfer characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER-ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	5	5	0.05				–	0	0.05	V
	–	10	10	0.05				–	0	0.05	
	–	15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0	5	4.95				4.95	5	–	
	–	0	10	9.95				9.95	10	–	
	–	0	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	4.5	–	5	1				—	—	1	V
	9	–	10	2				—	—	2	
	13.5	–	15	2.5				—	—	2.5	
Input High Voltage, V_{IH} Min.	0.5	–	5	4				4	—	—	
	1	–	10	8				8	—	—	
	1.5	–	15	12.5				12.5	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

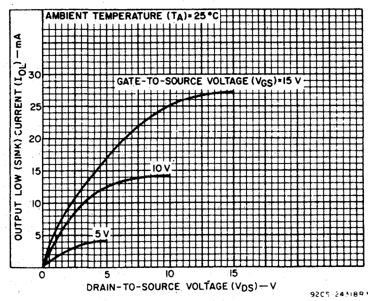


Fig. 4 – Typical output low (sink) current characteristics.

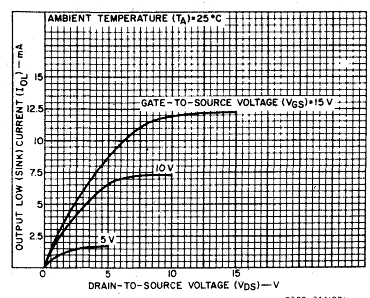


Fig. 5 – Minimum output low (sink) current characteristics.

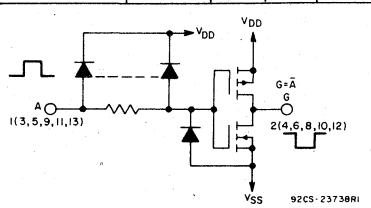


Fig. 6 – Schematic diagram of one of six identical inverters.

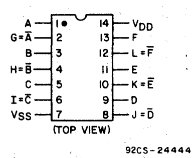


Fig. 7 – CD4069UB terminal assignment.

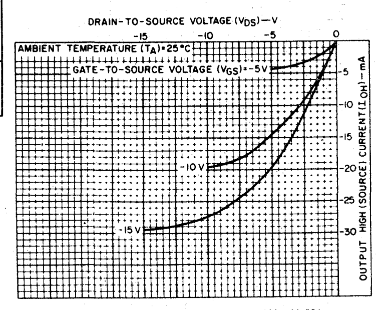


Fig. 8 – Typical output high (source) current characteristics.

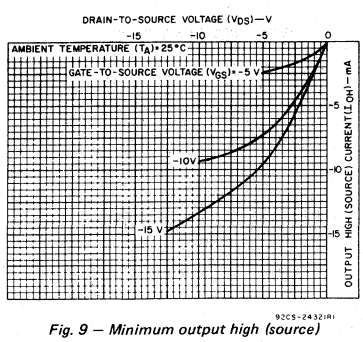


Fig. 9 – Minimum output high (source) current charactéristics.

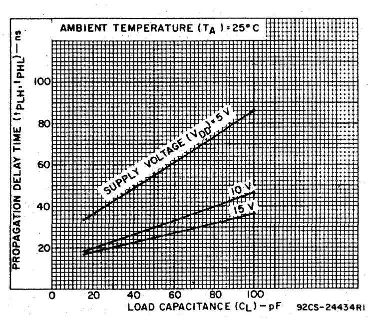


Fig. 10 – Typical propagation delay time vs. load capacitance.

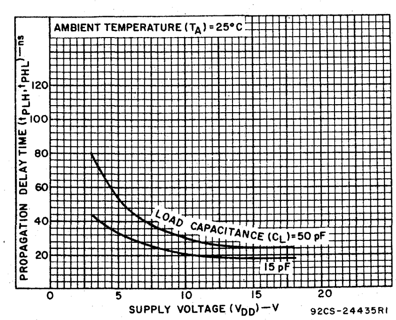


Fig. 11 – Typical propagation delay time vs. supply voltage.

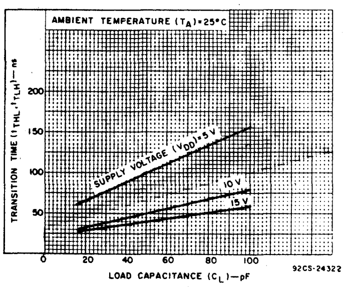


Fig. 12 – Typical transition time vs. load capacitance.

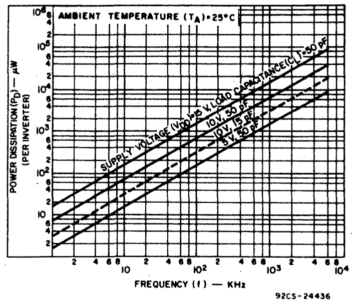


Fig. 13 – Typical dynamic power dissipation vs. frequency.

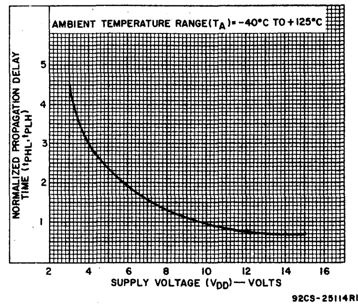


Fig. 14 – Variation of normalized propagation delay time (t_{PHL} and t_{PLH}) with supply voltage.

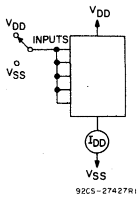


Fig. 15 – Quiescent device current test circuit.

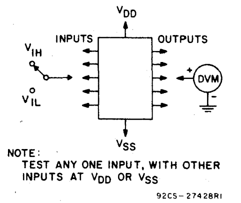


Fig. 16 – Noise immunity test circuit.

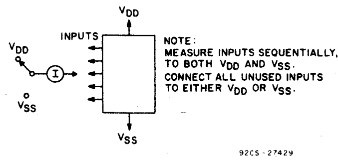


Fig. 17 – Input leakage current test circuit.

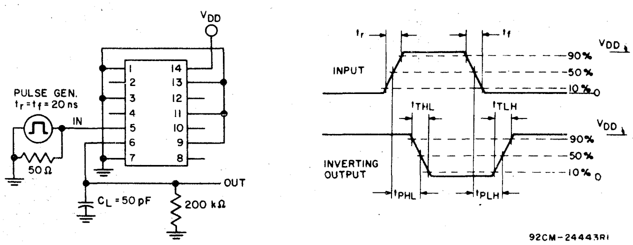


Fig. 18 – Dynamic electrical characteristics test circuit and waveforms.

APPLICATIONS

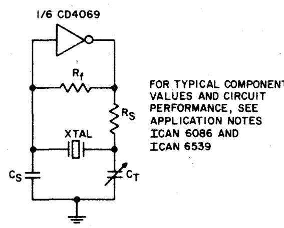


Fig. 19 – Typical crystal oscillator circuit.

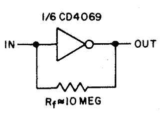


Fig. 20 – High-input impedance amplifier.

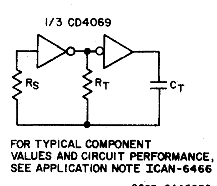


Fig. 21 – Typical RC oscillator circuit.

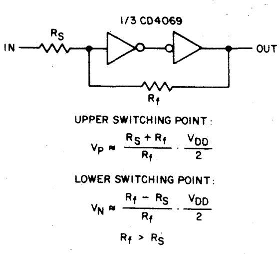
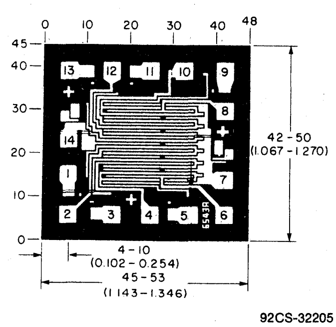


Fig. 22 – Input pulse shaping circuit (Schmitt trigger).

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



Dimensions and pad layout for CD4069UBH.

COS/MOS Quad Exclusive-OR and Exclusive-NOR Gates

High-Voltage Types (20-Volt Rating)

CD4070B – Quad Exclusive-OR Gate
CD4077B – Quad Exclusive-NOR Gate

The RCA-CD4070B contains four independent Exclusive-OR gates. The RCA-CD4077B contains four independent Exclusive-NOR gates.

The CD4070B and CD4077B provide the system designer with a means for direct implementation of the Exclusive-OR and Exclusive-NOR functions, respectively.

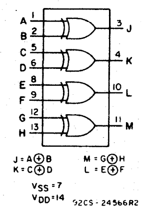
The CD4070B and CD4077B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

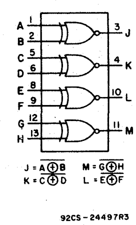
- Medium-speed operation—t_{PHL}, t_{PLH} = 65 ns (typ.) at V_{DD} = 10 V, C_L = 50 pF
- 100% tested for quiescent current at 20 V
- Standardized symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Logical comparators
- Adders/subtractors
- Parity generators and checkers



CD4070B FUNCTIONAL DIAGRAM



CD4077B Functional Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	–0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	–55 to +125°C
PACKAGE TYPE E	–40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	–65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

Characteristic	Min.	Max.	Units
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

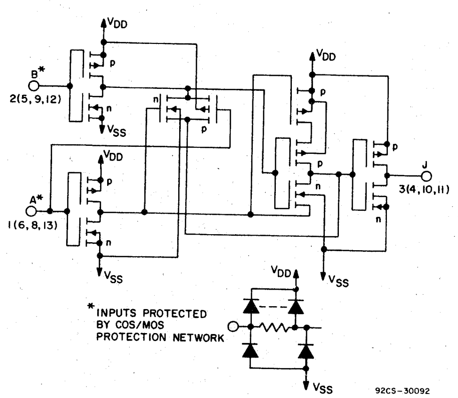
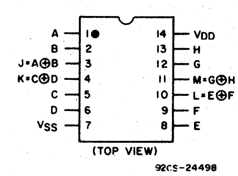


Fig. 1 – Schematic diagram for CD4070B (1 of 4 identical gates).

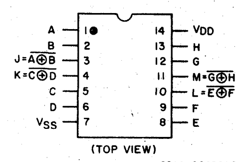
TRUTH TABLE CD4070B
1 of 4 Gates

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

1 = HIGH LEVEL
0 = LOW LEVEL
J = A ⊕ B



TERMINAL ASSIGNMENT CD4070B



TERMINAL ASSIGNMENT CD4077B

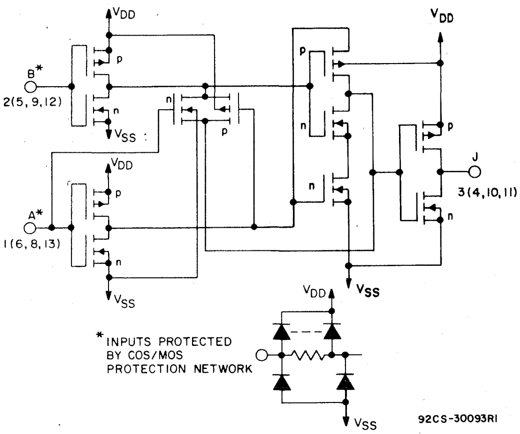


Fig. 2 – Schematic diagram for CD4077B (1 of 4 identical gates).

TRUTH TABLE CD4077B
1 of 4 Gates

A	B	J
0	0	1
1	0	0
0	1	0
1	1	1

1 = HIGH LEVEL
0 = LOW LEVEL
$J = \overline{A \oplus B}$

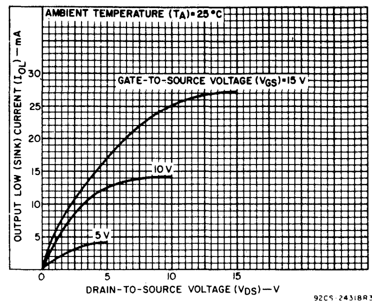


Fig. 3 – Typical output low (sink) current characteristics.

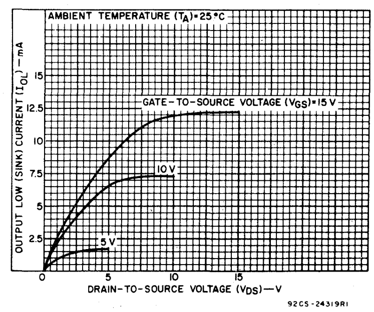


Fig. 4 – Minimum output low (sink) current characteristics.

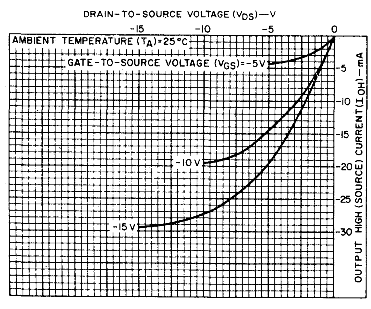


Fig. 5 – Typical output high (source) current characteristics.

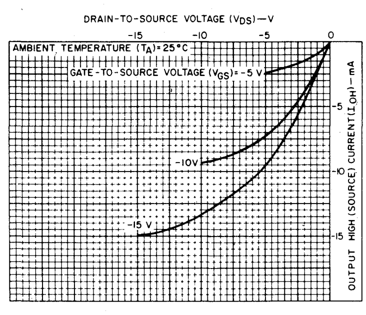


Fig. 6 – Minimum output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55,+25,+125 Apply to D,F,H Pkgs. Values at –40,+25,+85 Apply to E Pkgs.							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	µA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	µA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		CONDITIONS V_{DD} V	ALL TYPES LIMITS		UNITS
			Typ.	Max.	
Propagation Delay Time;	t_{PHL}, t_{PLH}	5	140	280	ns
		10	65	130	
		15	50	100	
Transition Time;	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance;	C_{IN}	Any Input	5	7.5	pF

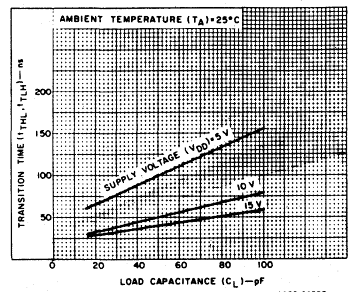


Fig. 7 – Typical transition time as a function of load capacitance.

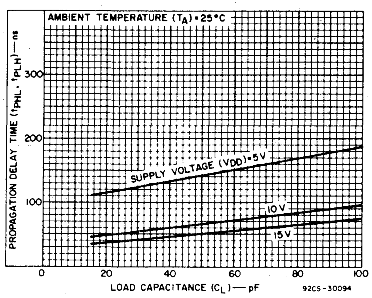


Fig. 8 – Typical propagation delay time as a function of load capacitance.

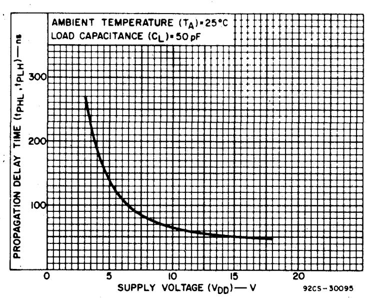


Fig. 9 – Typical propagation delay time as a function of supply voltage.

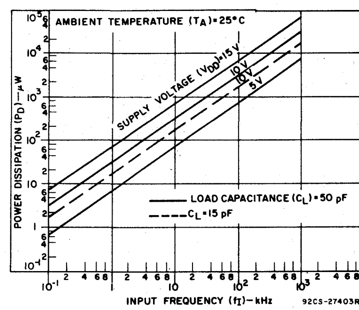
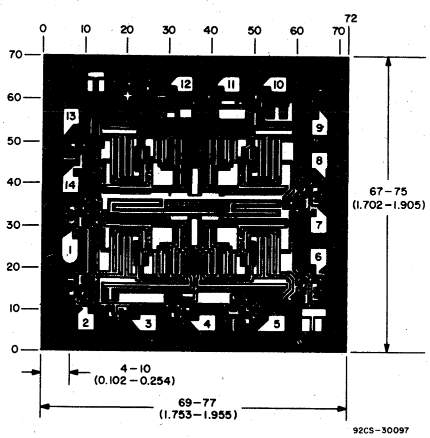


Fig. 10 – Typical dynamic power dissipation as a function of input frequency.



Dimensions and pad layout for CD4070BH. Dimensions and pad layout for CD4077BH are identical.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

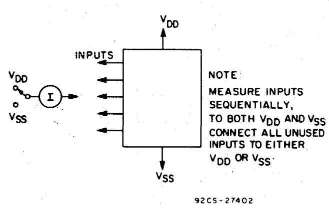


Fig. 11 –Input current test circuit.

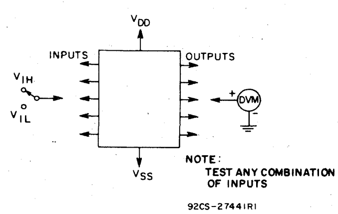


Fig. 12 – Input-voltage test circuit.

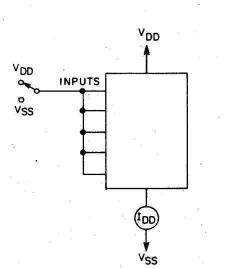


Fig. 13 – Quiescent-device-current test circuit.

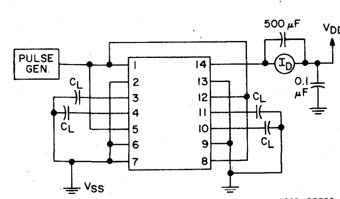


Fig. 14 – Dynamic power dissipation test circuit.

CD4071B, CD4072B, CD4075B Types

COS/MOS OR Gates

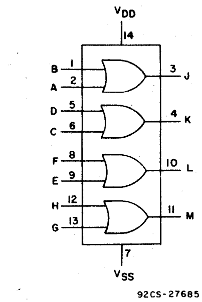
High-Voltage Types (20-Volt Rating)

CD4071B Quad 2-Input OR Gate
CD4072B Dual 4-Input OR Gate
CD4075B Triple 3-Input OR Gate

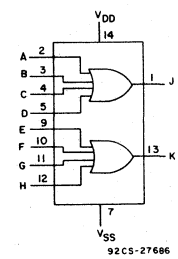
The RCA-CD4071B, CD4072B, and CD4075B OR gates provide the system designer with direct implementation of the positive-logic OR function and supplement the existing family of COS/MOS gates. The CD4071, CD4072, and CD4075 types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

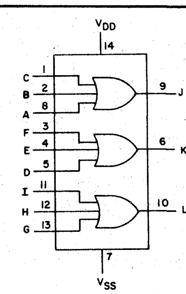
- **Medium-Speed Operation-t_{PLH}, t_{PHL} = 60 ns (typ.) at V_{DD} = 10 V**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Standardized, symmetrical output characteristics**
- **Noise margin (over full package temperature range)**
  - **1 V at V_{DD} = 5 V**
  - **2 V at V_{DD} = 10 V**
  - **2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13 A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



CD4071B
FUNCTIONAL DIAGRAM



CD4072B
FUNCTIONAL DIAGRAM



CD4075B
FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	4.5	–	5	3.5				3.5	–	–	
	9	–	10	7				7	–	–	
	13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

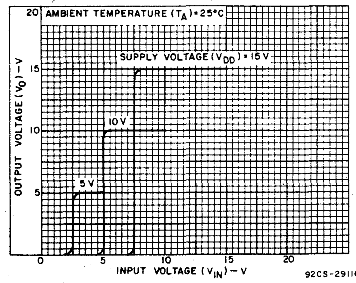


Fig. 1 — Typical voltage transfer characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, and C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5 10 15	125 60 45	250 120 90	ns
Transition Time, t_{THL}, t_{TLH}		5 10 15	100 50 40	200 100 80	ns
Input Capacitance, C_{IN}	Any Input	—	5	7.5	pF

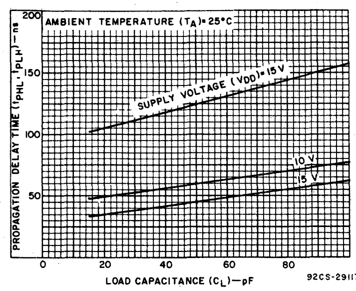


Fig. 2 — Typical propagation delay time as a function of load capacitance.

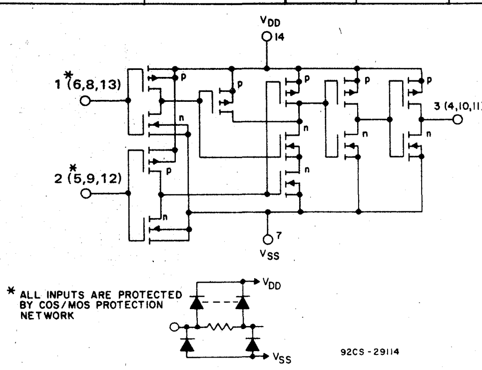


Fig. 3 — Schematic diagram for CD4071B (1 of 4 identical gates).

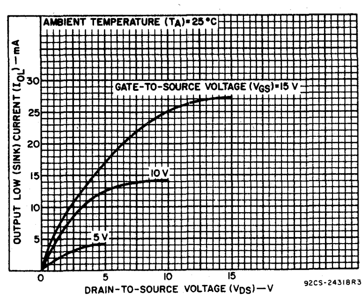


Fig. 4 — Typical output low (sink) current characteristics.

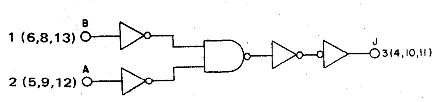


Fig. 5 — Logic diagram for CD4071B (1 of 4 identical gates).

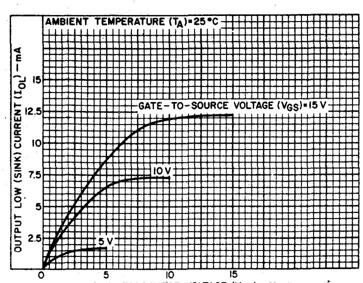
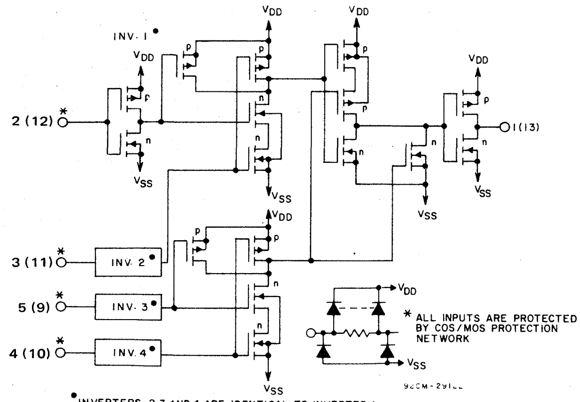


Fig. 6 — Minimum output low (sink) current characteristics.



•INVERTERS 2,3 AND 4 ARE IDENTICAL TO INVERTER 1.

Fig. 7 – Schematic diagram for CD4072B (1 of 2 identical gates).

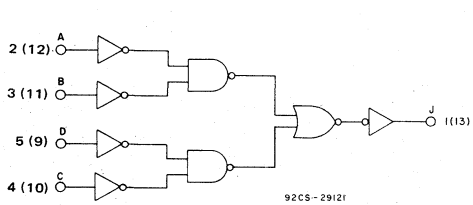


Fig. 9 – Logic diagram for CD4072B (1 of 2 identical gates).

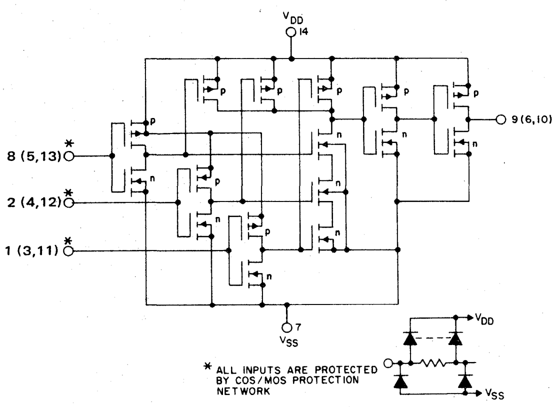


Fig. 11 – Schematic diagram for CD4075B (1 of 3 identical gates).

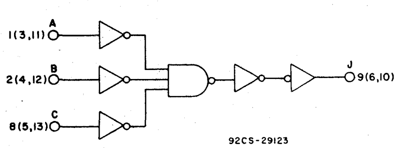


Fig. 13 – Logic diagram for CD4075B (1 of 3 identical gates).

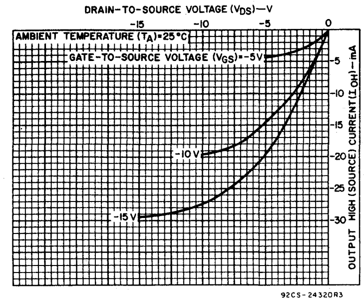


Fig. 8 – Typical output high (source) current characteristics.

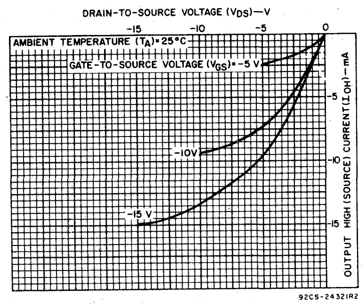


Fig. 10 – Minimum output high (source) current characteristics.

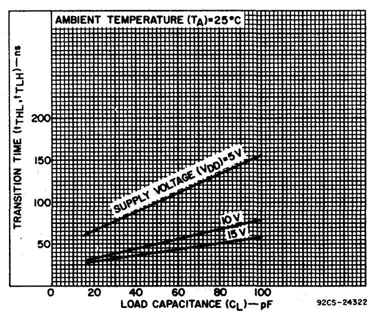


Fig. 12 – Typical transition time as a function of load capacitance.

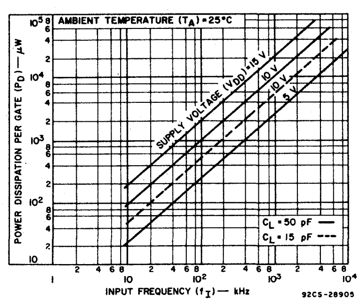
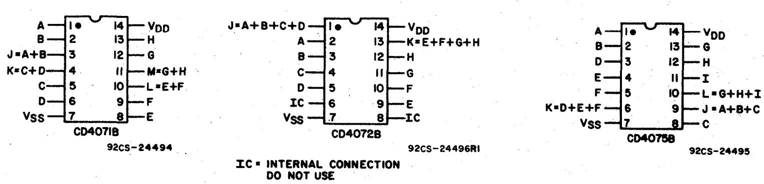


Fig. 14 – Typical dyanamic power dissipation as a function of frequency.

TERMINAL ASSIGNMENTS (TOP VIEW)



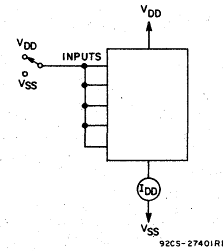


Fig. 15 – Quiescent device current test circuit.

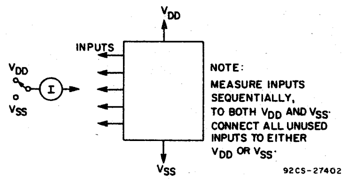


Fig. 16 – Input current test circuit.

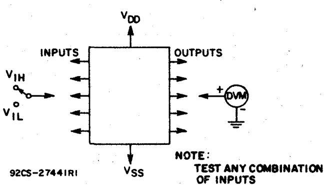
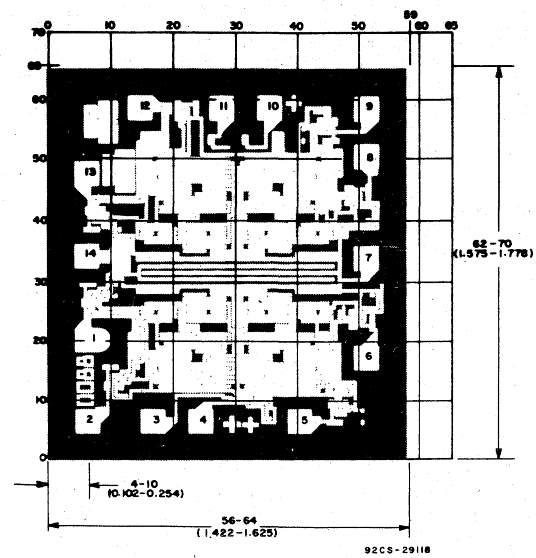


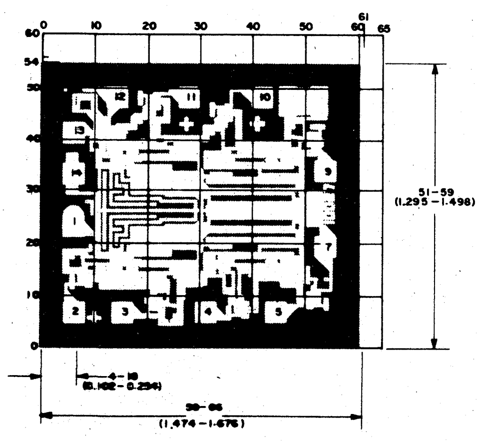
Fig. 17 – Input-voltage test circuit.



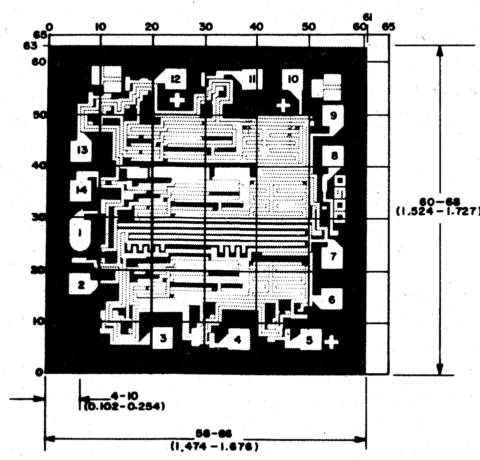
Dimensions and pad layout for CD4071B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



Dimensions and pad layout for CD4072B.



Dimensions and pad layout for CD4075B.

CD4073B, CD4081B, CD4082B Types

COS/MOS AND Gates

High-Voltage Types (20-Volt Rating)

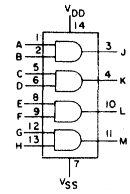
CD4073B Triple 3-Input AND Gate
CD4081B Quad 2-Input AND Gate
CD4082B Dual 4-Input AND Gate

The RCA-CD4073B, CD4081B and CD-4082B AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of COS/MOS gates.

The CD4073B, CD4081B and CD4082B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Medium-Speed Operation – t_{PLH}, t_{PHL} = 60 ns (typ.) at V_{DD} = 10 V**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) =**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

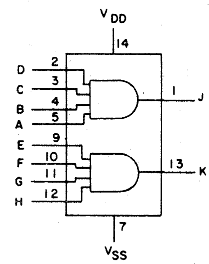


92CS-27583

CD4081B FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . –55 to +125°C
PACKAGE TYPE E . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C



92CS-27570

CD4082B FUNCTIONAL DIAGRAM

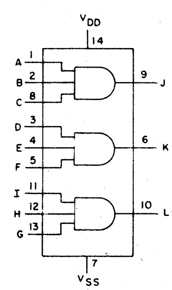
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, Input t_r,t_f=20 ns, and C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} Volts	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input	–	5	7.5	pF



92CS-27571

CD4073B FUNCTIONAL DIAGRAM

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages Values at –40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5	–	5	1.5				–	–	1.5	V
	1	–	10	3				–	–	3	
	1.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

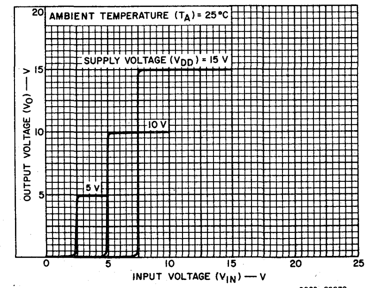


Fig. 3 — Typical voltage transfer characteristics.

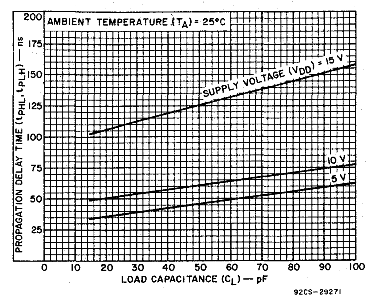


Fig. 4 — Typical propagation delay time as a function of load capacitance.

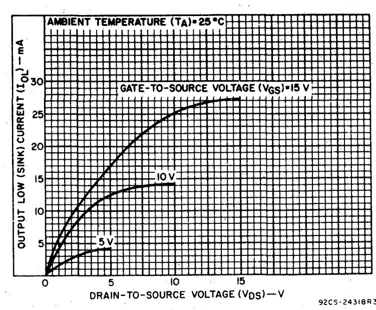


Fig. 5 — Typical output low (sink) current characteristics.

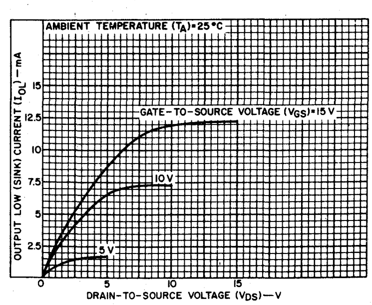


Fig. 6 — Minimum output low (sink) current characteristics.

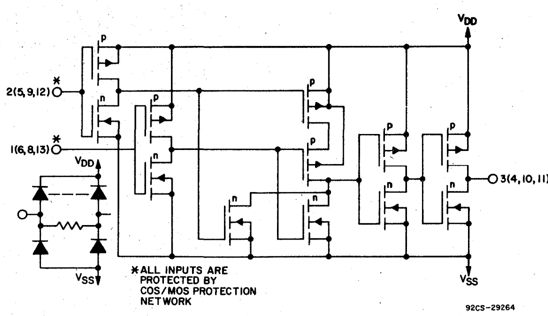


Fig. 1 — Schematic diagram for CD4081B (1 of 4 identical gates).

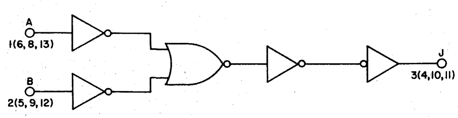


Fig. 2 — Logic diagram for CD4081B (1 of 4 identical gates).

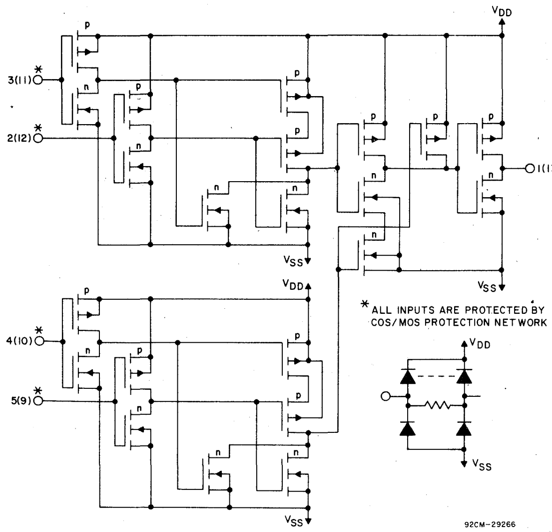


Fig. 7 — Schematic diagram for CD4082B (1 of 2 identical gates).

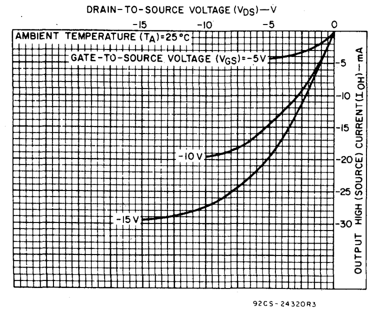


Fig. 8 — Typical output high (source) current characteristics.

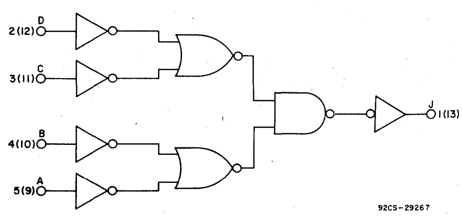


Fig. 9 — Logic diagram for CD4082B (1 of 2 identical gates).

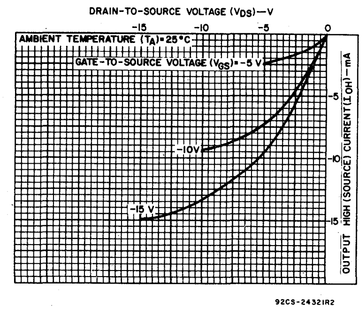


Fig. 10 — Minimum output high (source) current characteristics.

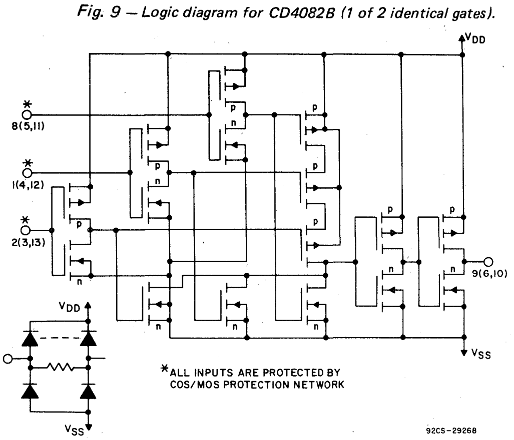


Fig. 11 — Schematic diagram for CD4073B (1 of 3 identical gates).

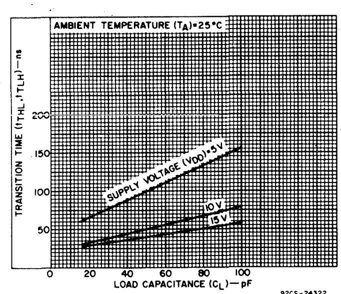


Fig. 12 — Typical transition time as a function of load capacitance.

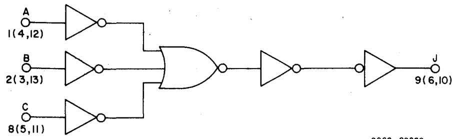


Fig. 13 — Logic diagram for CD4073B (1 of 3 identical gates).

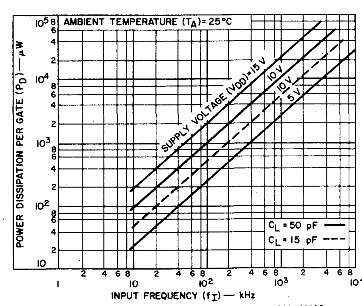


Fig. 14 — Typical dynamic power dissipation per gate as a function of frequency.

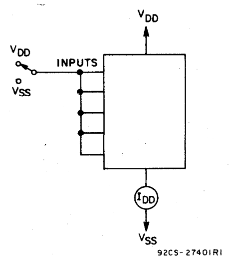


Fig. 15 — Quiescent device current test circuit.

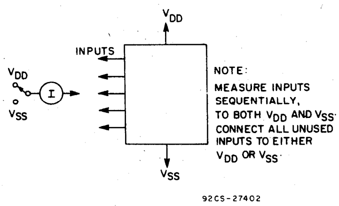


Fig. 16 — Input current test circuit.

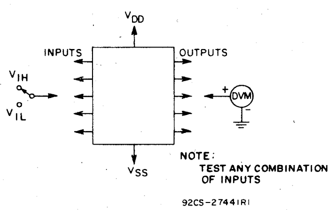
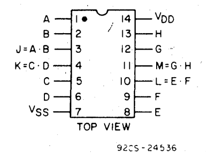
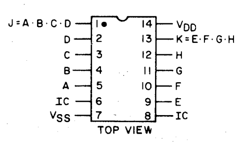


Fig. 17 — Input-voltage test circuit.

TERMINAL ASSIGNMENTS

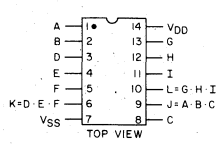


CD4081B

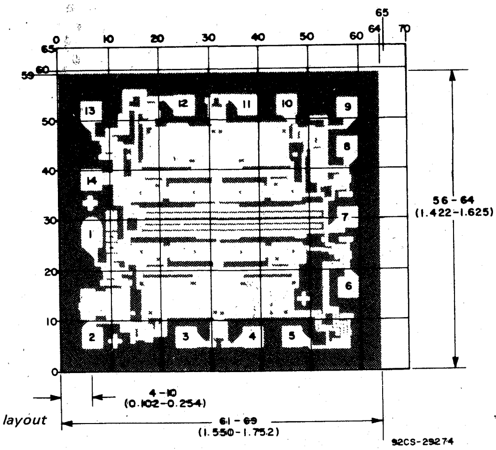


CD4082B

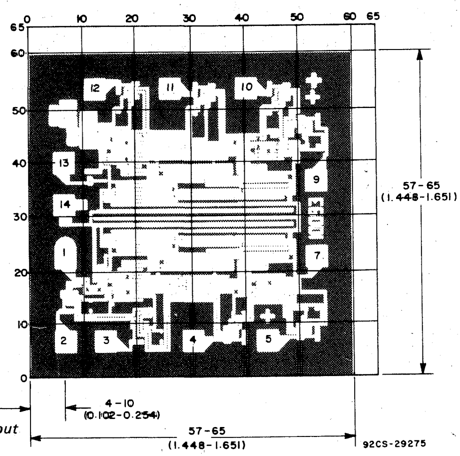
IC= INTERNAL CONNECTION- DO NOT USE



CD4073B



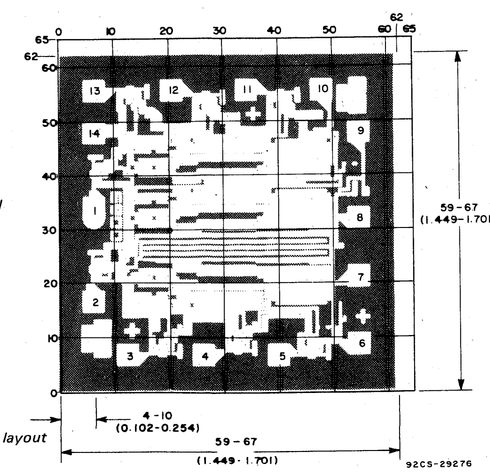
Dimensions and pad layout for CD4081B.



Dimensions and pad layout for CD4082B.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).



Dimensions and pad layout for CD4073B.

CD4076B Types

COS/MOS 4-Bit D-Type Registers

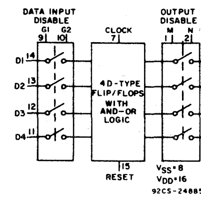
High-Voltage Types (20-Volt Rating)

The CD4076B types are four-bit registers consisting of D-type flip-flops that feature three-state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output Disable inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled independently of the clock by a high logic level at either Output Disable input, and present a high impedance.

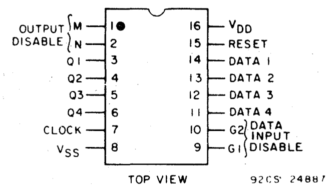
The CD4076B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Three-state outputs**
- **Input disabled without gating the clock**
- **Gated output control lines for enabling or disabling the outputs**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **Noise margin over full package temperature range:**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM



TERMINAL ASSIGNMENT

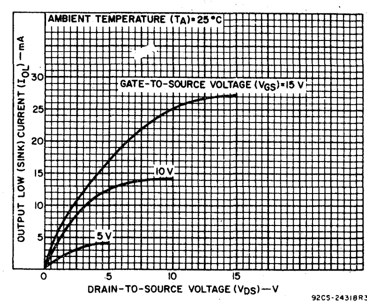


Fig.1 — Typical output low (sink) current characteristics.

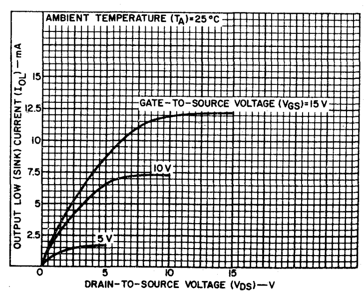


Fig.2 — Minimum output low (sink) current characteristics.

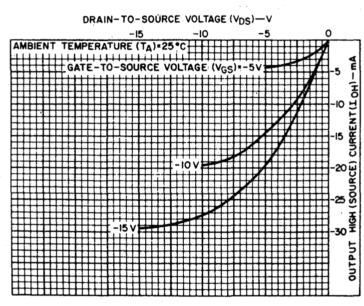


Fig.3 — Typical output high (source) current characteristics.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5	200	–	ns
	10	80	–	
	15	60	–	
Clock Pulse Width, t_W	5	200	–	ns
	10	100	–	
	15	80	–	
Clock Input Frequency, f_{CL}	5	dc	3	MHz
	10		6	
	15		8	
Clock Input Rise or Fall Time, t_rCL, t_fCL	5	–	15	μs
	10	–	5	
	15	–	5	
Reset Pulse Width, t_W	5	120	–	ns
	10	50	–	
	15	40	–	
Data Input Disable Setup Time, t_S	5	180	–	ns
	10	100	–	
	15	70	–	

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . . +265°C

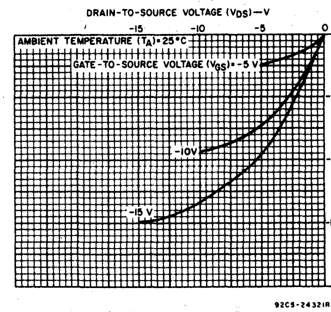
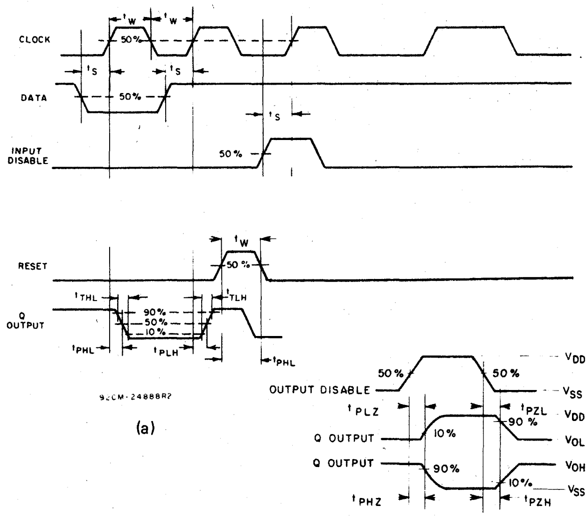


Fig.4 — Minimum output high (source) current characteristics.



CHAR.	TEST AT D	VOLT. AT Q
t_{PHZ}	V_{DD}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}
t_{PZL}	V_{SS}	V_{DD}
t_{PZH}	V_{DD}	V_{SS}

92CS-29299

(b)

Fig.5 — Functional waveforms for CD4076B.

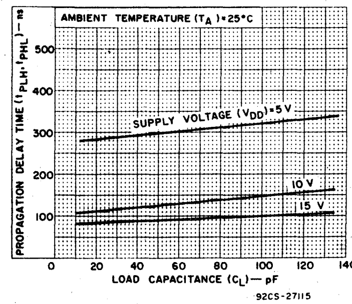


Fig.6 — Typical propagation delay time vs. load capacitance (clock to Q).

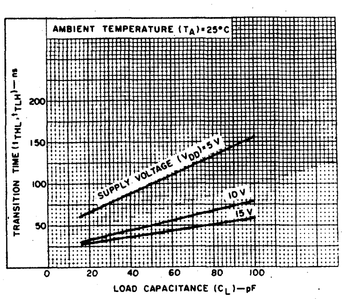


Fig.7 — Typical transition time vs. load capacitance.

Truth Table

Reset	Clock	Data Input Disable G1	Data Input Disable G2	Data D	Next State Output Q	
1	X	X	X	X	0	
0	0	X	X	X	Q	NC
0	↑	1	X	X	Q	NC
0	↑	X	1	X	Q	NC
0	↑	0	0	1	1	
0	↑	0	0	0	0	
0	1	X	X	X	Q	NC
0	↓	X	X	X	Q	NC

When either Output Disable M or N is high, the outputs are disabled (high impedance state), however sequential operation of the flip-flops is not affected.

1 ≡ High Level X = Don't Care
0 ≡ Low Level NC = No Change

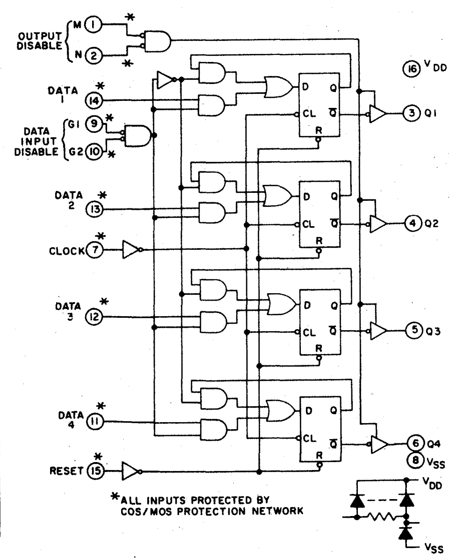


Fig.8 — CD4076B logic diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ (Unless otherwise noted)

CHARACTERISTIC	TEST CONDITIONS	V_{DD} V	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time: Clock to Q Output, t_{PHL}, t_{PLH}		5	–	300	600	ns
		10		125	250	
		15		90	180	
Reset, t_{PHL}		5		230	460	
		10		100	200	
		15	–	75	150	
3-State Output 1 or 0 to High Impedance, t_{PHZ}, t_{PLZ}	R_L = 1 kΩ	5		150	300	
		10	–	75	150	
		15		60	120	
3-State High Impedance to 1 or 0 Output, t_{PZH}, t_{PZL}	R_L = 1 kΩ	5		150	300	
		10		75	150	
		15		60	120	
Transition Time, t_{THL}, t_{TLH}		5		100	200	ns
		10		50	100	
		15	–	40	80	
Maximum Clock Input Frequency, f_{CL}		5	3	6	–	MHz
		10	6	12	–	
		15	8	16	–	
Minimum Clock Pulse Width, t_W		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Maximum Clock Input Rise or Fall Time, t_{rcl}, t_{fcl}		5	15	–	–	μs
		10	5	–	–	
		15	5	–	–	
Minimum Reset Pulse With, t_W		5	–	60	120	ns
		10	–	25	50	
		15	–	20	40	
Minimum Data Setup Time, t_S		5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
Minimum Data Input Disable Setup Time, t_S		5	–	90	180	ns
		10	–	50	100	
		15	–	35	70	
Input Capacitance, C_{IN}	Any Input	–	–	5	7.5	pF

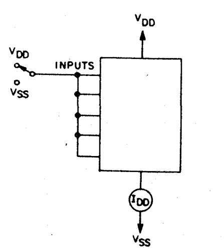


Fig. 11 – Quiescent device current test circuit.

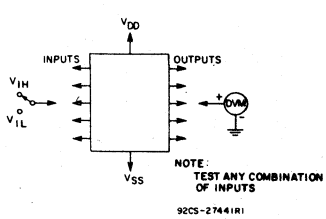


Fig. 12 – Input voltage test circuit.

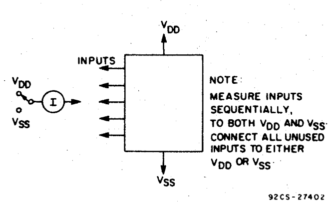


Fig. 13 – Input current test circuit.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm10^{-4}$	±0.4	μA

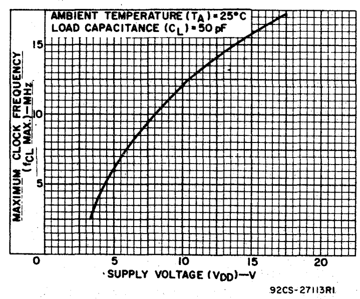


Fig.9 – Typical maximum clock input frequency vs. supply voltage.

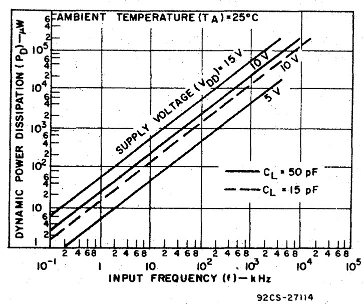
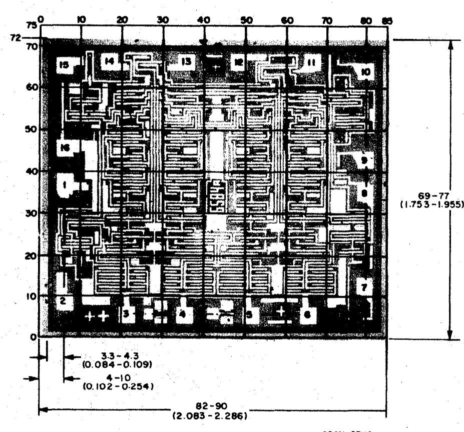


Fig.10 – Typical dynamic power dissipation vs. frequency.



Dimensions and pad layout for CD4076BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS 8-Input NOR/OR Gate

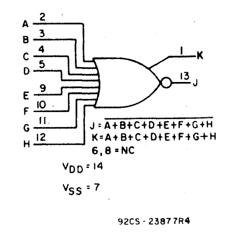
High-Voltage Types (20-Volt Rating)

The RCA-CD4078B NOR/OR Gate provides the system designer with direct implementation of the positive-logic 8-input NOR and OR functions and supplements the existing family of COS/MOS gates.

The CD4078B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Medium-Speed Operation:** t_{PHL}, t_{PLH} = 75 ns (typ.) at V_{DD} = 10 V
- **Buffered inputs and output**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range: 100 nA at 18 V and 25°C**
- **Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD} = 15 V**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

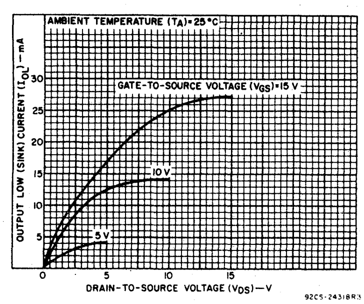


Fig. 2 — Typical output low (sink) current characteristics.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	Min.	Max.	Units
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

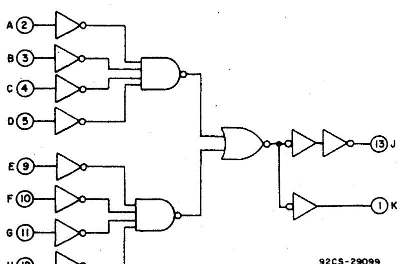


Fig. 1 — Logic diagram.

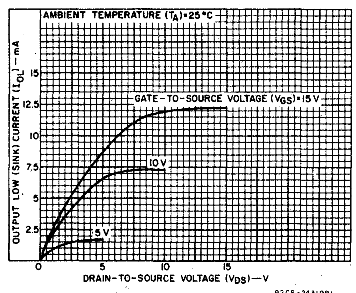


Fig. 3 — Minimum output low (sink) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200kΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5 10 15	150 75 55	300 150 110	ns
Transition Time, t_{THL}, t_{TLH}		5 10 15	100 50 40	200 100 80	ns
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

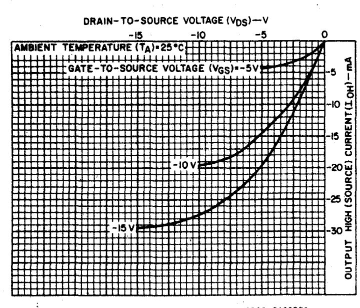


Fig. 4 — Typical output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages; Values at −40, +25, +85 Apply to E Package −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	µA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1		mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6		
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8		
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1		
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2		
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6		
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8		
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05					0	0.05	V
	–	0,10	10	0.05					0	0.05	
	–	0,15	15	0.05					0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5		
	–	0,10	10	9.95				9.95	10		
	–	0,15	15	14.95				14.95	15		
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	µA

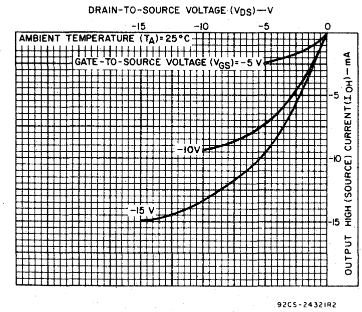


Fig. 5 — Minimum output high (source) current characteristics.

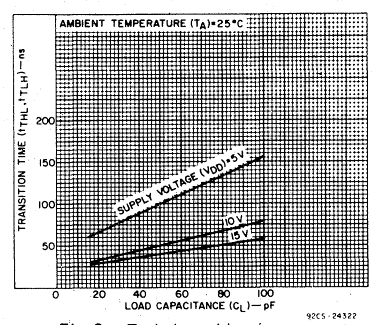


Fig. 6 — Typical transition time as a function of load capacitance.

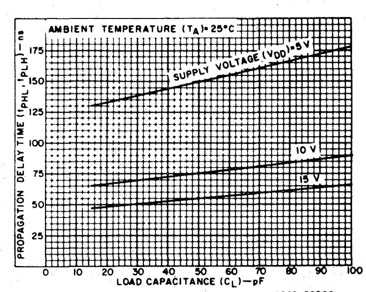


Fig. 7 — Typical propagation delay time as a function of load capacitance.

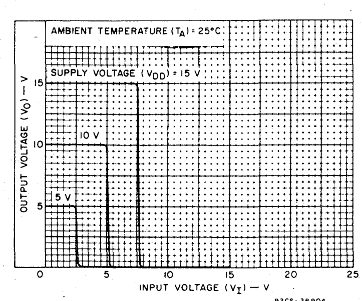


Fig. 9 — Typical voltage transfer characteristics (NOR output).

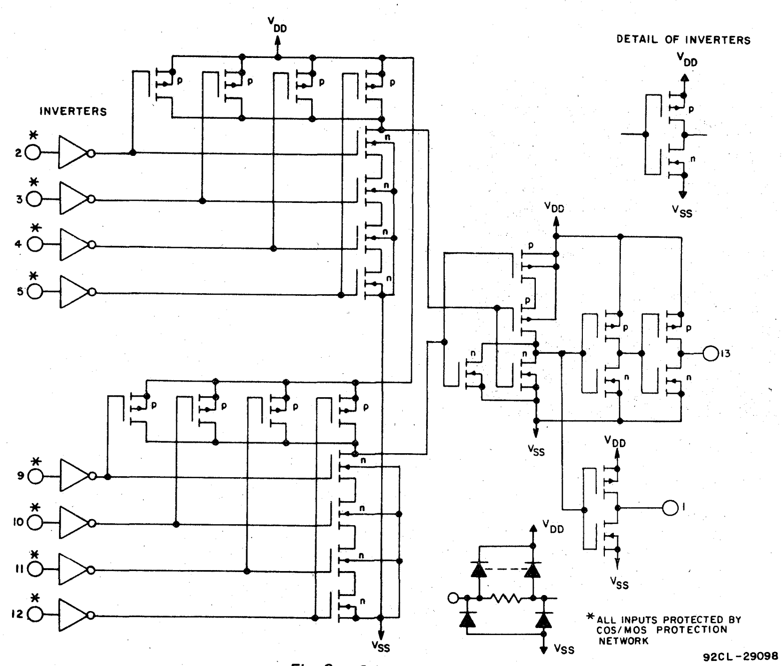


Fig. 8 — Schematic diagram.

CD4078B Types

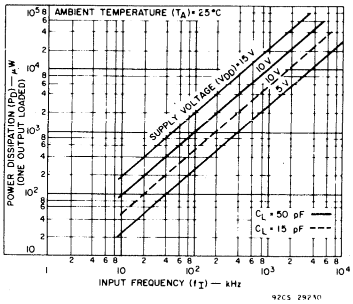


Fig. 10 — Typical dynamic power dissipation as a function of frequency.

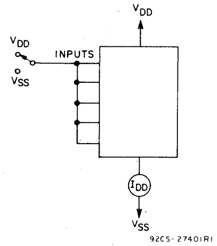


Fig. 11 — Quiescent-device-current test circuit.

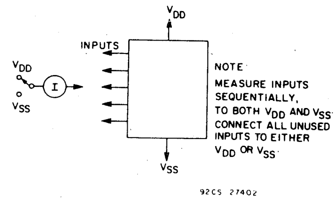


Fig. 12 — Input current test circuit.

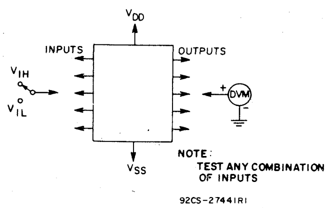


Fig. 13 — Input-voltage test circuit.

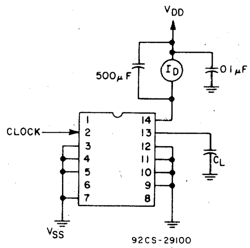
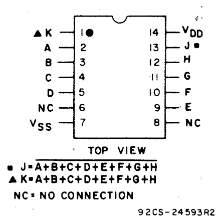
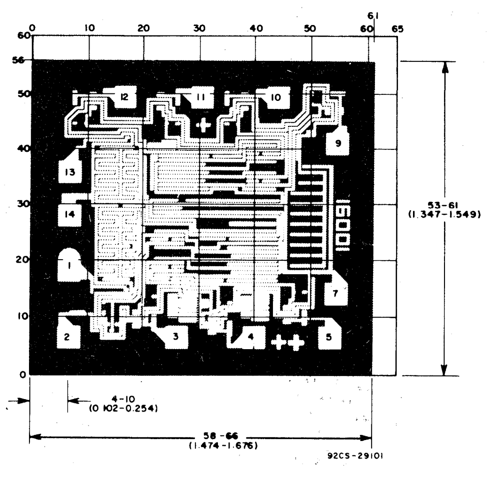


Fig. 14 — Dynamic power dissipation test circuit.



TERMINAL ASSIGNMENT



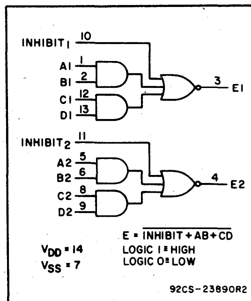
Dimensions and pad layout for CD4078BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of e.. .i COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Dual 2-Wide 2-Input AND-OR-INVERT Gate

High-Voltage Types (20-Volt Rating)



FUNCTIONAL DIAGRAM

The RCA-CD4085 contains a pair of AND-OR-INVERT gates, each consisting of two 2-input AND gates driving a 3-input NOR gate. Individual inhibit controls are provided for both A-O-I gates.

The CD4085B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Medium-speed operation – t_{PHL} = 90 ns; t_{PLH} = 125 ns (typ.) at 10 V**
- **Individual inhibit controls**
- **Standardized symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package-temperature range):**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

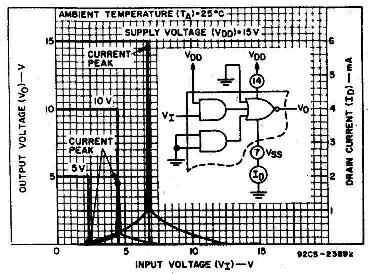


Fig. 1 – Typical voltage and current transfer characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . –55 to +125°C
PACKAGE TYPE E . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

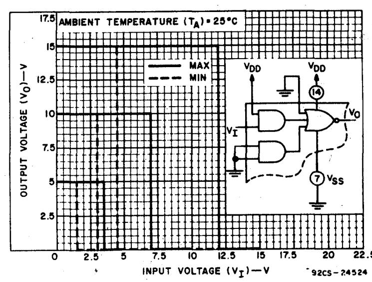
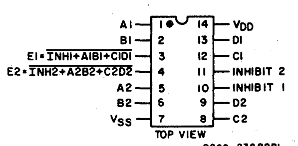


Fig. 2 – Min. and max. voltage transfer characteristics.

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V



Terminal Assignment

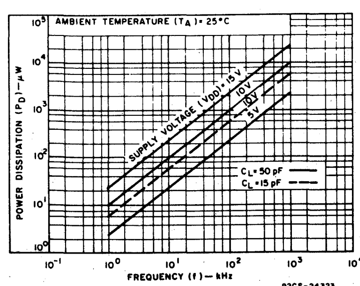


Fig. 3 – Typical power dissipation vs. frequency.

CD4085B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55,+25,+125 Apply to D,F,H Pkgs. Values at −40,+25,+85 Apply to E Pkgs. −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

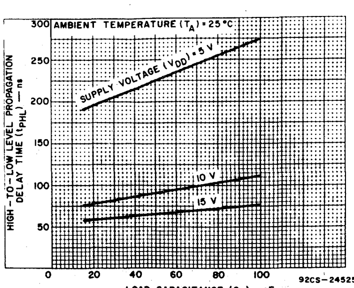


Fig. 4 – Typical data high-to-low level propagation delay time vs. load capacitance.

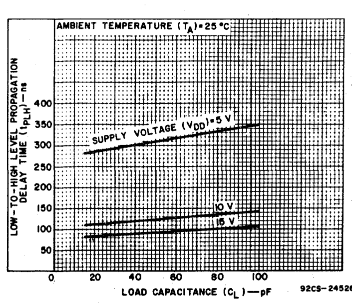


Fig. 5 – Typical data low-to-high level propagation delay time vs. load capacitance.

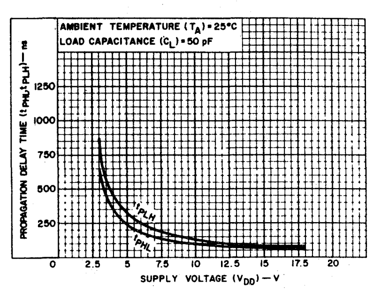


Fig. 6 – Typical data propagation delay time vs. supply voltage.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		CONDITIONS V_{DD} V	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time (Data): High-to-Low Level,	t_{PHL}	5	225	450	ns
		10	90	180	
		15	65	130	
Low-to-High Level,	t_{PLH}	5	310	620	ns
		10	125	250	
		15	90	180	
Propagation Delay Time (Inhibit): High-to-Low Level,	t_{PHL}	5	150	300	ns
		10	60	120	
		15	40	80	
Low-to-High Level,	t_{PLH}	5	250	500	ns
		10	100	200	
		15	70	140	
Transition Time,	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance,	C_{IN}	Any Input	5	7.5	pF

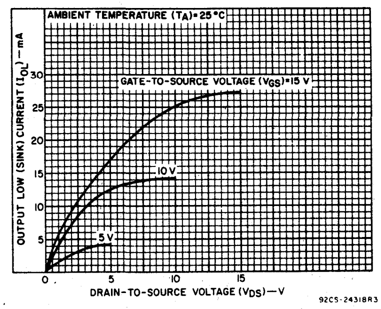


Fig. 7 – Typical output low (sink) current characteristics.

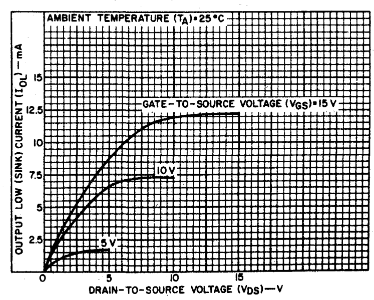


Fig. 8 – Minimum output low (sink) current characteristics.

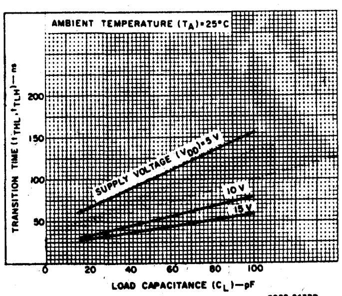


Fig. 9 – Typical transition time vs. load capacitance.

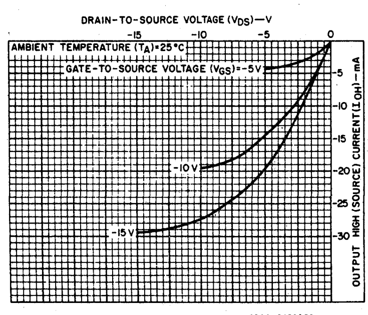


Fig. 10 – Typical output high (source) current characteristics.

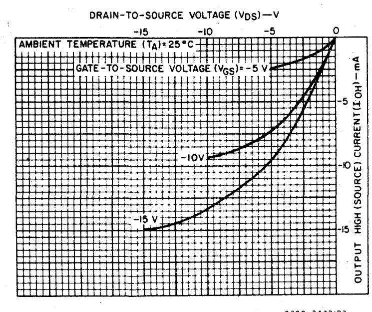


Fig. 11 – Minimum output high (source) current characteristics.

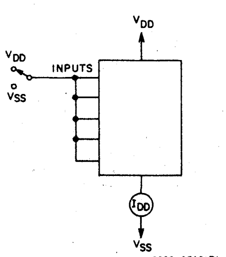


Fig. 12 – Quiescent device current test circuit.

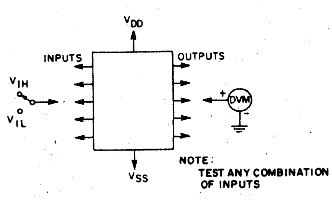


Fig. 13 – Input voltage test circuit.

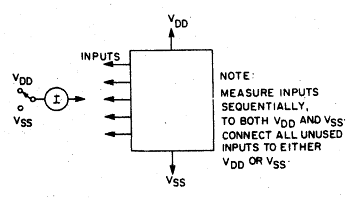


Fig. 14 – Input current test circuit.

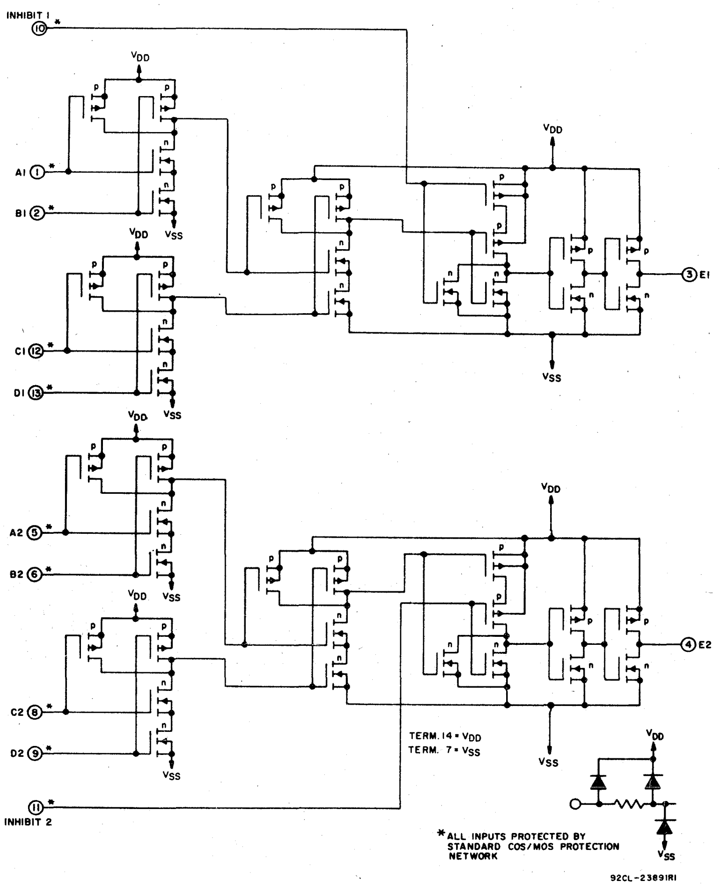
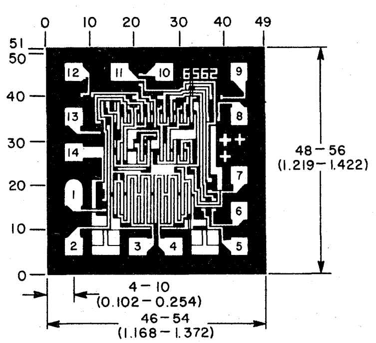


Fig. 15 – CD4085 schematic diagram.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and Pad Layout for CD4085BH.

COS/MOS Expandable 4-Wide 2-Input AND-OR-INVERT Gate

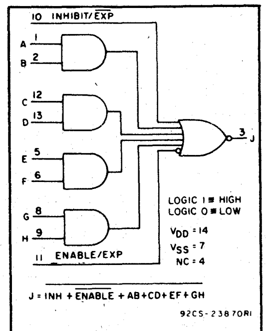
High-Voltage Types (20-Volt Rating)

The RCA-CD4086B contains one 4-wide 2-input AND-OR-INVERT gate with an INHIBIT/$\overline{EXP}$ input and an ENABLE/EXP input. For a 4-wide A-O-I function INHIBIT/$\overline{EXP}$ is tied to V_{SS} and ENABLE/EXP to V_{DD}. See Fig.10 and its associated explanation for applications where a capability greater than 4-wide is required.

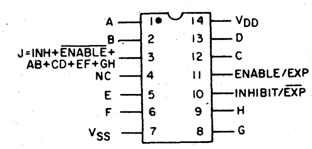
The CD4086B is supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Medium-speed operation — t_{PHL} = 90 ns; t_{PLH} = 140 ns (typ.) at 10 V**
- **INHIBIT and ENABLE inputs**
- **Buffered outputs**
- **100% tested for quiescent current at 20 V**
- **Maximum input leakage current of 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package termperature range):**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM



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Top View

TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

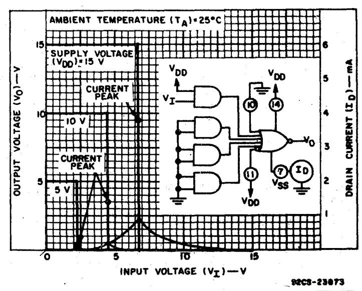

Fig. 1 – Typical voltage and current transfer characteristics.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

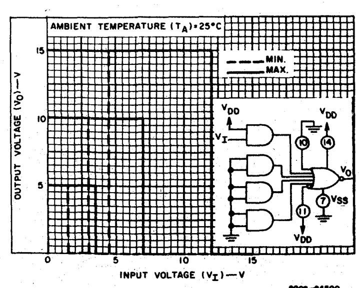

Fig. 2 – Minimum and maximum voltage transfer characteristics.

CD4086B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at –55,+25,+125 Apply to D,F,H Pkgs. Values at –40,+25,+85 Apply to E Pkgs. –55	–40	+85	+125	+25 Min.	Typ.	Max.	UNITS
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

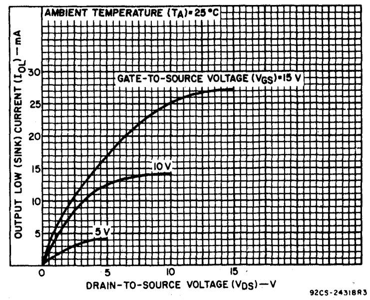

Fig. 3 – Typical output low (sink) current characteristics.

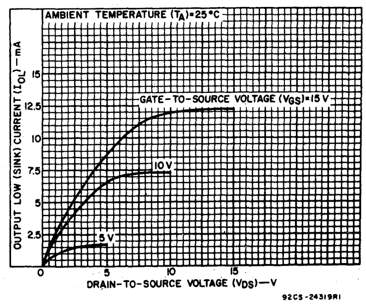

Fig. 4 – Minimum output low (sink) current characteristics.

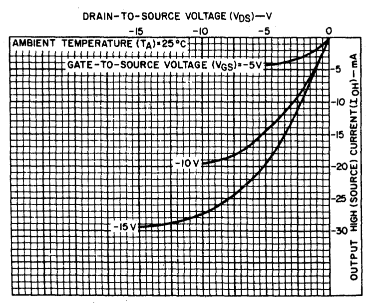

Fig.5 – Typical output high (source) current characteristics.

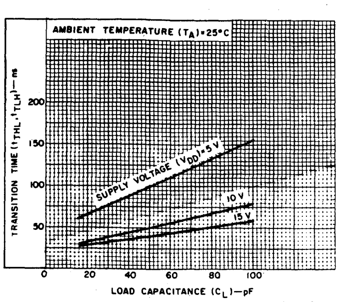

Fig.6 – Typical transition time vs. load capacitance.

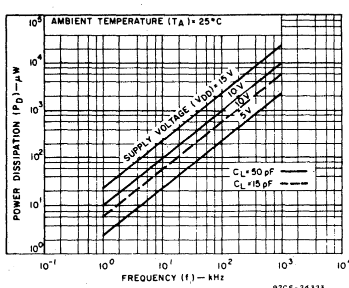

Fig.7 – Typical power dissipation vs. frequency.

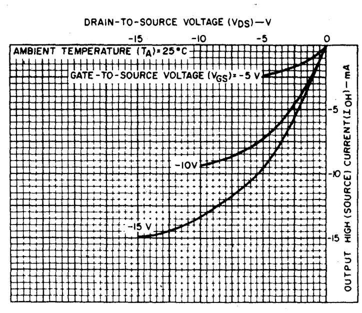

Fig.8 – Minimum output high (source) current characteristics.

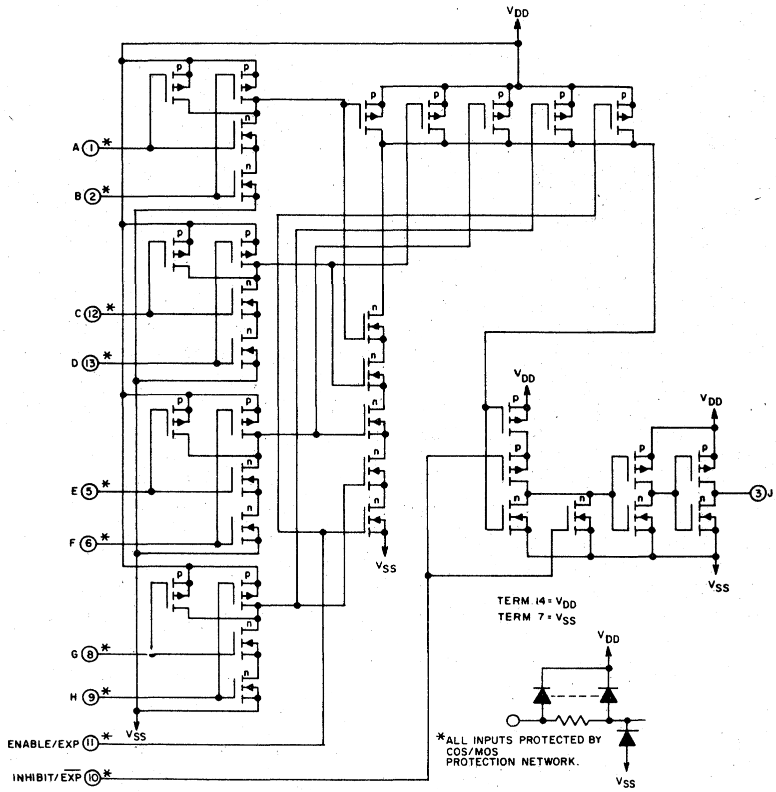

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Fig. 9 – CD4086B schematic diagram.

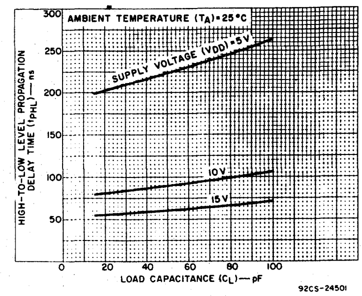

Fig. 11 – Typical DATA or ENABLE high-to-low level propagation delay time vs. load capacitance.

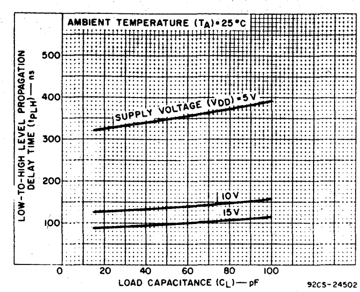

Fig. 12 – Typical DATA or ENABLE low-to-high level propagation delay time vs. load capacitance.

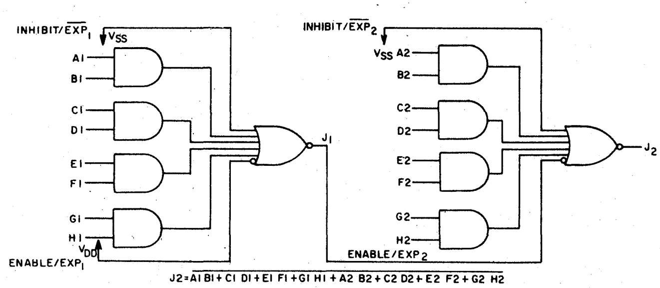

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Fig. 10 – Two CD4086B's connected as an 8-wide 2-input A-O-I gate.

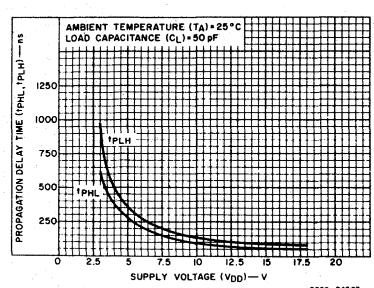


Fig. 13 – Typical DATA or ENABLE propagation delay time vs. supply voltage.

Fig. 10 above shows two CD4086's utilized to obtain an 8-wide 2-input A-O-I function. The output (J1) of one CD4086 is fed directly to the ENABLE/EXP2 line of the second CD4086. In a similar fashion, any NAND gate output can be fed directly into the ENABLE/EXP input to obtain a 5-wide A-O-I function. In addition, any AND gate output can be fed directly into the INHIBIT/$\overline{EXP}$ input with the same result.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	CONDITIONS		LIMITS		UNITS
		V_{DD} (V)	TYP.	MAX.	
Propagation Delay Time (Data): High-to-Low Level, t_{PHL}		5	225	450	ns
		10	90	180	
		15	60	120	
Low-to-High Level, t_{PLH}		5	310	620	ns
		10	125	250	
		15	90	180	
Propagation Delay Time (Inhibit): High-to-Low Level, $t_{PHL(INH)}$		5	150	300	ns
		10	60	120	
		15	40	80	
Low-to-High Level, $t_{PLH(INH)}$		5	250	500	ns
		10	100	200	
		15	70	140	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance C_{IN}	Any Input		5	7.5	pF

TEST CIRCUITS

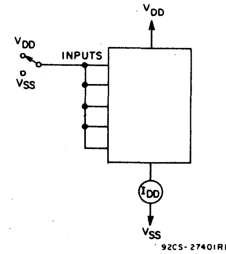


Fig. 14 – Quiescent device current.

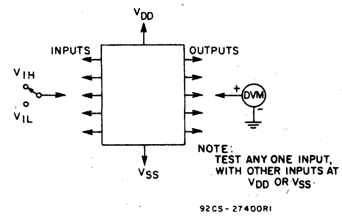


Fig. 15 – Input voltage.

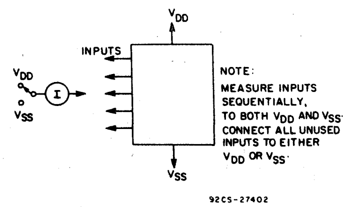
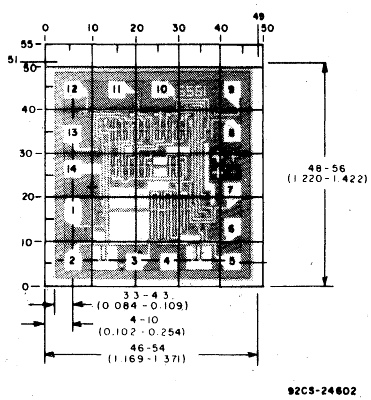


Fig. 16 – Input leakage current.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and Pad Layout for the CD4086BH

COS/MOS Binary Rate Multiplier

High-Voltage Types (20-Volt Rating)

The RCA-CD4089B is a low-power 4-bit digital rate multiplier that provides an output pulse rate that is the clock-input-pulse rate multiplied by 1/16 times the binary input. For example, when the binary input number is 13, there will be 13 output pulses for every 16 input pulses. This device may be used in conjunction with an up/down counter and control logic used to perform arithmetic operations (adds, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigometric functions, A/D and D/A conversions, and frequency division.

For words of more than 4 bits, CD4089B devices may be cascaded in two different modes: an Add mode and a Multiply mode (see Figs.14 and 15). In the Add mode some of the gaps left by the more significant unit at the count of 15 are filled in by the less significant units. For example, when two units are cascaded in the Add mode and programmed to 11 and 13, respectively, the more significant unit will have 11 output pulses for every 16 input pulses and the other unit will have 13 output pulses for every 256 input pulses for a total of

$$\frac{11}{16}+\frac{13}{256}=\frac{189}{256}$$

In the Multiply mode the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second multiplier. Thus the output rate will be

$$\frac{11}{16}\times\frac{13}{16}=\frac{143}{256}$$

Features:

- Cascadable in multiples of 4-bits
- Set to "15" input and "15" detect output
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

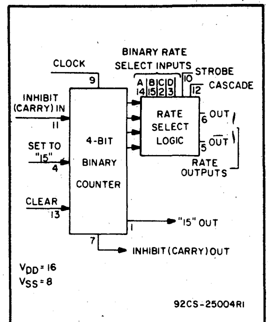
Applications:

- Numerical control
- Instrumentation
- Digital filtering
- Frequency synthesis

The CD4089B has an internal synchronous 4-bit counter which, together with one of the four binary input bits, produces pulse trains as shown in Fig. 2.

If more than one binary input bit is high, the resulting pulse train is a combination of the separate pulse trains as shown in Fig. 2.

The CD4089B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



FUNCTIONAL DIAGRAM

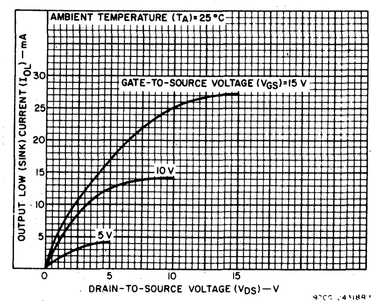


Fig. 1 — Typical output low (sink) current characteristics.

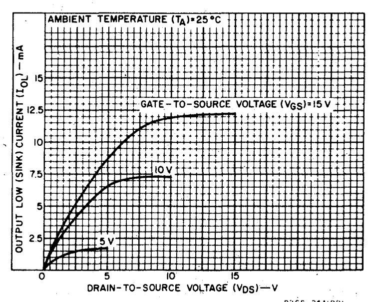


Fig. 2 — Minimum output low (sink) current characteristics.

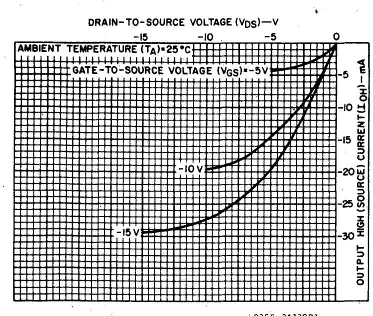


Fig. 3 — Typical output high (source) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)			3	18	V
Set or Clear Pulse Width,	t_W	5 10 15	160 90 60	– – –	ns
Clock Pulse Width,	t_W	5 10 15	330 170 100	– – –	ns
Clock Frequency,	f_{CL}	5 10 15	dc	1.2 2.5 3.5	MHz
Clock Rise or Fall Time,	t_{rCL} or t_{fCL}	5, 10,15	–	15	μs
Inhibit In Setup Time,	t_{SU}	5 10 15	100 40 20	– – –	ns
Inhibit In Removal Time,	t_{REM}	5 10 15	240 130 110	– – –	ns
Set Removal Time,	t_{REM}	5 10 15	150 80 50	– – –	ns
Clear Removal Time,	t_{REM}	5 10 15	60 40 30	– – –	ns

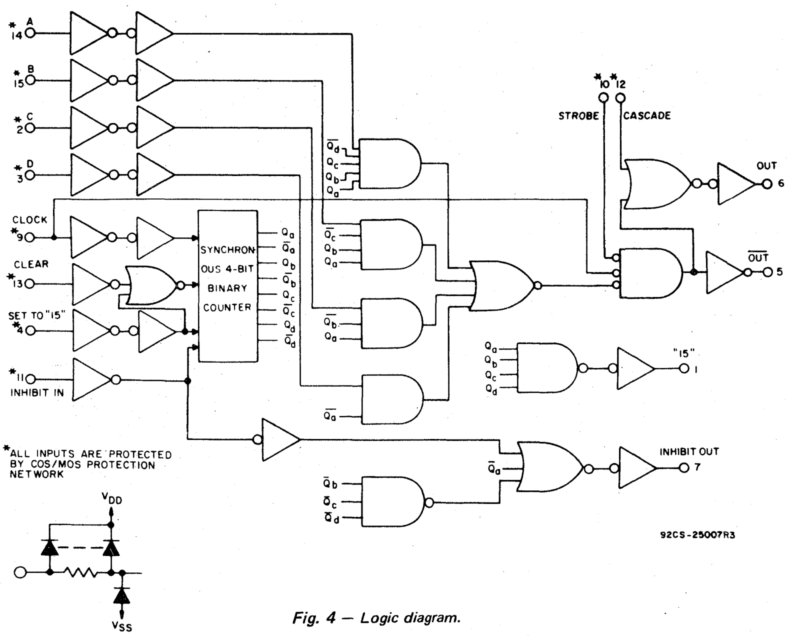


Fig. 4 – Logic diagram.

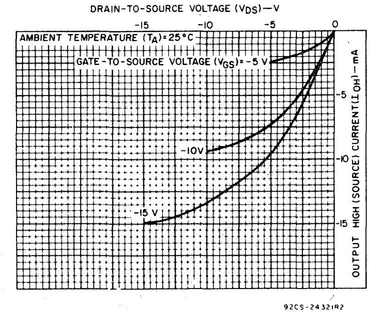


Fig. 5 – Minimum output high (source) current characteristics.

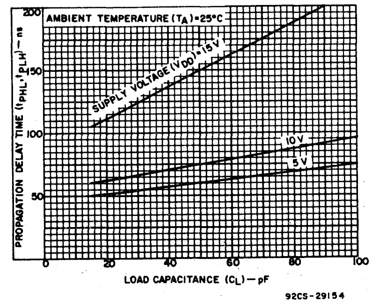


Fig. 6 – Typical propagation delay time as a function of load capacitance (Clock or Strobe to Out).

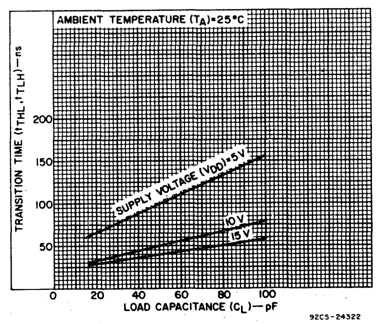


Fig. 7 – Typical transition time as a function of load capacitance.

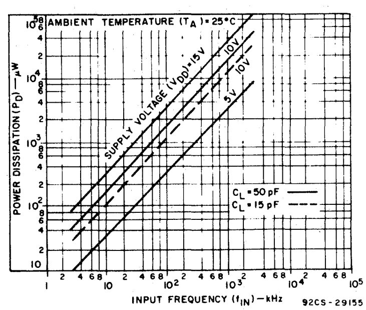


Fig. 8 – Typical dynamic power dissipation as a function of input frequency.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C;
Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} V	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH} Clock to $\overline{Out}$	5	–	110	220	ns
	10	–	55	110	
	15	–	45	90	
Clock or Strobe to Out	5	–	150	300	
	10	–	75	150	
	15	–	60	120	
Clock to Inhibit Out High Level to Low Level	5	–	360	720	ns
	10	–	160	320	
	15	–	110	220	
Low Level to High Level	5	–	250	500	ns
	10	–	100	200	
	15	–	75	150	
Clear to Out	5	–	380	760	ns
	10	–	175	350	
	15	–	130	260	
Clock to "9" or "15" Out	5	–	300	600	ns
	10	–	125	250	
	15	–	90	180	
Cascade to Out	5	–	90	180	ns
	10	–	45	90	
	15	–	35	70	
Inhibit In to Inhibit Out	5	–	160	320	ns
	10	–	75	150	
	15	–	55	110	
Set to Out	5	–	330	660	
	10	–	150	300	
	15	–	110	220	
Transition Time, t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Maximum Clock Frequency, f_{CL}	5	1.2	2.4	–	MHz
	10	2.5	5	–	
	15	3.5	7	–	
Minimum Clock Pulse Width, t_W	5	–	165	330	ns
	10	–	85	170	
	15	–	50	100	
Clock Rise or Fall Time, t_{rCL}, t_{fCL}	5	–	–	15	μs
	10	–	–	15	
	15	–	–	15	
Minimum Set or Clear Pulse Width, t_W	5	–	80	160	ns
	10	–	45	90	
	15	–	30	60	
Minimum Inhibit-In Setup Time, t_{SU}	5	–	50	100	ns
	10	–	20	40	
	15	–	10	20	
Minimum Inhibit In Removal Time, t_{REM}	5	–	120	240	ns
	10	–	65	130	
	15	–	55	110	

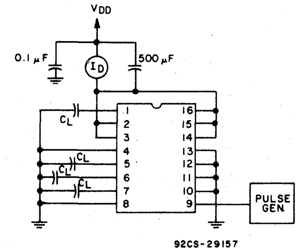


Fig. 9 — Dynamic power dissipation test circuit.

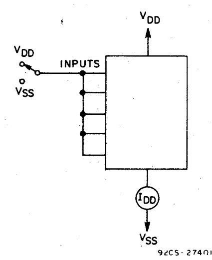


Fig. 10 — Quiescent device current test circuit.

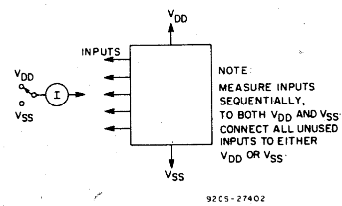


Fig. 11 — Input-current test circuit.

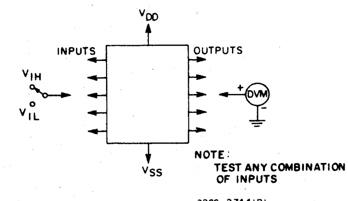
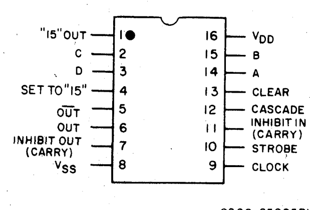


Fig. 12 — Input-voltage test circuit.



TOP VIEW
TERMINAL ASSIGNMENT

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C (cont'd)
Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} V	LIMITS Min.	Typ.	Max.	UNITS
Minimum Set Removal Time, t_{REM}		5 10 15	– – –	75 40 25	150 80 50	ns
Minimum Clear Removal Time, t_{REM}		5 10 15	– – –	30 20 15	60 40 30	ns
Input Capacitance, C_{IN}	Any Input	–	–	5	7.5	pF

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
				LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages; Values at −40, +25, +85 Apply to E Package							
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

TRUTH TABLE

INPUTS										OUTPUTS			
Number of Pulses or Input Logic Level (0 = Low; 1 = High; X = Don't Care)										Number of Pulses or Output Logic Level (L = Low; H = High)			
D	C	B	A	CLK	INH IN	STR	CAS	CLR	SET	OUT	$\overline{OUT}$	INH OUT	"15" OUT
0	0	0	0	16	0	0	0	0	0	L	H	1	1
0	0	0	1	16	0	0	0	0	0	1	1	1	1
0	0	1	0	16	0	0	0	0	0	2	2	1	1
0	0	1	1	16	0	0	0	0	0	3	3	1	1
0	1	0	0	16	0	0	0	0	0	4	4	1	1
0	1	0	1	16	0	0	0	0	0	5	5	1	1
0	1	1	0	16	0	0	0	0	0	6	6	1	1
0	1	1	1	16	0	0	0	0	0	7	7	1	1
1	0	0	0	16	0	0	0	0	0	8	8	1	1
1	0	0	1	16	0	0	0	0	0	9	9	1	1
1	0	1	0	16	0	0	0	0	0	10	10	1	1
1	0	1	1	16	0	0	0	0	0	11	11	1	1
1	1	0	0	16	0	0	0	0	0	12	12	1	1
1	1	0	1	16	0	0	0	0	0	13	13	1	1
1	1	1	0	16	0	0	0	0	0	14	14	1	1
1	1	1	1	16	0	0	0	0	0	15	15	1	1
X	X	X	X	16	1	0	0	0	0	†	†	H	†
X	X	X	X	16	0	1	0	0	0	L	H	1	1
X	X	X	X	16	0	0	1	0	0	H	*	1	1
1	X	X	X	16	0	0	0	1	0	16	16	H	L
0	X	X	X	16	0	0	0	1	0	L	H	H	L
X	X	X	X	16	0	0	0	X	1	L	H	L	H

* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).
† Depends on internal state of counter.

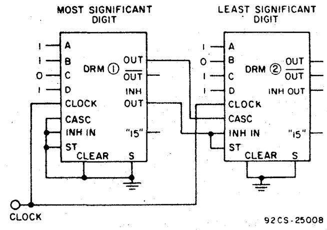


Fig. 13 – Two CD4089B's cascaded in the "Add" mode with a preset number of 189 $\left(\frac{11}{16}+\frac{13}{256}=\frac{189}{256}\right)$.

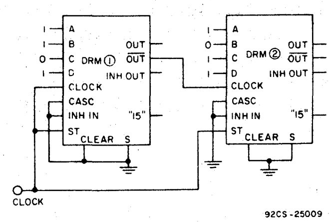


Fig. 14 – Two CD4089B's cascaded in the "Multiply" mode with a preset number of 143 $\left(\frac{11}{16}\times\frac{13}{16}=\frac{143}{256}\right)$.

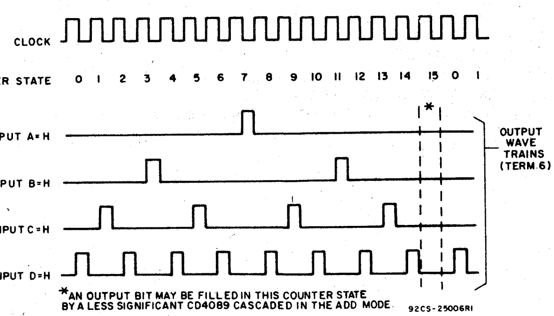
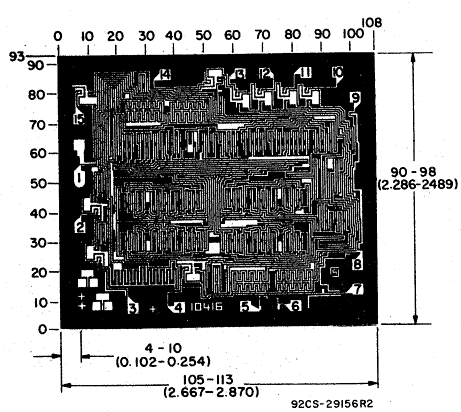


Fig. 15 – Timing diagram.



Dimensions and Pad Layout for CD4089BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Quad 2-Input NAND Schmitt Triggers

High-Voltage Types (20 Volt Rating)

The RCA-CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive- and negative-going signals. The difference between the positive voltage (V_P) and the negative voltage (V_N) is defined as hysteresis voltage (V_H) (see Fig. 2).

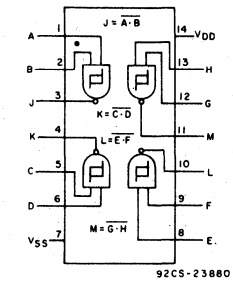
The CD4093B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- Schmitt-trigger action on each input with no external components
- Hysteresis voltage typically 0.9 V at V_{DD} = 5 V and 2.3 V at V_{DD} = 10 V
- Noise immunity greater than 50%
- No limit on input rise and fall times
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range, 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators
- NAND logic



FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	MIN.	MAX.	UNITS
Supply-Voltage Range (T_A = Full Package-Temp. Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . −55 to +125°C
PACKAGE TYPE E . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . +265°C

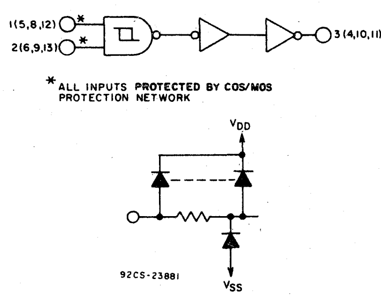
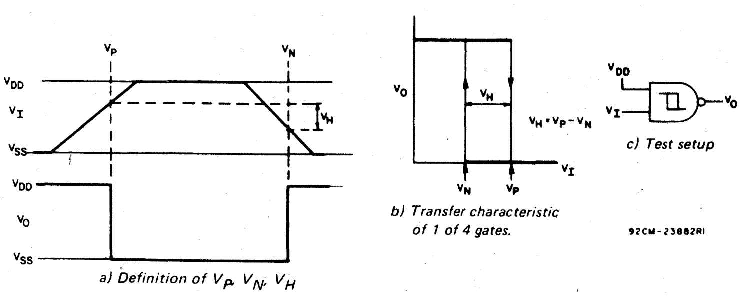


Fig. 1 – Logic diagram—1 of 4 Schmitt triggers.



a) Definition of V_P, V_N, V_H

b) Transfer characteristic of 1 of 4 gates.

c) Test setup

Fig. 2 – Hysteresis definition, characteristic, and test setup.

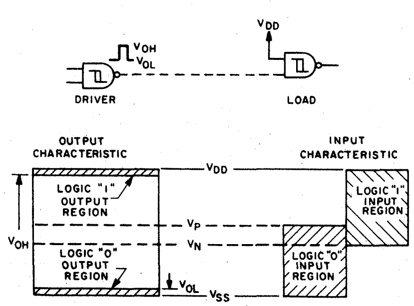


Fig. 3 – Input and output characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER-ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages Values at −40, +25, +85 Apply to E Packages							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 MIN.	+25 TYP.	+25 MAX.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Positive Trigger Threshold Voltage V_P Min.	–	a	5	2.2	2.2	2.2	2.2	2.2	2.9	–	V
	–	a	10	4.6	4.6	4.6	4.6	4.6	5.9	–	
	–	a	15	6.8	6.8	6.8	6.8	6.8	8.8	–	
	–	b	5	2.6	2.6	2.6	2.6	2.6	3.3	–	
	–	b	10	5.6	5.6	5.6	5.6	5.6	7	–	
	–	b	15	6.3	6.3	6.3	6.3	6.3	9.4	–	
V_P Max.	–	a	5	3.6	3.6	3.6	3.6	–	2.9	3.6	V
	–	a	10	7.1	7.1	7.1	7.1	–	5.9	7.1	
	–	a	15	10.8	10.8	10.8	10.8	–	8.8	10.8	
	–	b	5	4	4	4	4	–	3.3	4	
	–	b	10	8.2	8.2	8.2	8.2	–	7	8.2	
	–	b	15	12.7	12.7	12.7	12.7	–	9.4	12.7	
Negative Trigger Threshold Voltage V_N Min.	–	a	5	0.9	0.9	0.9	0.9	0.9	1.9	–	V
	–	a	10	2.5	2.5	2.5	2.5	2.5	3.9	–	
	–	a	15	4	4	4	4	4	5.8	–	
	–	b	5	1.4	1.4	1.4	1.4	1.4	2.3	–	
	–	b	10	3.4	3.4	3.4	3.4	3.4	5.1	–	
	–	b	15	4.8	4.8	4.8	4.8	4.8	7.3	–	
V_N Max.	–	a	5	2.8	2.8	2.8	2.8	–	1.9	2.8	V
	–	a	10	5.2	5.2	5.2	5.2	–	3.9	5.2	
	–	a	15	7.4	7.4	7.4	7.4	–	5.8	7.4	
	–	b	5	3.2	3.2	3.2	3.2	–	2.3	3.2	
	–	b	10	6.6	6.6	6.6	6.6	–	5.1	6.6	
	–	b	15	9.6	9.6	9.6	9.6	–	7.3	9.6	
Hysteresis Voltage V_H Min.	–	a	5	0.3	0.3	0.3	0.3	0.3	0.9	–	V
	–	a	10	1.2	1.2	1.2	1.2	1.2	2.3	–	
	–	a	15	1.6	1.6	1.6	1.6	1.6	3.5	–	
	–	b	5	0.3	0.3	0.3	0.3	0.3	0.9	–	
	–	b	10	1.2	1.2	1.2	1.2	1.2	2.3	–	
	–	b	15	1.6	1.6	1.6	1.6	1.6	3.5	–	
V_H Max.	–	a	5	1.6	1.6	1.6	1.6	–	0.9	1.6	V
	–	a	10	3.4	3.4	3.4	3.4	–	2.3	3.4	
	–	a	15	5	5	5	5	–	3.5	5	
	–	b	5	1.6	1.6	1.6	1.6	–	0.9	1.6	
	–	b	10	3.4	3.4	3.4	3.4	–	2.3	3.4	
	–	b	15	5	5	5	5	–	3.5	5	

[a] Input on terminals 1,5,8,12 or 2,6,9,13; other inputs to V_{DD}.

[b] Input on terminals 1 and 2, 5 and 6,8 and 9, or 12 and 13; other inputs to V_{DD}.

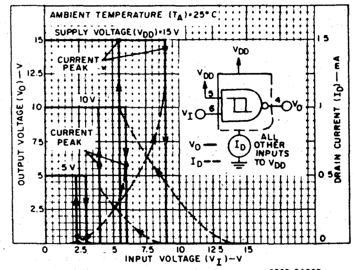


Fig. 4 – Typical current and voltage transfer characteristics.

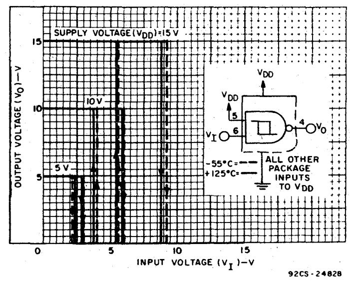


Fig. 5 – Typical voltage transfer characteristics as a function of temperature.

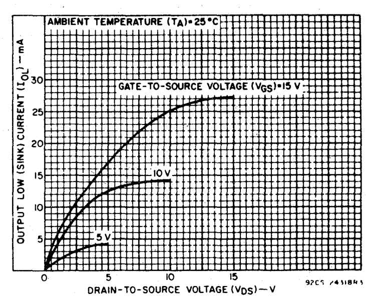


Fig. 6 – Typical output low (sink) current characteristics.

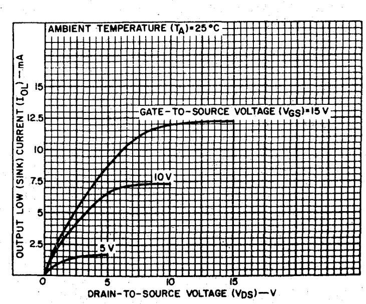


Fig. 7 – Minimum output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS (CONT'D)

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURE (°C) Values at −55, +25, +125 Apply to D, F, H Packages; Values at −40, +25, +85 Apply to E Packages							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 MIN.	+25 TYP.	+25 MAX.	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95		–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

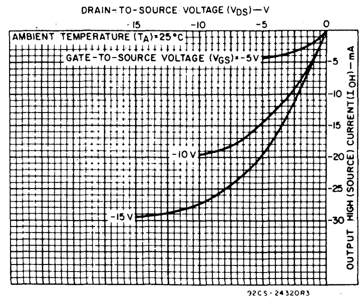


Fig. 8 – Typical output high (source) current characteristics.

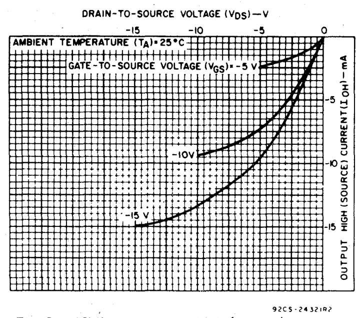


Fig. 9 – Minimum output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} VOLTS	LIMITS TYP.	LIMITS MAX.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH}		5	190	380	ns
		10	90	180	
		15	65	130	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

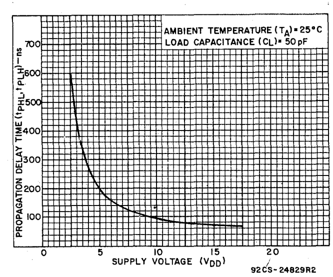


Fig. 10 – Typical propagation delay time vs. supply voltage.

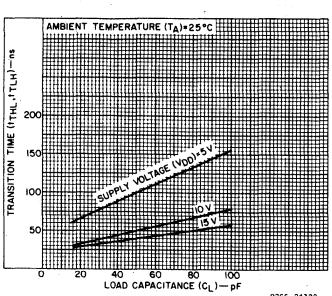


Fig. 11 – Typical transition time vs. load capacitance.

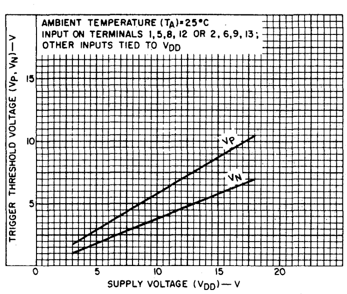


Fig. 12 – Typical trigger threshold voltage vs. V_{DD}.

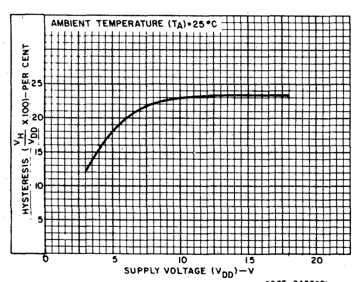


Fig. 13 – Typical per cent hysteresis vs. supply voltage.

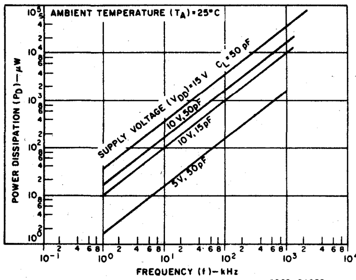


Fig. 14 – Typical power dissipation vs. frequency characteristics.

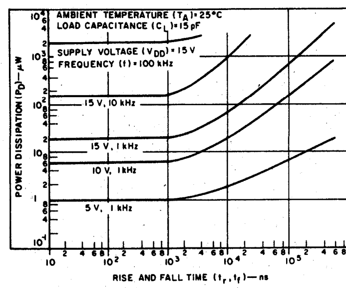
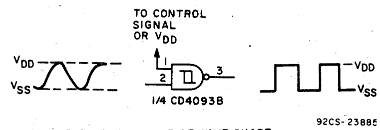


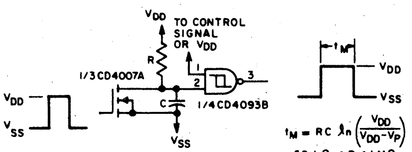
Fig. 15 – Typical power dissipation vs. rise and fall times.

APPLICATIONS



FREQUENCY RANGE OF WAVE SHAPE IS FROM DC TO 1 MHz

Fig. 16 – Wave shaper.



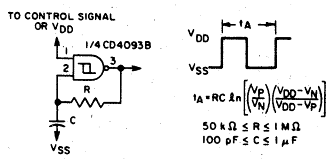
$t_M = RC \ln\left(\frac{V_{DD}}{V_{DD}-V_P}\right)$

50 kΩ ≤ R ≤ 1 MΩ
100 pF ≤ C ≤ 1 µF

FOR THE RANGE OF R AND C GIVEN 5 µs < t_M < 1s

92CS-23886R1

Fig. 17 – Monostable multivibrator.



$t_A = RC \ln\left[\left(\frac{V_P}{V_N}\right)\left(\frac{V_{DD}-V_N}{V_{DD}-V_P}\right)\right]$

50 kΩ ≤ R ≤ 1 MΩ
100 pF ≤ C ≤ 1 µF

FOR THE RANGE OF R AND C GIVEN 2 µs < t_A < 0.4 s

92CS-23887R1

Fig. 18 – Astable multivibrator.

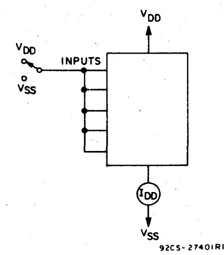


Fig. 19 – Quiescent device current test circuit.

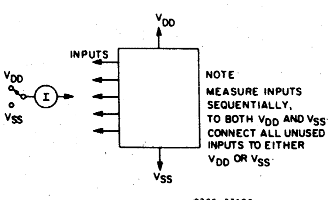
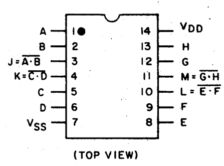
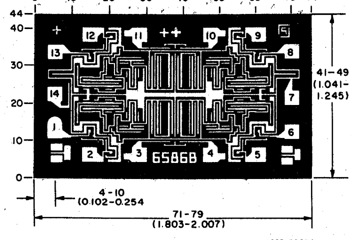


Fig. 20 – Input current test circuit.



TERMINAL ASSIGNMENT



Dimensions and Pad Layout for CD4093BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS 8-Stage Shift-and-Store Bus Register

High-Voltage Types (20-Volt Rating)

The RCA-CD4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high.

Two serial outputs are available for cascading a number of CD4094B devices. Data is available at the Q_S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q'_S terminal on the next negative clock edge, provides a means for cascading CD4094B devices when the clock rise time is slow.

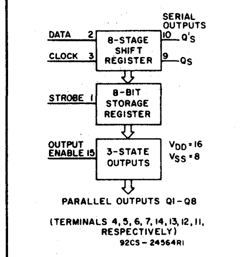
The CD4094B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **3-state parallel outputs for connection to common bus**
- **Separate serial outputs synchronous to both positive and negative clock edges for cascading**
- **Medium speed operation – 5 MHz at 10 V (typ.)**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package temperature range):**
  1 V at V_{DD} = 5 V   2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Serial-to-parallel data conversion**
- **Remote control holding register**
- **Dual-rank shift, hold, and bus applications**



FUNCTIONAL DIAGRAM

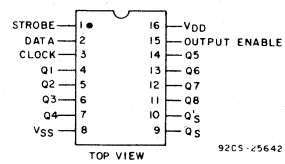


Fig. 1 – Terminal assignment.

MAXIMUM RATINGS, ***Absolute-Maximum Values:***

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	–0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	–55 to +125°C
PACKAGE TYPE E	–40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	–65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

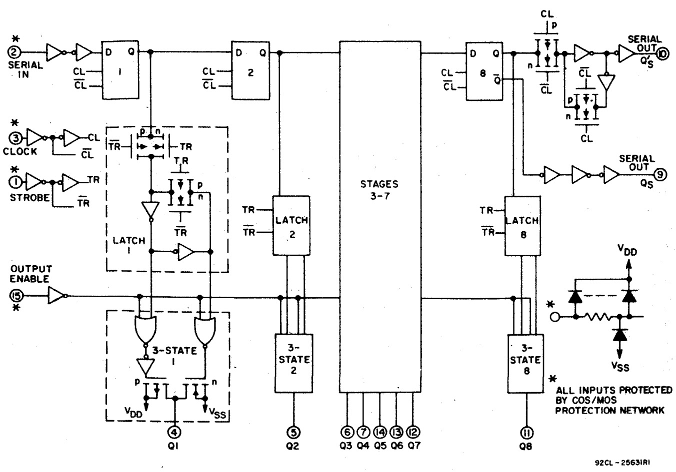


Fig. 2 – CD4094B Logic diagram.

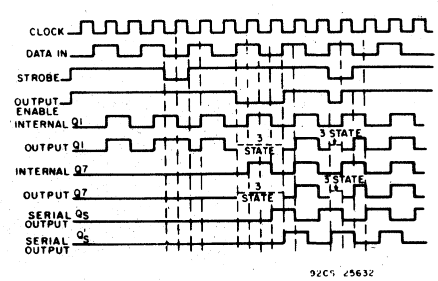


Fig. 3 – Timing diagram.

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:*

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5 10 15	125 55 35	– – –	ns
Clock Pulse Width, t_W	5 10 15	200 100 83	– – –	ns
Clock Input Frequency, f_{CL}	5 10 15	dc	1.25 2.5 3	MHz
Clock Input Rise or Fall time, t_rCL, t_fCL:*	5 10 15	–	15 5 5	μs
Strobe Pulse Width, t_W	5 10 15	200 80 70	– – –	ns

*If more than one unit is cascaded t_fCL (for Q_S only) should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the output driving stage for the estimated capacitive load.

TRUTH TABLE

CL▲	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	QN	QS*	Q'S
↑	0	X	X	OC	OC	Q7	NC
↓	0	X	X	OC	OC	NC	Q7
↑	1	0	X	NC	NC	Q7	NC
↑	1	1	0	0	Q_{N-1}	Q7	NC
↑	1	1	1	1	Q_{N-1}	Q7	NC
↓	1	1	1	NC	NC	NC	Q7

▲ = Level Change
X = Don't Care
NC = No Change
OC = Open Circuit

Logic 1 ≡ High
Logic 0 ≡ Low

* At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the Q_S output.

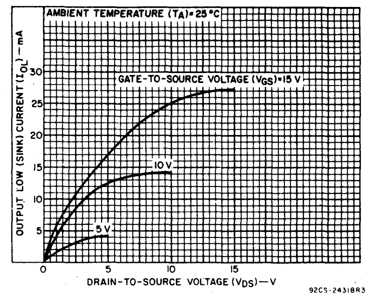


Fig. 4 – Typical output low (sink) current characteristics.

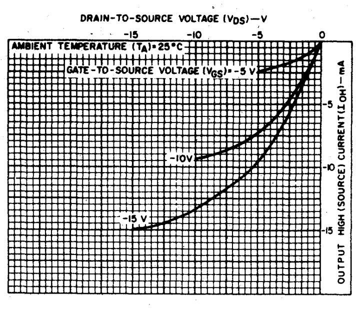


Fig. 5 – Minimum output low (sink) current characteristics.

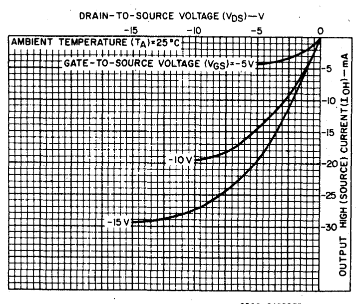


Fig. 6 – Typical output high (source) current characteristics.

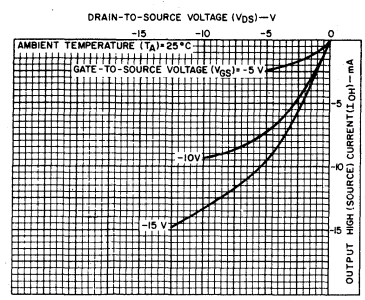


Fig. 7 – Minimum output high (source) current characteristics.

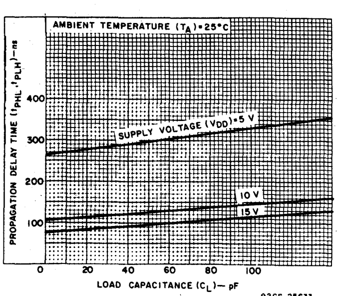


Fig. 8 – Clock-to-serial output Q_S propagation delay vs C_L.

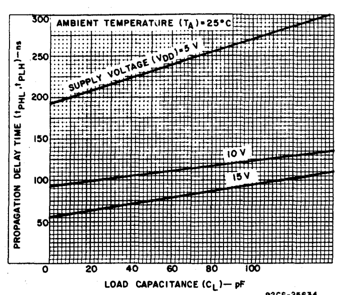


Fig. 9 – Clock-to-serial output Q'_S propagation delay vs C_L.

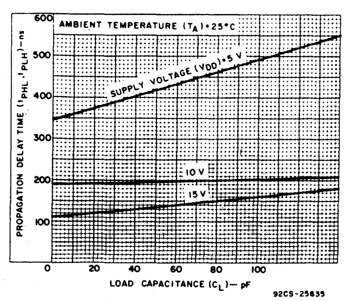


Fig. 10 – Clock-to-parallel output propagation delay vs C_L.

CD4094B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm10^{-4}$	±0.4	μA

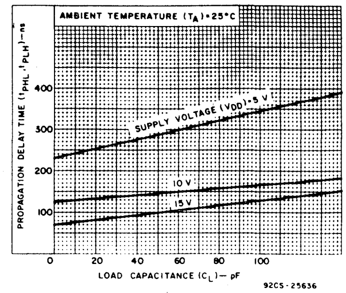


Fig. 11 – Strobe-to-parallel output propagation delay vs C_L.

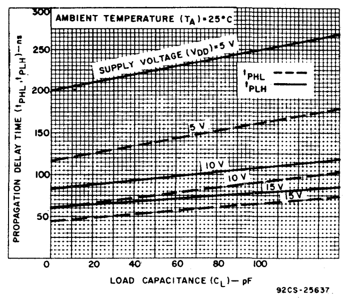


Fig. 12 – Output enable-to-parallel output propagation delay vs C_L.

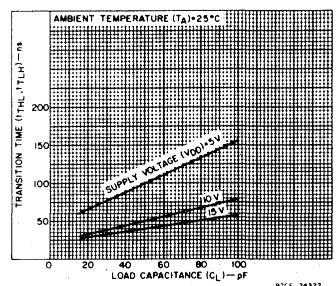


Fig. 13 – Typical transition time vs. load capacitance.

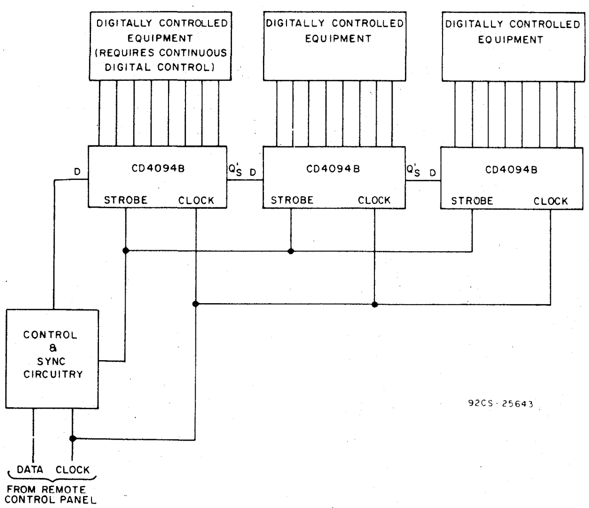


Fig. 14 – Remote control holding register.

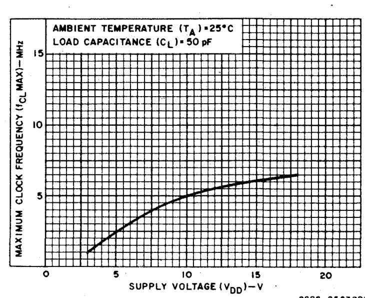


Fig. 15 – Typical maximum-clock-frequency vs. supply voltage.

DYNAMIC ELECTRICAL CHARACTERISTICS
At T_A=25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	VDD (V)	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH} Clock to Serial Output Q_S	5 10 15	– – –	300 125 95	600 250 190	ns
Clock to Serial Output Q'_S	5 10 15	– – –	230 110 75	460 220 150	ns
Clock to Parallel Output	5 10 15	– – –	420 195 135	840 390 270	ns
Strobe to Parallel Output	5 10 15	– – –	290 145 100	580 290 200	ns
Output Enable to Parallel Output: Output High to High Impedance, t_{PHZ}	5 10 15	– – –	140 75 55	280 150 110	ns
Output Low to High Impedance, t_{PLZ}	5 10 15	– – –	225 95 70	450 190 140	ns
Minimum Strobe Pulse Width, t_W	5 10 15	– – –	100 40 35	200 80 70	ns
Minimum Clock Pulse Width, t_W	5 10 15	– – –	100 50 40	200 100 83	ns
Minimum Data Setup Time, t_S	5 10 15	– – –	60 30 20	125 55 35	ns
Transition Time; t_{THL}, t_{TLH}	5 10 15	– – –	100 50 40	200 100 80	ns
Maximum Clock Input Rise or Fall Time, t_rCL, t_fCL	5 10 15	15 5 5	– – –	– – –	µs
Maximum Clock Input Frequency, f_{CL}	5 10 15	1.25 2.5 3	2.5 5 6	– – –	MHz
Input Capacitance C_{IN} (Any Input)	–	–	5	7.5	pF

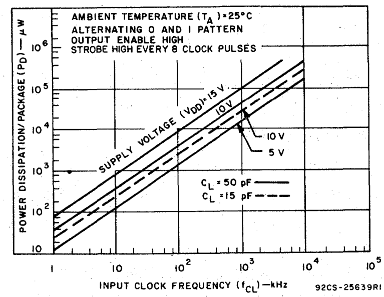


Fig. 16 – Dynamic power dissipation vs input clock frequency.

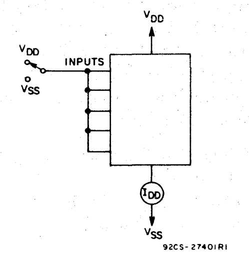


Fig. 17 – Quiescent device current test circuit.

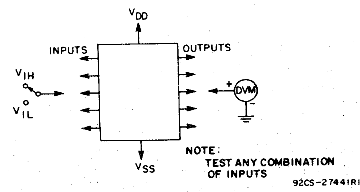


Fig. 18 – Input voltage test circuit.

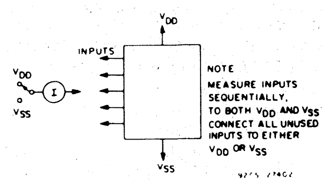
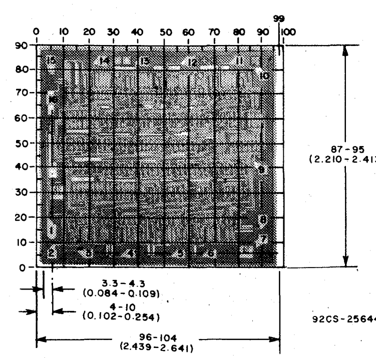


Fig. 19 – Input current test circuit.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and Pad Layout for CD4094B Chip.

CD4095B, CD4096B Types

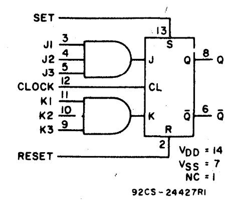
COS/MOS Gated J-K Master-Slave Flip-Flops

With Set-Reset Capability

High-Voltage Types (20-Volt Rating)

CD4095B Non-Inverting J and K Inputs

CD4096B Inverting and Non-Inverting J and K Inputs



CD4095B
Functional Diagram

The RCA-CD4095B and CD4096B are J-K Master-Slave Flip-Flops featuring separate AND gating of multiple J and K inputs. The gated J-K inputs control transfer of information into the master section during clocked operation. Information on the J-K inputs is transferred to the Q and $\overline{Q}$ outputs on the positive edge of the clock pulse. SET and RESET inputs (active high) are provided for asynchronous operation.

The CD4095B and CD4096B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **16 MHz toggle rate (typ.) at $V_{DD} - V_{SS}$ = 10 V**
- **Gated inputs**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin over full package-temperature range: 1 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Registers**
- **Counters**
- **Control circuits**

TRUTH TABLES

SYNCHRONOUS OPERATION (S=0 R=0)

Inputs Before Positive Clock Transition		Outputs After Positive Clock Transition	
J*	K*	Q	$\overline{Q}$
0	0	No Change	
0	1	0	1
1	0	1	0
1	1	Toggles	

* For CD4095B: J = J1 · J2 · J3, K = K1 · K2 · K3

For CD4096B: J = J1 · J2 · $\overline{J3}$, K = K1 · K2 · $\overline{K3}$

ASYNCHRONOUS OPERATION (J and K - DON'T CARE)

S	R	Q	$\overline{Q}$
0	0	No Change	
0	1	0	1
1	0	1	0
1	1	0	0

0 = V_{SS}, 1 = V_{DD}

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . −55 to +125°C
PACKAGE TYPE E . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . +265°C

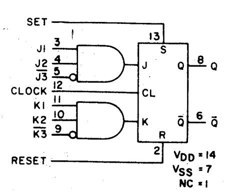


Fig. 1 – CD4096B Functional Diagram.

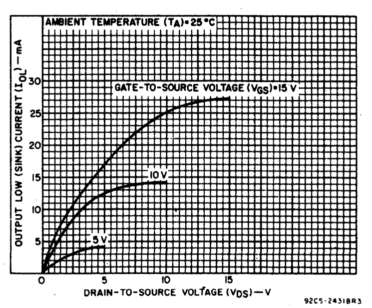


Fig.2 – Typical output low (sink) current characteristics.

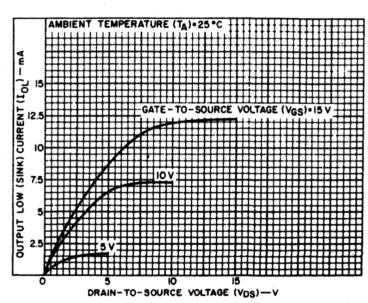


Fig.3 – Minimum output low (sink) current characteristics.

RECOMMENDED OPERATING CONDITIONS at T_A = 25° C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5	400	–	ns
	10	160	–	
	15	100	–	
Clock Pulse Width, t_W	5	140	–	ns
	10	60	–	
	15	40	–	
Clock Input Frequency, f_{CL}	5	dc	3.5	MHz
	10		8	
	15		12	
Clock Rise and Fall Time, t_rCL, t_fCL:	5	–	15	μs
	10	–	5	
	15	–	5	
Set or Reset Pulse Width, t_W	5	200	–	ns
	10	100	–	
	15	50	–	

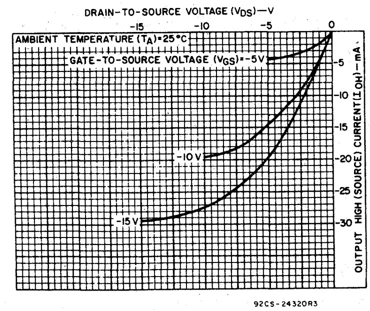


Fig.4 – Typical output high (source) current characteristics.

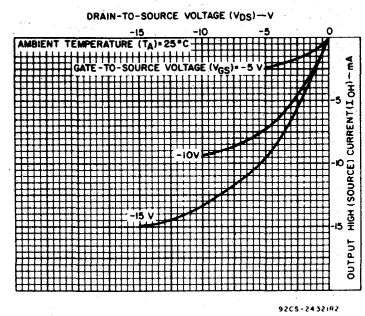


Fig.5 – Minimum output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages Values at –40, +25, +85 Apply to E Package –55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5, 13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5, 13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

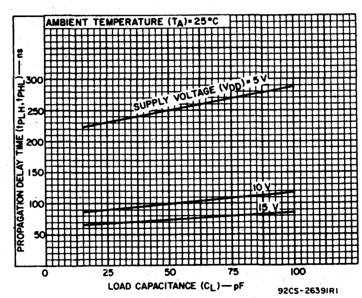


Fig.6 – Typical propagation delay time vs. load capacitance.

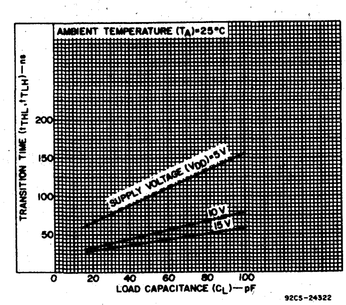


Fig.7 – Typical transition time vs. load capacitance.

CD4095B, CD4096B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
		V_{DD} (V)	MIN.	TYP.	MAX.	
Propagation Delay Time: t_{PHL}, t_{PLH} Clock		5	–	250	500	ns
		10	–	100	200	
		15	–	75	150	
Set or Reset		5	–	150	300	
		10	–	75	150	
		15	–	50	100	
Transition Time, t_{THL}, t_{TLH}		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Maximum Clock Input Frequency, (f_{CL})*		5	3.5	7	–	MHz
		10	8	16	–	
		15	12	24	–	
Minimum Clock Pulse Width, t_W		5	–	70	140	ns
		10	–	30	60	
		15	–	20	40	
Clock Input Rise or Fall Time, t_{rcl}, t_{rcf}		5	–	–	15	μs
		10	–	–	5	
		15	–	–	5	
Minimum Set or Reset Pulse Width, t_W		5	–	100	200	ns
		10	–	50	100	
		15	–	25	50	
Minimum Data Setup Time, t_S		5	–	200	400	ns
		10	–	80	160	
		15	–	50	100	
Input Capacitance, C_{IN}	Any Input	–	–	5	7.5	pF

* t_r, t_f = 5 ns

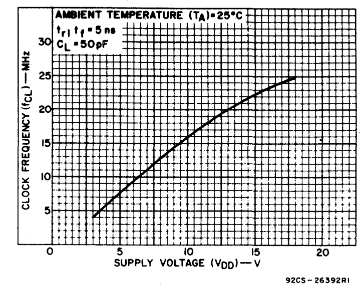


Fig.8 – Typical clock frequency vs. supply voltage (toggle mode—see Fig. 16).

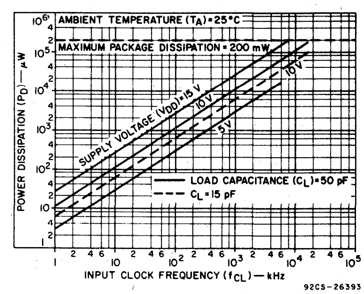


Fig. 9 – Typical power dissipation vs. input clock frequency.

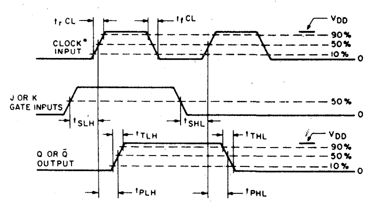


Fig.10 – Propagation delay, transition, and setup-time waveforms.

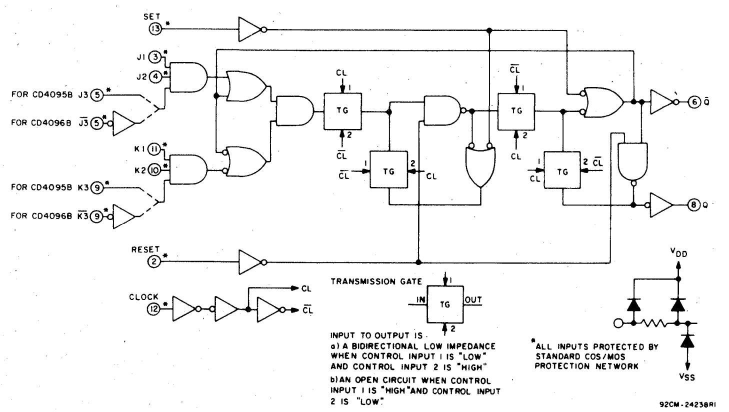


Fig.11 – CD4095B and CD4096B logic diagram.

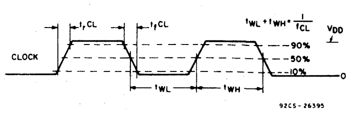


Fig.12 – Clock pulse rise and fall time waveforms.

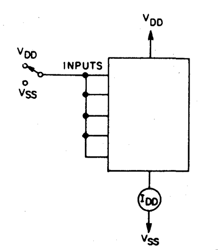


Fig.13 – Quiescent device current test circuit.

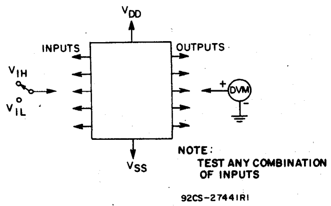


Fig.14 – Input voltage test circuit.

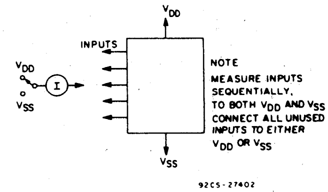


Fig.15 – Input leakage current test circuit.

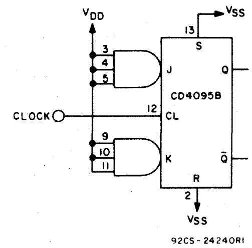


Fig.16 – CD4095B connected in toggle mode.

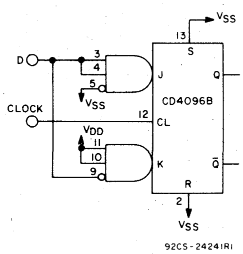
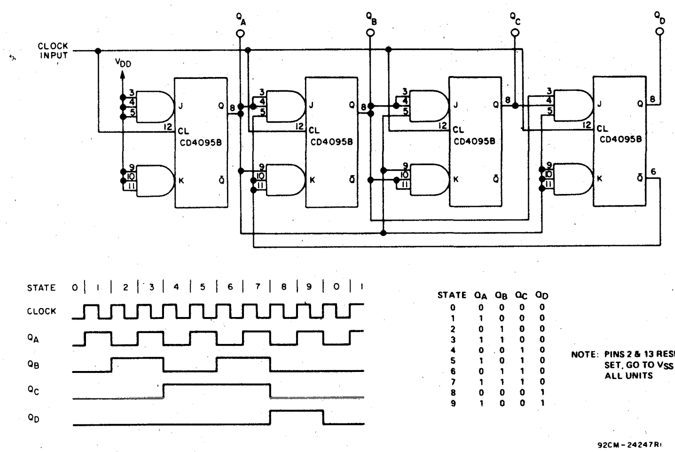


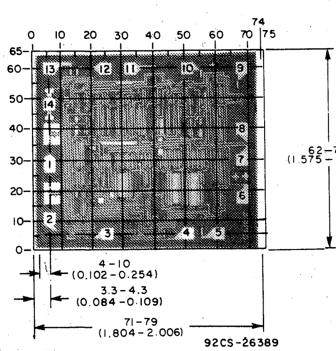
Fig.17 – CD4096B connected as a "D" type flip-flop.



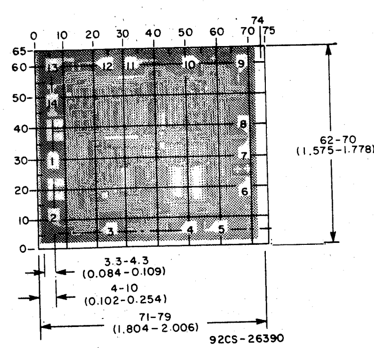
STATE	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

Fig. 18 – Synchronous binary divide-by-ten counter.

DIMENSIONS AND PAD LAYOUT FOR CD4095B AND CD4096B



CD4095BH

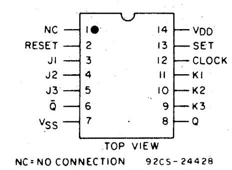


CD4096BH

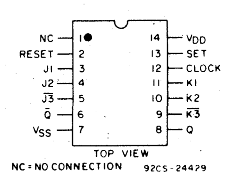
The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

TERMINAL ASSIGNMENTS



CD4095B



CD4096B

CD4098B Types

COS/MOS Dual Monostable Multivibrator

High-Voltage Types (20-Volt Rating)

The RCA-CD4098B dual monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor (R_X) and an external capacitor (C_X) control the timing for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_X and C_X.

Leading-edge-triggering (+TR) and trailing-edge-triggering (−TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to V_{SS}. An unused −TR input should be tied to V_{DD}. A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to V_{DD}. However, if an entire section of the CD4098B is not used, its RESET should be tied to V_{SS}. See Table I.

In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode, $\overline{Q}$ is connected to −TR when leading-edge triggering (+TR) is used or Q is connected to +TR when trailing-edge triggering (−TR) is used.

The time period (T) for this multivibrator can be approximated by: $T_X = ½R_XC_X$ for $C_X \geqslant 0.01\ \mu F$. Time periods as a function of R_X for values of C_X and V_{DD} are given in Fig. 8. Values of T vary from unit to unit and as a function of voltage, temperature, and R_XC_X.

The minimum value of external resistance, R_X, is 5 kΩ. The maximum value of external capacitance, C_X, is 100 μF. Fig. 9 shows time periods as a function of C_X for values of R_X and V_{DD}.

The output pulse width has variations of ±2.5% typically, over the temperature range of −55°C to 125°C for C_X=1000 pF and R_X=100 kΩ.

For power supply variations of ±5%, the output pulse width has variations of ±0.5% typically, for V_{DD}=10 V and 15 V and ±1% typically, for V_{DD}=5 V at C_X=1000 pF and R_X=5 kΩ.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

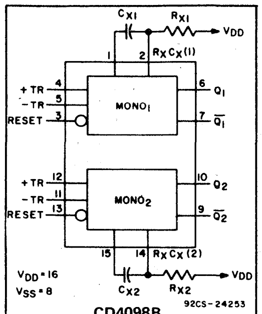
The CD4098B is similar to type MC14528.

Features:

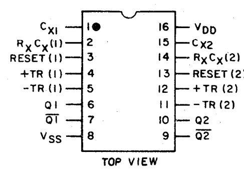
- **Retriggerable/resettable capability**
- **Trigger and reset propagation delays independent of R_X, C_X**
- **Triggering from leading or trailing edge**
- **Q and $\overline{Q}$ buffered outputs available**
- **Separate resets**
- **Wide range of output-pulse widths**
- **100% tested for maximum quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range): 1 V at V_{DD}= 5 V; 2 V at V_{DD}=10 V; 2.5 V at V_{DD}=15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices."**

Applications:

- **Pulse delay and timing**
- **Pulse shaping**
- **Astable multivibrator**



CD4098B
Functional Diagram



TERMINALS 1,8,15 ARE ELECTRICALLY CONNECTED INTERNALLY

92CS-24848R1

TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} V	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	—	3	18	V
Trigger Pulse Width t_W(TR)	5 10 15	140 60 40	— — —	ns
Reset Pulse Width t_W(R) (This is a function of C_X)	—	See Dynamic Char. Chart and Fig. 10		—
Trigger Rise or Fall Time t_r(TR), t_f(TR)	5 - 15	—	100	μs

TABLE I

CD4098B FUNCTIONAL TERMINAL CONNECTIONS

FUNCTION	V_{DD} TO TERM. NO.		V_{SS} TO TERM. NO.		INPUT PULSE TO TERM. NO.		OTHER CONNECTIONS	
	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$
Leading-Edge Trigger/ Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/ Non-retriggerable	3	13			4	12	5-7	11-9
Trailing-Edge Trigger/ Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/ Non-retriggerable	3	13			5	11	4-6	12-10
Unused Section	5	11	3, 4	12, 13				

NOTES:

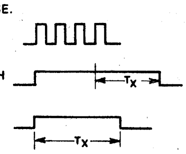
1. A RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS AN OUTPUT PULSE WIDTH WHICH IS EXTENDED ONE FULL TIME PERIOD (T_X) AFTER APPLICATION OF THE LAST TRIGGER PULSE.
   The minimum time between retriggering edges (or trigger and retrigger edges) is 40 per cent of (T_X).

2. A NON-RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS A TIME PERIOD T_X REFERENCED FROM THE APPLICATION OF THE FIRST TRIGGER PULSE.

INPUT PULSE TRAIN

RETRIGGERABLE MODE PULSE WIDTH (+TR MODE)

NON-RETRIGGERABLE MODE PULSE WIDTH (+TR MODE)



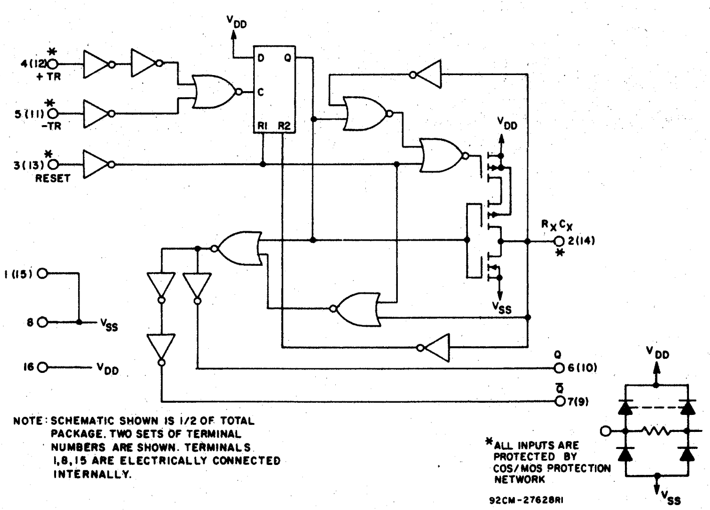


Fig. 4 – CD4098B logic diagram.

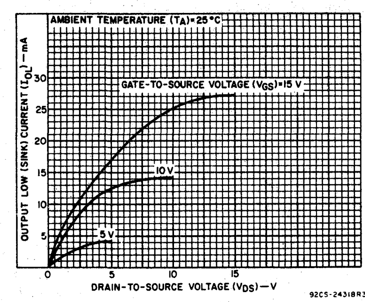


Fig. 1 – Typical output low (sink) current characteristics.

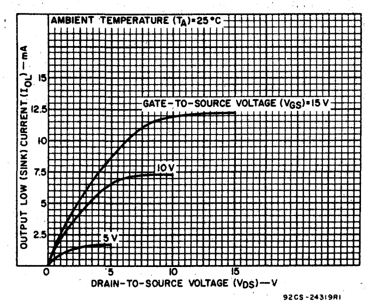


Fig. 2 – Minimum output low (sink) current characteristics.

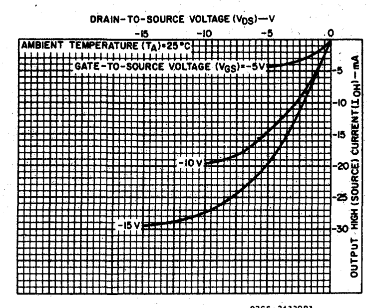


Fig. 3 – Typical output high (source) current characteristics.

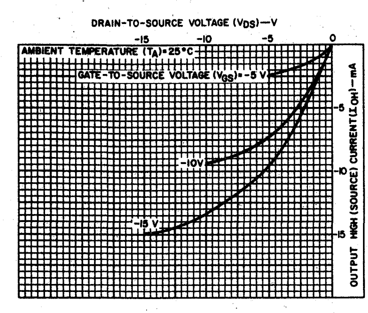


Fig. 5 – Minimum output high (source) current characteristics.

CD4098B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55,+25,+125 Apply to D,F,H Pkgs. Values at −40,+25,+85 Apply to E Pkgs.							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
Output Leakage I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	μA

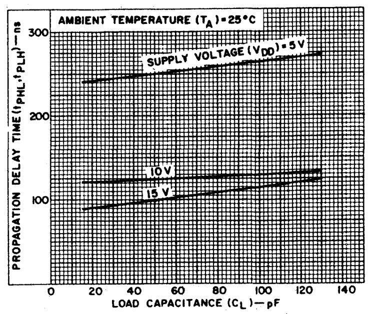


Fig. 6 – Typical propagation delay time vs. load capacitance, trigger into Q out. (All values of C_X and R_X.)

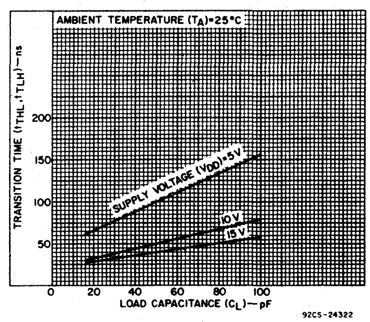


Fig. 7 – Transition time vs. load capacitance for R_X = 5 kΩ-10000 kΩ and C_X = 15 pF-10000 pF.

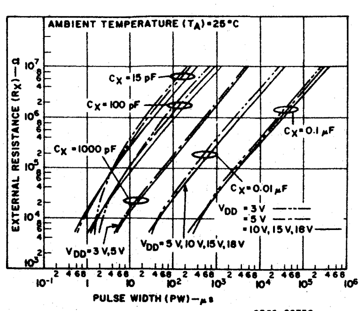


Fig. 8 – Typical external resistance vs. pulse width.

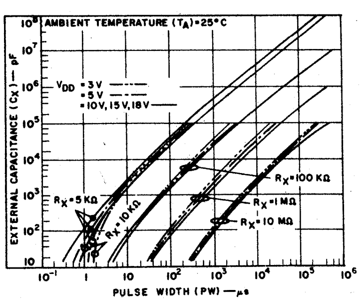


Fig. 9 – Typical external capacitance vs. pulse width.

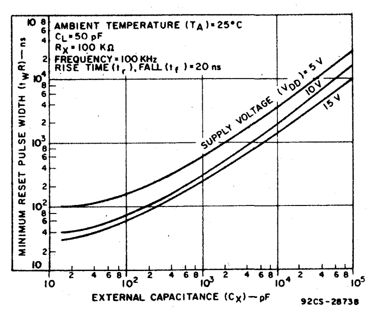


Fig. 10 – Typical minimum reset pulse width vs. external capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS
At $T_A = 25°C$; Input t_r, t_f=20 ns, C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS			LIMITS		UNITS
	R_X (kΩ)	C_X (pF)	V_{DD} (V)	Typ.	Max.	
Trigger Propagation Delay Time +TR, −TR to Q, $\bar{Q}$ t_{PHL}, t_{PLH}	5 to 10,000	⩾15	5	250	500	ns
			10	125	250	
			15	100	200	
Minimum Trigger Pulse Width, t_{WH}, t_{WL}	5 to 10,000	⩾15	5	70	140	ns
			10	30	60	
			15	20	40	
Transition Time, t_{TLH}	5 to 10,000	⩾15	5	100	200	ns
			10	50	100	
			15	40	80	
t_{THL}	5 to 10,000	15 to 10,000	5	100	200	
			10	50	100	
			15	40	80	
	5 to 10,000	0.01 μF to 0.1 μF	5	150	300	
			10	75	150	
			15	65	130	
	5 to 10,000	0.1 μF to 1 μF	5	250	500	
			10	150	300	
			15	80	160	
Reset Propagation Delay Time, T_{PHL}, T_{PLH}	5 to 10,000	⩾15	5	225	450	ns
			10	125	250	
			15	75	150	
Minimum Reset Pulse Width, t_{WR}	100	15	5	100	200	ns
			10	40	80	
			15	30	60	
		1000	5	600	1200	
			10	300	600	
			15	250	500	
		0.1 μF	5	25	50	μs
			10	15	30	
			15	10	20	
Trigger Rise or Fall Time t_r(TR), t_f(TR)	–	–	5 to 15	–	100	μs
Pulse Width Match Between Circuits in Same Package	10	10,000	5	5	10	%
			10	7.5	15	
			15	7.5	15	
Input Capacitance, C_{IN}	Any Input			5	7.5	pF

TEST CIRCUITS

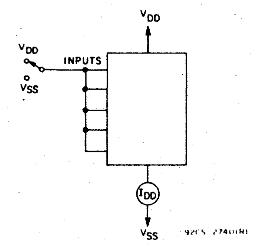


Fig. 12 – Quiescent-device-current test circuits.

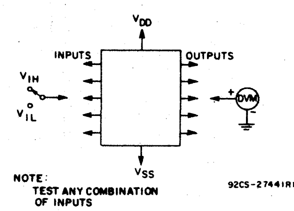


Fig. 13 – Input-voltage test circuit.

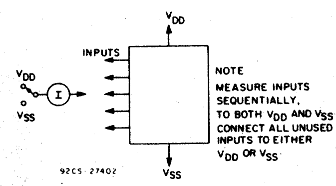


Fig. 14 – Input leakage current test circuit.

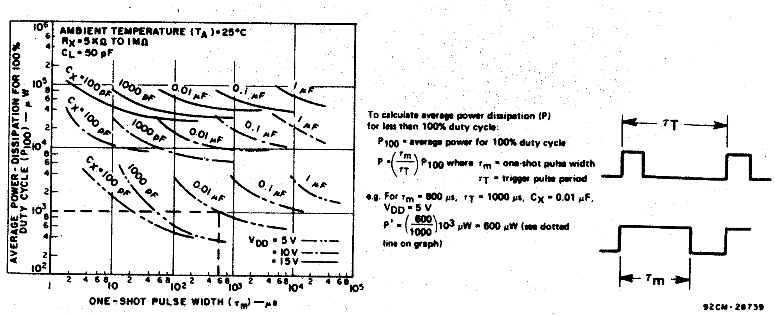


Fig. 11 – Average power dissipation vs. one-short pulse width.

CD4098B Types

APPLICATIONS

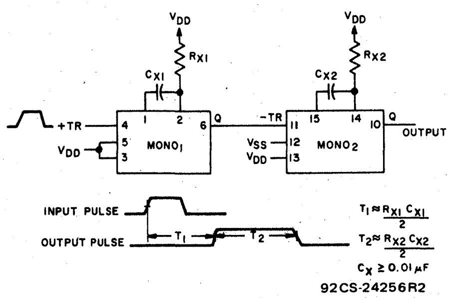
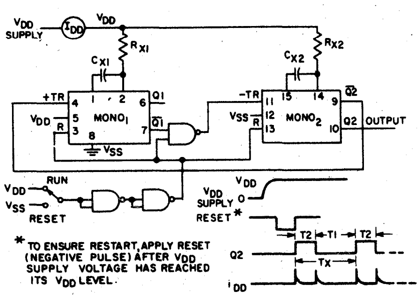


Fig. 15 – Pulse delay.



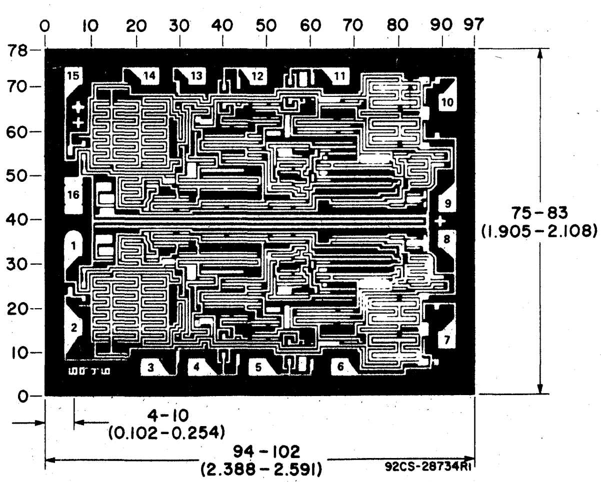
I_{DD}, T_X vs. R_X

R_X	I_{DD} (Avg.)	T_X (T1 + T2)	V_{DD}
10 kΩ	1 mA ↓ 0.05 mA	3.8 µs ↓ 0.5 s	5 V
↓	2.5 mA ↓ 0.5 mA	3.2 µs ↓ 0.5 s	10 V
10 MΩ	5 mA ↓ 1 mA	3 µs ↓ 0.5 s	15 V

Note:
All values are typical.
C_X range: 0.0001 µF to 0.1 µF.

92CM-28740

Fig. 16 – Astable multivibrator with restart after reset capability.



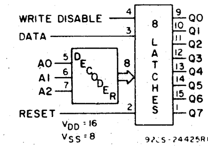
Dimensions and Pad Layout for CD4098BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photograph and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS
8-Bit Addressable Latch

High-Voltage Types (20-Volt Rating)



Functional Diagram

The RCA-CD4099B 8-bit addressable latch is a serial-input, parallel-output storage register that can perform a variety of functions.

Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when WRITE DISABLE is at a low level. When WRITE DISABLE is high, data entry is inhibited; however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs.

A master RESET input is available, which resets all bits to a logic "0" level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1-of-8 demultiplexer; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.

The CD4099B types are supplied in 16-lead hermetic ceramic dual-in-line packages (D and F suffixes), 16-lead plastic dual-in-line packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Serial data input**
- **Active parallel output**
- **Storage register capability**
- **Master clear**
- **Can function as demultiplexer**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V (full package-temperature range), 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) = 1 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Multi-line decoders**
- **A/D converters**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

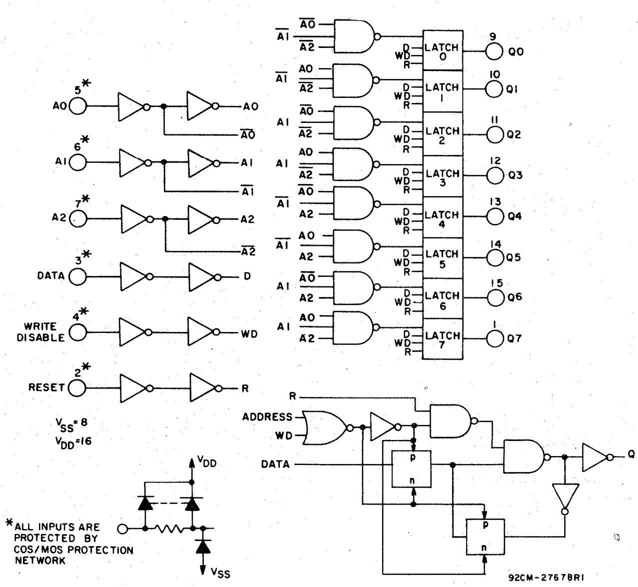
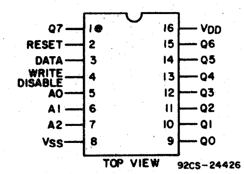


Fig. 1 — Logic diagram of CD4099B and detail of 1 of 8 latches.



TERMINAL ASSIGNMENT

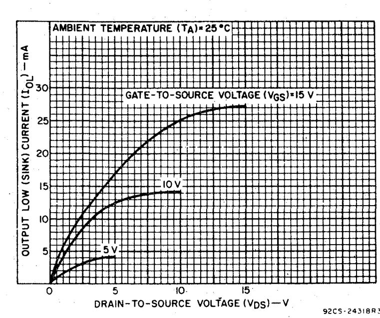


Fig. 2 — Typical output low (sink) current characteristics.

CD4099B Types

RECOMMENDED OPERATING CONDITIONS *at T_A = 25° C (Unless otherwise specified)*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	SEE FIG. 15*	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply Voltage Range: (At T_A = Full Package Temperature Range)			3	18	V
Minimum Pulse Width, t_W Data	4	5	200	–	ns
		10	100	–	
		15	80		
Address	8	5	400	–	
		10	200	–	
		15	125	–	
Reset	5	5	150	–	
		10	75	–	
		15	50	–	
Setup Time, t_S Data to WRITE DISABLE	6	5	100	–	ns
		10	50	–	
		15	35	–	
Hold Time, t_H Data to WRITE DISABLE	7	5	150	–	ns
		10	75	–	
		15	50	–	

* Circled numbers refer to times indicated on master timing diagram.

Note: In addition to the above characteristics, a WRITE DISABLE ON time (the time that WRITE DISABLE is at a high level) must be observed during an address change for the total time that the external address lines A0, A1, and A2 are settling to a stable level, to prevent a wrong cell from being addressed (see Fig. 3).

MODE SELECTION			
WD	R	ADDRESSED LATCH	UNADDRESSED LATCH
0	0	Follows Data	Holds Previous State
0	1	Follows Data	Reset to "0" (Active High 8-Channel Demultiplexer)
1	0	Holds Previous State	
1	1	Reset to "0"	Reset to "0"

WD = WRITE DISABLE R = RESET

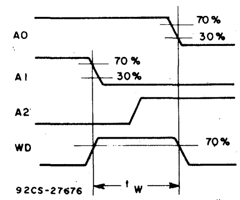


Fig. 3 – Definition of WRITE DISABLE ON time.

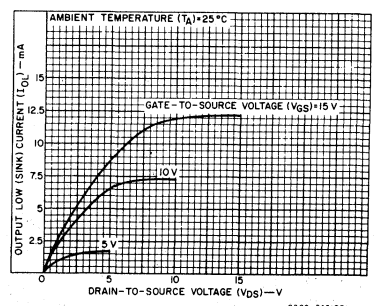


Fig. 4 — Minimum output low (sink) current characteristics.

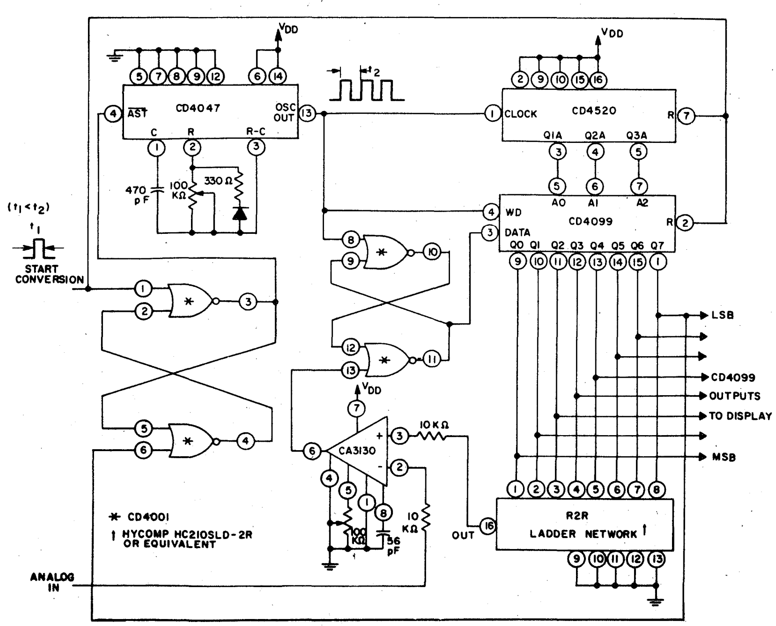


Fig. 5 — A/D converter 92CL-27681

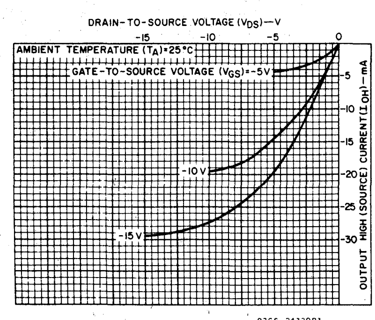
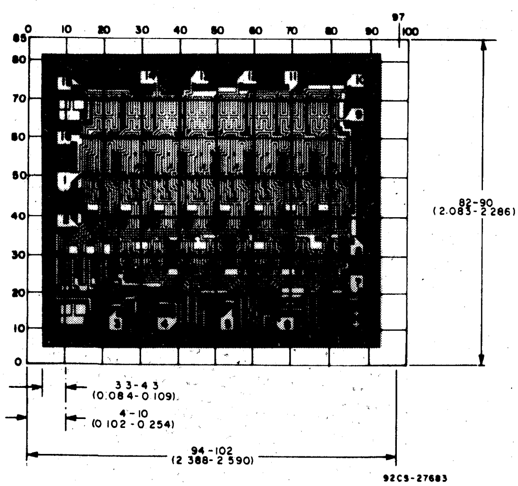


Fig. 6 — Typical output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA



CD4099BH
DIMENSIONS AND PAD LAYOUT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

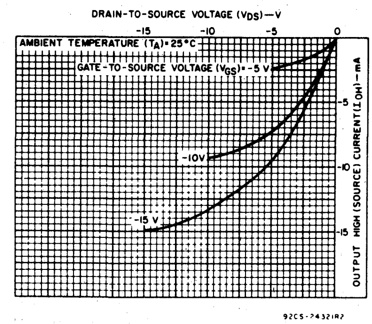


Fig.7 – Minimum output high (source) current characteristics.

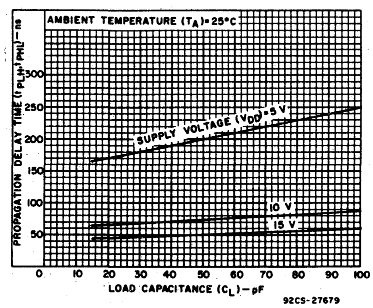


Fig. 8 – Typical propagation delay time (data to Qn) vs. load capacitance.

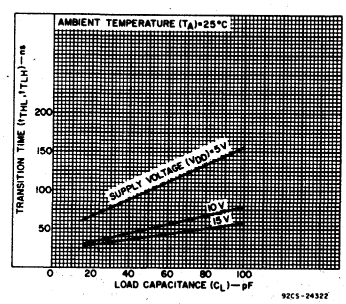


Fig. 9 – Typical transition time vs. load capacitance.

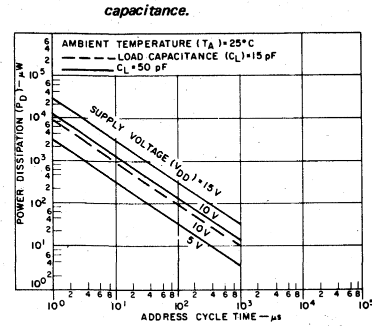


Fig.10 – Typical dynamic power dissipation vs. address cycle time.

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25°C$, $C_L = 50\,pF$, Input t_r, $t_f = 20\,ns$, $R_L = 200\,K\Omega$*

CHARACTERISTIC	CONDITIONS SEE FIG.15*	CONDITIONS V_{DD} (V)	LIMITS ALL PACKAGE TYPES TYP.	LIMITS ALL PACKAGE TYPES MAX.	UNITS
Propagation Delay: t_{PLH}, t_{PHL} Data to Output,	①	5	200	400	ns
		10	75	150	
		15	50	100	
WRITE DISABLE to Output, t_{PLH}, t_{PHL}	②	5	200	400	
		10	80	160	
		15	60	120	
Reset to Output, t_{PHL}	③	5	175	350	
		10	80	160	
		15	65	130	
Address to Output, t_{PLH}, t_{PHL}	⑨	5	225	450	
		10	100	200	
		15	75	150	
Transition Time, t_{THL}, (Any Output) t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Minimum Pulse Width, t_W Data	④	5	100	200	ns
		10	50	100	
		15	40	80	
Address	⑧	5	200	400	ns
		10	100	200	
		15	65	125	
Reset	⑤	5	75	150	ns
		10	40	75	
		15	25	50	
Minimum Setup Time, t_S Data to WRITE DISABLE	⑥	5	50	100	ns
		10	25	50	
		15	20	35	
Minimum Hold Time, t_H Data to WRITE DISABLE	⑦	5	75	150	ns
		10	40	75	
		15	25	50	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

*Circled numbers refer to times indicated on master timing diagram.

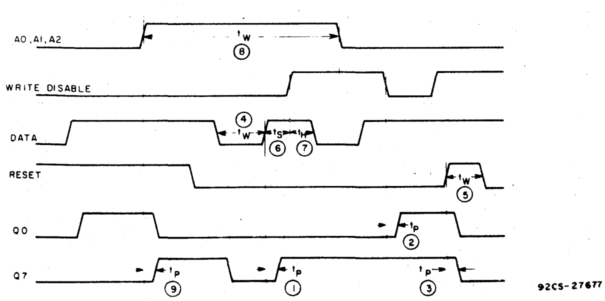


Fig. 15 — Master timing diagram.

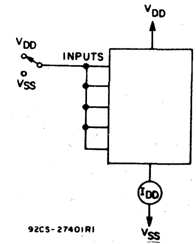


Fig. 11 — Quiescent device current test circuit.

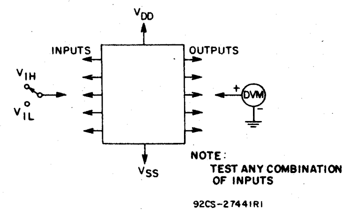


Fig. 12 — Input voltage test circuit.

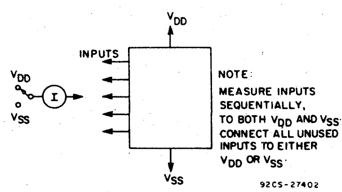


Fig. 13 — Input current test circuit.

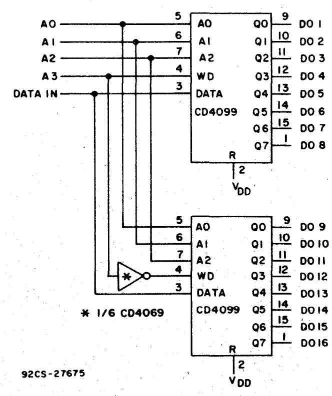


Fig. 14 — 1 of 16 decoder/demultiplexer.

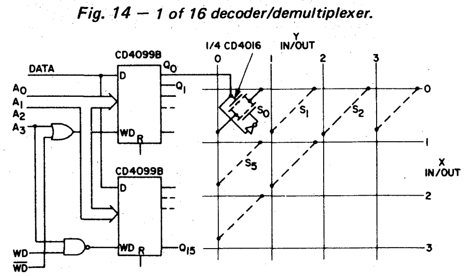


Fig. 16 — Multiple selection decoding — 4 x 4 crosspoint switch.

COS/MOS Strobed Hex Inverter/Buffer

High-Voltage Types (20-Volt Rating)

The RCA-CD4502B consists of six inverter/buffers with 3-state outputs. A logic "1" on the OUTPUT DISABLE input produces a high-impedance state in all six outputs. This feature permits common busing of the outputs, thus simplifying system design. A Logic "1" on the INHIBIT input switches all six outputs to logic "0" if the OUTPUT DISABLE input is a logic "0". This device is capable of driving two standard TTL loads, which is equivalent to six times the JEDEC "B"-series I_{OL} standard.

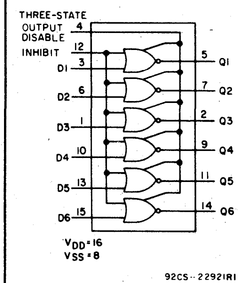
The CD4502B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix). This device is similar to the MC14502.

Features:

- 2 TTL-load output drive capability
- 3-state outputs
- Common output-disable control
- Inhibit control
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**
- **Noise margin (full package-temperature range) =**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V

Applications:

- **3-state hex inverter for interfacing IC's with data buses**
- **COS/MOS to TTL hex buffer**



FUNCTIONAL DIAGRAM

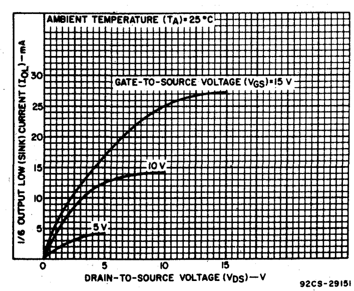


Fig.2 – Typical output low (sink) current characteristics.

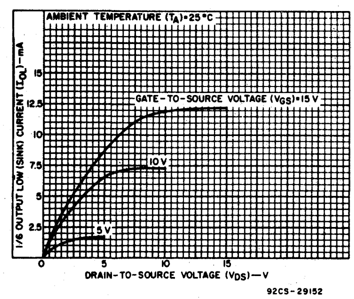


Fig.3 – Minimum output low (sink) current characteristics.

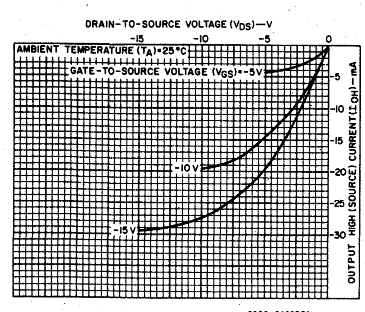


Fig.4 – Typical output high (source) current characteristics.

MAXIMUM RATINGS, ***Absolute-Maximum Values:***

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	–0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	–55 to +125°C
PACKAGE TYPE E	–40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	–65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

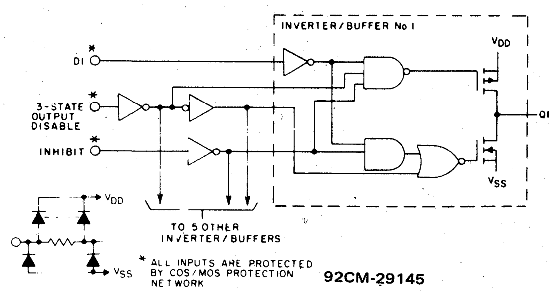
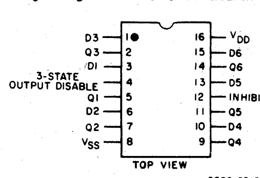


Fig. 1 – Logic diagram of 1 of 6 identical inverter/buffers.

TRUTH TABLE

DISABLE	INHIBIT	Dn	Qn
0	0	0	1
0	0	1	0
0	1	X	0
1	X	X	Z

Logic 0 = Low
Z = High Impedance
X = Don't Care
Logic 1 = High



TERMINAL ASSIGNMENT

CD4502B Types

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	3.84	3.66	2.52	2.16	3.06	6	–	mA
	0.5	0,10	10	9.6	9	6.6	5.4	7.8	15.6	–	
	1.5	0,15	15	25.2	24	16.8	14.4	20.4	40.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5, 13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	4.5	–	5	3.5				3.5	–	–	
	9	–	10	7				7	–	–	
	13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	±10⁻⁵	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	±10⁻⁴	±0.4	μA

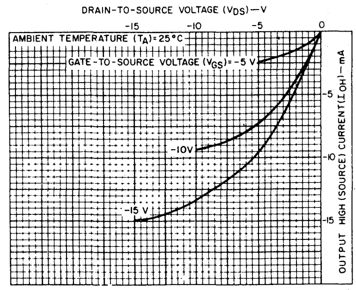


Fig.5 – Minimum output high (source) current characteristics.

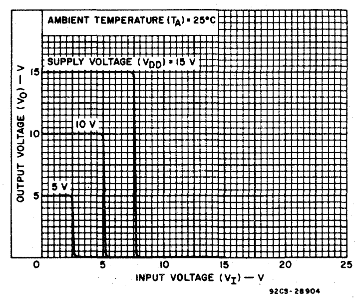


Fig.6 – Typical voltage transfer characteristics.

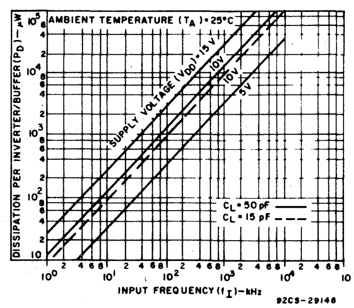


Fig.7 – Typical power dissipation as a function of input frequency.

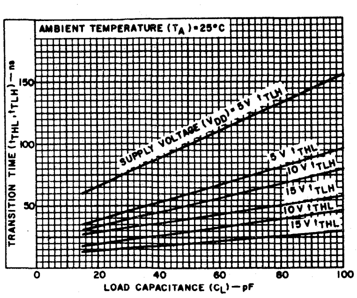


Fig.8 – Typical transition time as a function of load capacitance.

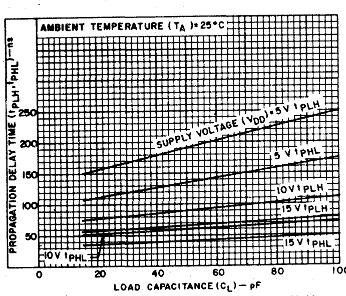


Fig.9 – Typical propagation-delay time as a function of load capacitance.

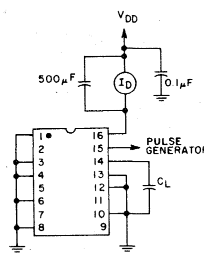


Fig. 10 – Power-dissipation test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS TYP	LIMITS MAX	UNITS
Data or Inhibit Delay Times: High to Low, t_{PHL}		5	135	270	ns
		10	60	120	
		15	40	80	
Low to High, t_{PLH}		5	190	380	
		10	90	180	
		15	65	130	
Disable Delay Times: Output High to High Impedance, t_{PHZ}	See Fig. 14	5	60	120	ns
		10	40	80	
		15	30	60	
High-Impedance to Output High, t_{PZH}		5	110	220	
		10	50	100	
		15	40	80	
Output Low to High Impedance, t_{PLZ}		5	125	250	
		10	65	130	
		15	55	110	
High Impedance to Output Low, t_{PZL}		5	125	250	
		10	55	110	
		15	40	80	
Transition Times: Low to High, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
High to Low, t_{THL}		5	60	120	
		10	30	60	
		15	20	40	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

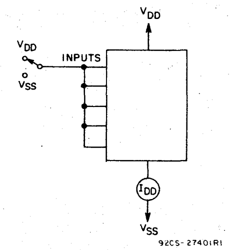


Fig. 11 — Quiescent-device-current test circuit.

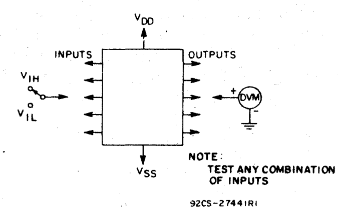


Fig. 12 — Input-voltage test circuit.

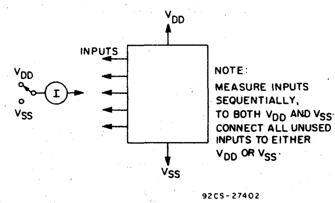
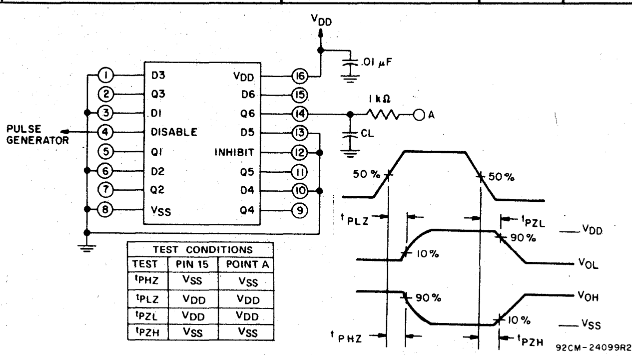


Fig. 13 — Input leakage current test circuit.

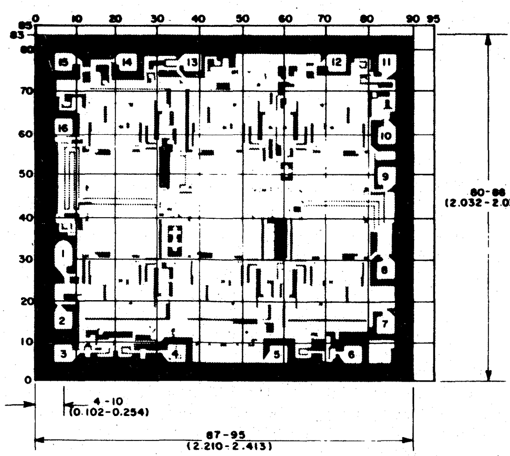


TEST CONDITIONS		
TEST	PIN 15	POINT A
t_{PHZ}	V_{SS}	V_{SS}
t_{PLZ}	V_{DD}	V_{DD}
t_{PZL}	V_{DD}	V_{DD}
t_{PZH}	V_{SS}	V_{SS}

Fig. 14 — Disable delay times test circuit and waveforms.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch.)

The photograph and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



Dimensions and Pad Layout for CD4502BH

CD4503B Types

COS/MOS Hex Buffer

High-Voltage Types (20-Volt Rating)

3-State Non-Inverting Type

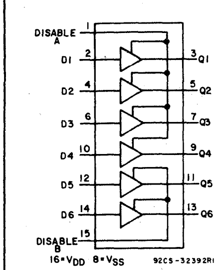
The RCA-CD4503B is a hex noninverting buffer with 3-state outputs having high sink- and source-current capability. Two disable controls are provided, one of which controls four buffers and the other controls the remaining two buffers. The CD4503B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

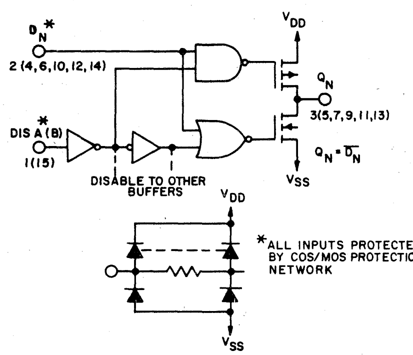
- **1 TTL-load output drive capability**
- **2 output-disable controls**
- **3-state outputs**
- **Pin compatible with industry types MM80C97, MC14503, and 340097**
- **5-V, 10-V, and 15-V parametric ratings**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **3-state hex buffer for interfacing IC's with data buses**
- **COS/MOS to TTL hex buffer**



FUNCTIONAL DIAGRAM



TRUTH TABLE

D_N	DIS A(B)	Q_N
0	0	0
1	0	1
X	1	HIGH Z

X = DON'T CARE

92CM-32393

Fig. 1—Logic diagram of 1 to 6 identical buffers.

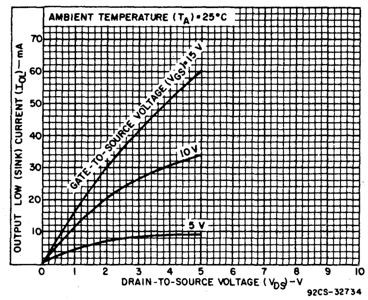


Fig. 2—Typical n-channel output low (sink) current characteristics.

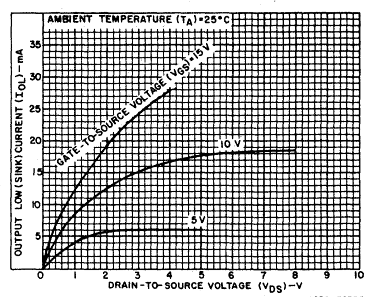
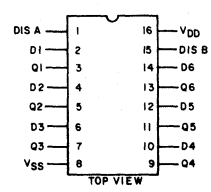


Fig. 3—Minimum n-channel output low (sink) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) .... −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT .... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) .... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TERMPERATURE RANGE (All Package Types) .... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H .... −55 to +125°C
PACKAGE TYPE E .... −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max .... +265°C



TERMINAL ASSIGNMENT

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	—	0,5	5	1	1	30	30	—	0.02	1	μA
	—	0,10	10	2	2	60	60	—	0.02	2	
	—	0,15	15	4	4	120	120	—	0.02	4	
	—	0,20	20	20	20	600	600	—	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0	5	2.6	2.5	1.4	1.3	2.1	2.3	—	mA
	0.5	0	10	6.5	6.4	3.9	3.8	5.5	6.2	—	
	1.5	0	15	19.2	18.9	11.4	11.2	16.1	23	—	
Output High (Source) Current, I_{OH} Min.	4.6	5	5	−1.2	−1.16	−0.7	−0.7	−1.02	−1.9	—	
	2.5	5	5	−5.8	−5.7	−3.4	−3	−4.8	−6.1	—	
	9.5	10	10	−3.1	−3	−1.9	−1.8	−2.6	−3.7	—	
	13.5	15	15	−8.2	−8	−4.9	−4.8	−6.8	−14.1	—	
Output Voltage: Low-Level, V_{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	—	0,5	5	4.95				4.95	5	—	
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V_{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I_{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	$\pm 10^{-5}$	±0.1	μA
3-State Output Leakage Current, I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	—	$\pm 10^{-4}$	±0.4	μA

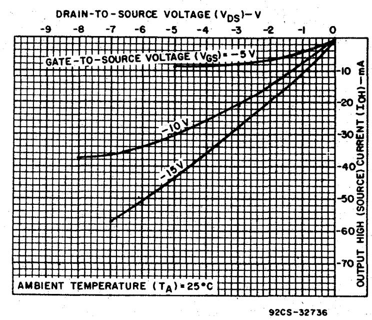


Fig. 4—Typical p-channel output high (source) current characteristics.

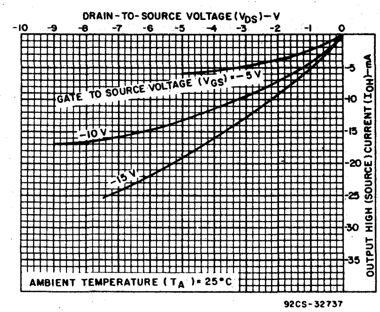


Fig. 5—Minimum p-channel output high (source) current characteristics.

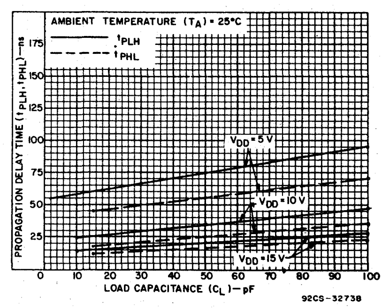


Fig. 6—Typical propagation delay time as a function of load capacitance.

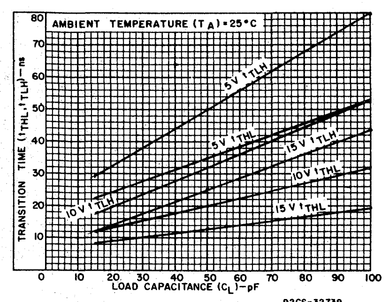


Fig. 7—Typical transition time as a function of load capacitance.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

CD4503B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ unless otherwise specified.

CHARACTERISTIC	V_{DD} (V)	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time: Low-to-High, t_{PLH}	5 10 15	75 35 25	150 70 50	ns
High-to-Low, t_{PHL}	5 10 15	55 25 17	110 50 35	ns
Transition Time: Low-to-High, t_{TLH}	5 10 15	50 30 25	90 45 35	ns
High-to-Low, t_{THL}	5 10 15	35 20 13	70 40 25	ns
3-State Propagation Delay Time: t_{PHZ}, t_{PZH}	5 10 15	70 30 25	140 60 50	ns
t_{PZL}, t_{PLZ}	5 10 15	90 40 35	180 80 70	ns

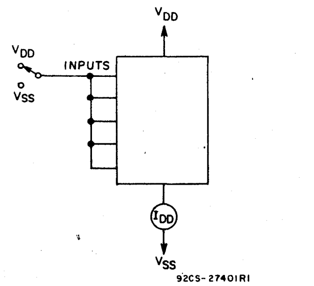


Fig. 10—Quiescent-device-current test circuit.

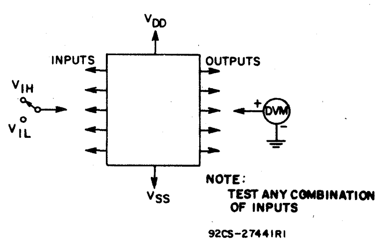


Fig. 11—Input-voltage test circuit.

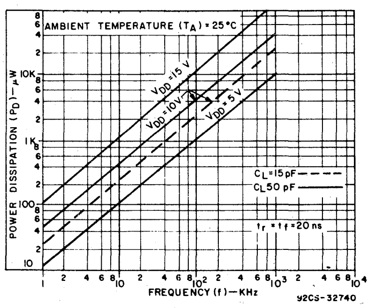


Fig. 8—Typical power dissipation as a function of frequency.

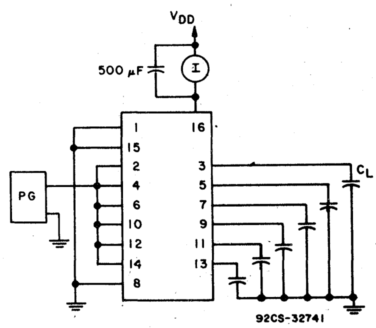


Fig. 9—Dynamic power dissipation test circuit.

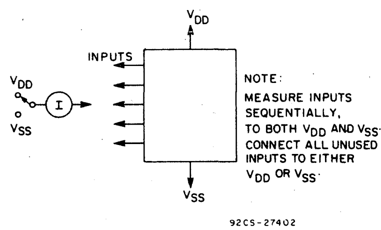
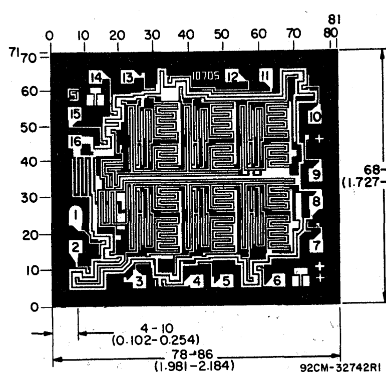


Fig. 12—Input current test circuit.



Dimensions and pad layout for CD4503BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Dual 4-Bit Latch

High-Voltage Types (20-Volt Rating)

The RCA-CD4508B dual 4-bit latch contains two identical 4-bit latches with separate STROBE, RESET, and OUTPUT DISABLE controls. With the STROBE line in the high state, the data on the "D" inputs appear at the corresponding "Q" outputs provided the DISABLE line is in the low state. Changing the STROBE line to the low state locks the data into the latch. A high on the reset line forces the outputs to a low level regardless of the state of the STROBE input. The outputs are forced to the high-impedance state for bus line applications by a high level on the DISABLE input.

The CD4508B types are supplied in the 24-lead dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

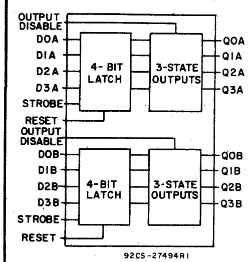
The CD4508B is similar to industry type MC14508.

Features:

- Two independent 4-bit latches
- Individual master reset for each 4-bit latch
- 3-state outputs with high-impedance state for bus line applications
- Medium-speed operation: $t_{PHL} = t_{PLH}$ = 70 ns (typ.) at V_{DD} = 10 V and C_L = 50 pF
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Buffer storage
- Holding registers
- Data storage and multiplexing



FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . −55 to +125°C
PACKAGE TYPE E . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Reset Pulse Width, $t_{W(R)}$	5	200	–	ns
	10	140	–	
	15	100	–	
Strobe Pulse Width, $t_{W(st)}$	5	140	–	
	10	80	–	
	15	70	–	
Setup Time, t_{SU}	5	50	–	
	10	30	–	
	15	20	–	
Hold Time, t_H	5	0	–	
	10	0	–	
	15	0	–	

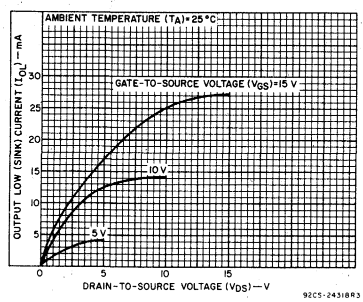


Fig.2 – Typical output low (sink) current characteristics.

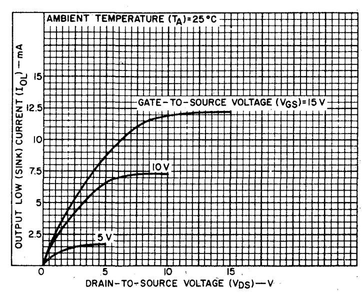


Fig.3 – Minimum output low (sink) current characteristics.

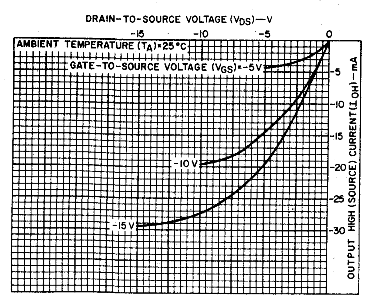
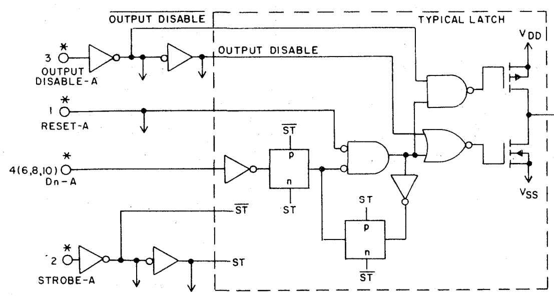
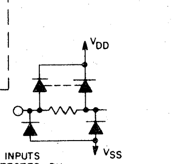


Fig.4 – Typical output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages Values at –40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm10^{-4}$	±0.4	μA





TRUTH TABLE

RESET	DISABLE	STROBE	D INPUT	Q OUTPUT
0	0	1	1	1
0	0	1	0	0
0	0	0	X	LATCHED
1	0	X	X	0
X	1	X	X	Z

1 = HIGH LEVEL   X = DON'T CARE
0 = LOW LEVEL   Z = HIGH IMPEDANCE

Fig. 7 — Logic diagram (A-Section), 1 of 4 identical latches with common output disable, reset, and strobe.

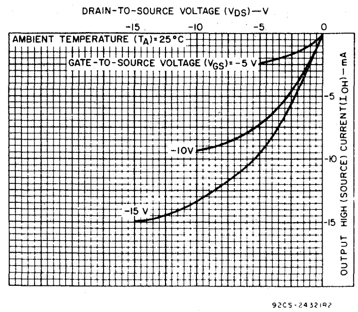


Fig. 4 — Minimum output high (source) current characteristics.

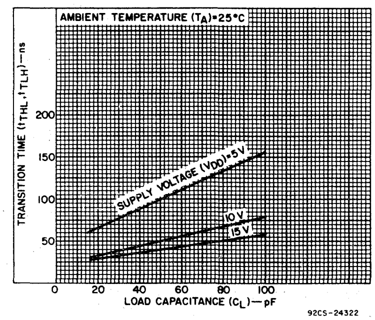


Fig. 5 — Typical transition time as a function of load capacitance.

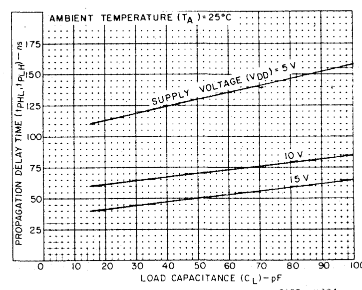


Fig. 6 — Typical propagation delay time as a function of load capacitance (strobe to data out).

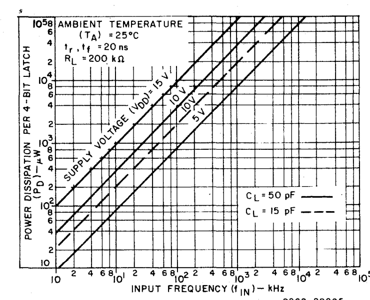


Fig. 8 — Typical power dissipation as a function of frequency.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ, unless otherwise specified.

CHARACTERISTIC	TEST CONDITIONS	VDD	LIMITS Typ.	LIMITS Max.	UNITS
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Minimum Reset Pulse Width, $t_{W(R)}$		5	100	200	
		10	70	140	
		15	50	100	
Minimum Strobe Pulse Width, $t_{W(st)}$		5	70	140	
		10	40	80	
		15	35	70	
Minimum Setup Time, t_{SU}		5	25	50	
		10	15	30	
		15	10	20	
Minimum Hold Time, t_H		5	0	0	
		10	0	0	
		15	0	0	
Propagation Delay Times: t_{PHL}, t_{PLH} Strobe to Data Out		5	130	260	
		10	70	140	
		15	50	100	
Data In to Data Out		5	105	210	
		10	60	120	
		15	45	90	
Reset to Data Out		5	90	180	
		10	50	100	
		15	40	80	
3-State Propagation Delay Times: Output High to High Impedance, t_{PHZ}		5	90	180	
		10	50	100	
		15	35	70	
High Impedance to Output High, t_{PZH}		5	90	180	
		10	50	100	
		15	35	70	
Output Low to High Impedance, t_{PLZ}		5	90	180	
		10	50	100	
		15	35	70	
High Impedance to Output Low, t_{PZL}		5	90	180	
		10	50	100	
		15	35	70	
Input Capacitance, C_{IN}	Any Input	–	5	7.5	pF

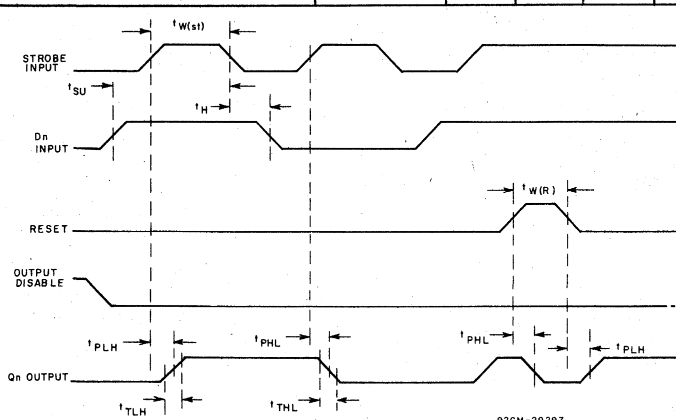


Fig. 12 — Test waveforms.

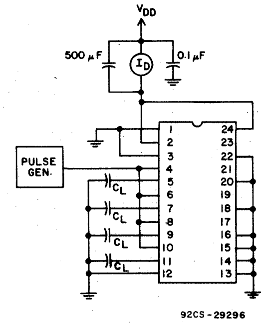


Fig.9 — Power dissipation test circuit.

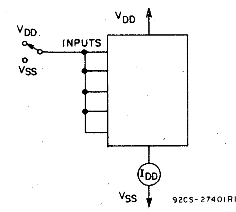


Fig. 10 — Quiescent device current test circuit.

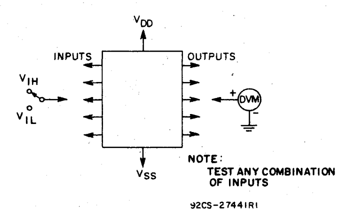


Fig. 11 — Input voltage test circuit.

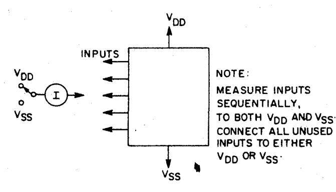
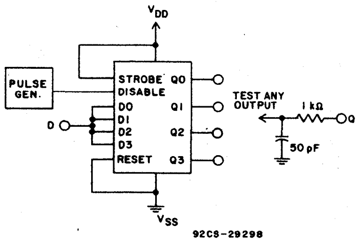
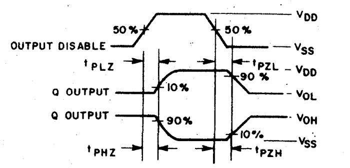


Fig. 13 — Input current test circuit.





CHAR.	TEST VOLT. AT D	AT Q
t_{PHZ}	V_{DD}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}
t_{PZL}	V_{SS}	V_{DD}
t_{PZH}	V_{DD}	V_{SS}

92CS-29299

Fig. 14 – Output disable test circuit and waveforms.

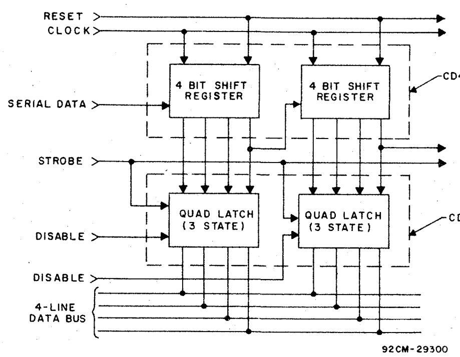
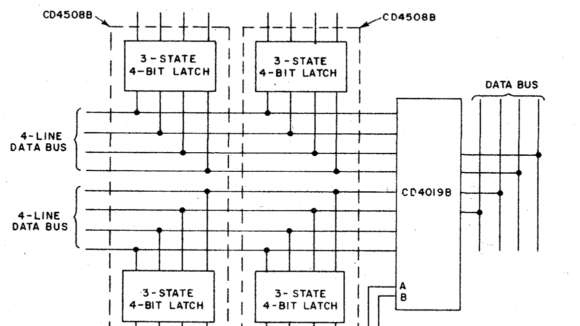


Fig. 15 – Bus register.

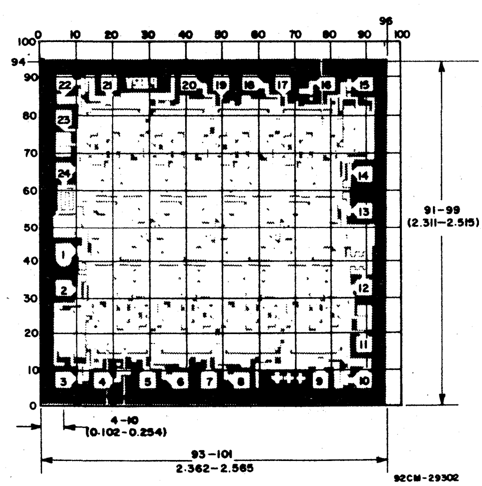


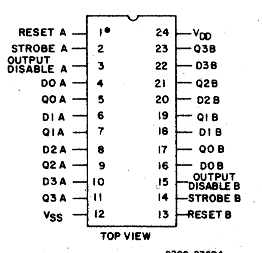
FUNCTION SELECT

A	B	Function
0	0	Inhibit (all 0)
1	0	Select A Bus
0	1	Select B Bus
1	1	$A_I + B_I$

92CM-29301

Fig. 16 – Dual multiplexed bus register with function select.





TERMINAL ASSIGNMENT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for CD4508B.

COS/MOS Presettable Up/Down Counters

High-Voltage Types (20-Volt Rating)

CD4510B – – – BCD Type

CD4516B – – – Binary Type

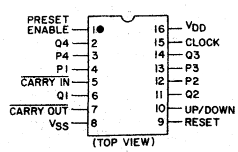
The RCA-CD4510B Presettable BCD Up/Down Counter and the CD4516 Presettable Binary Up/Down Counter consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. These counters can be cleared by a high level on the RESET line, and can be preset to any binary number present on the jam inputs by a high level on the PRESET ENABLE line. The CD4510B will count out of non-BCD counter states in a maximum of two clock pulses in the up mode, and a maximum of four clock pulses in the down mode.

If the CARRY-IN input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY-OUT of a less significant stage to the CARRY-IN of a more significant stage.

The CD4510B and CD4516B can be cascaded in the ripple mode by connecting the CARRY-OUT to the clock of the next stage. If the UP/DOWN input changes during a terminal count, the CARRY-OUT must be gated with the clock, and the UP/DOWN input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage. (See Fig. 15).

These devices are similar to types MC14510 and MC14516.

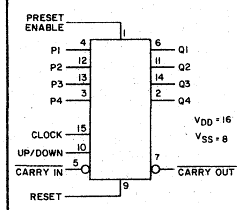
The CD4510B and CD4516B Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (k suffix), and in chip form (H suffix).



CD4510B, CD4516B TERMINAL ASSIGNMENT

Features:

- **Medium-speed operation -- f_{CL} = 8 MHz typ. at 10 V**
- **Synchronous internal carry propagation**
- **Reset and Preset capability**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized symmetrical output characteristics**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



CD4510B, CD4516B FUNCTIONAL DIAGRAM
92CS-24824

Applications:

- **Up/Down difference counting**
- **Multistage synchronous counting**
- **Multistage ripple counting**
- **Synchronous frequency dividers**

OPERATING CONDITIONS AT T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units
Supply Voltage Range (At T_A = Full Package-Temperature Range)		3	18	V
Clock Pulse Width, t_W	5 10 15	150 75 60	– – –	ns
Clock Input Frequency, f_{CL}	5 10 15	– – –	2 4 5.5	MHz
Preset Enable or Reset Removal Time●	5 10 15	150 80 60	– – –	ns
Clock Rise and Fall Time, t_rCL, t_fCL *	5 10 15	– – –	15 5 5	μs
Carry-In Setup Time, t_S	5 10 15	130 60 45	– – –	ns
Up-Down Setup Time, t_S	5 10 15	360 160 110	– – –	ns
Preset Enable or Reset Pulse Width, t_W	5 10 15	220 100 75	– – –	ns

●Time required after the falling edge of the reset or preset enable inputs before the rising edge of the clock will trigger the counter (similar to setup time).

*If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

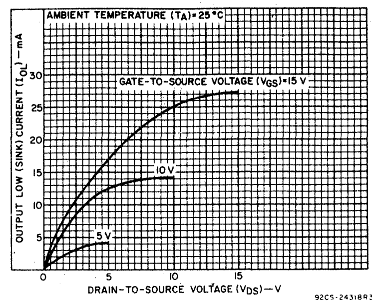


Fig.1 – Typical output low (sink) current characteristics.

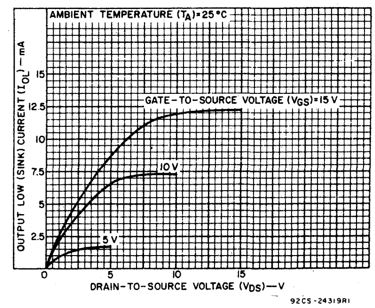


Fig.2 – Minimum output low (sink) current characteristics.

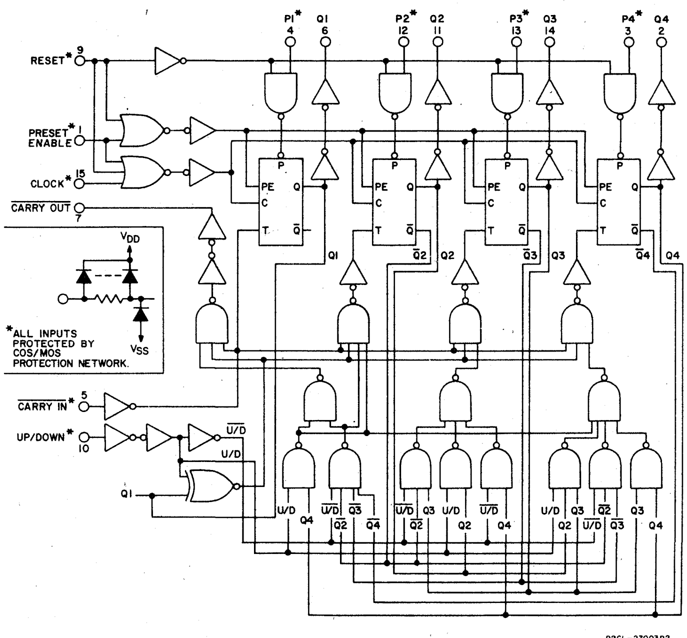


Fig.3 – Logic Diagram for CD4510B.

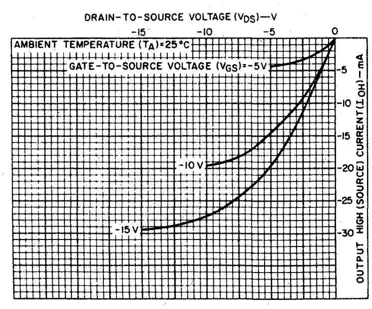


Fig.4 – Typical output high (source) current characteristics.

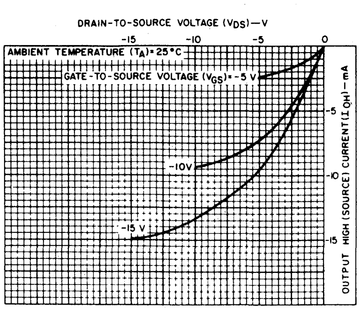


Fig.5 – Minimum output high (source) current characteristics.

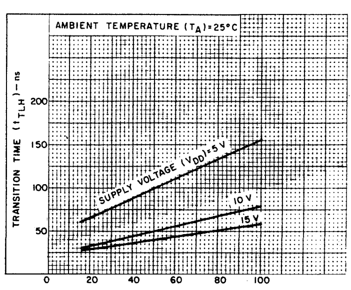


Fig.6 – Typical transition time vs. load capacitance.

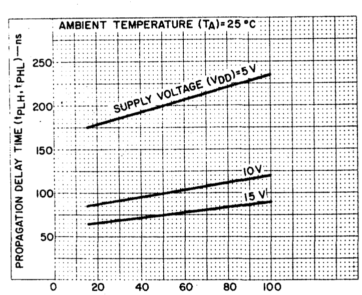


Fig.7 – Typical propagation delay time vs. load capacitance for clock-to-Q outputs.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages; Values at –40, +25, +85 Apply to E Package: –55	–40	+85	+125	+25 Min.	Typ.	Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	±10⁻⁵	±0.1	μA

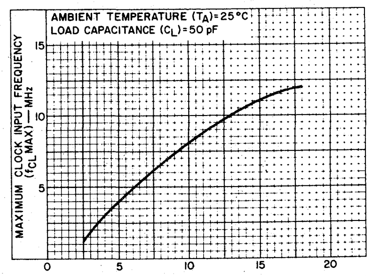


Fig.8 – Typical maximum clock input frequency vs. supply voltage.

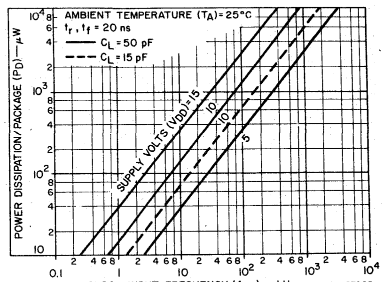


Fig.9 – Typical dynamic power dissipation vs. frequency.

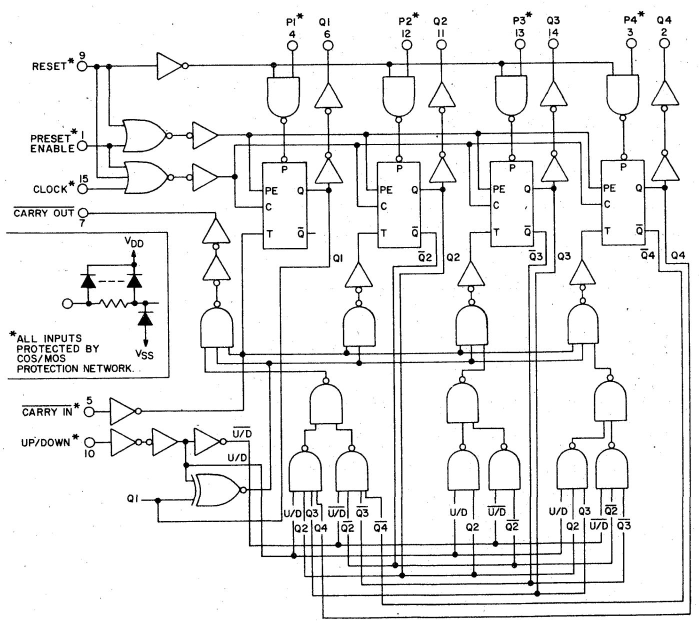


Fig.10 – Logic Diagram for CD4516B.

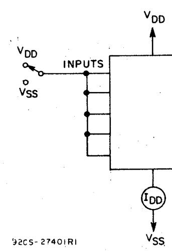


Fig. 11 – Quiescent-device-current test circuit.

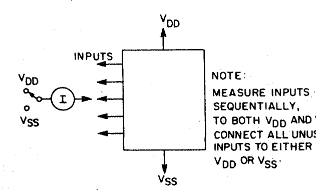


Fig. 12 – Input-current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 50 pF, Input t_r, t_f = 20 ns, R_L = 200 kΩ

Characteristic	Conditions V_{DD} (V)	Limits All Packages Min.	Typ.	Max.	Units
Propagation Delay Time (t_{PHL}, t_{PLH}): Clock-to-Q Output (See Fig. 10)	5	–	200	400	ns
	10	–	100	200	
	15	–	75	150	
Preset or Reset-to-Q Output	5	–	210	420	ns
	10	–	105	210	
	15	–	80	160	
Clock-to-Carry Out	5	–	240	480	ns
	10	–	120	240	
	15	–	90	180	
Carry-In-to-Carry Out	5	–	125	250	ns
	10	–	60	120	
	15	–	50	100	
Preset or Reset-to-Carry Out	5	–	320	640	ns
	10	–	160	320	
	15	–	125	250	
Transition Time (t_{THL}, t_{TLH}) (See Fig. 9)	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Max. Clock Input Frequency (f_{CL})	5	2	4	–	MHz
	10	4	8	–	
	15	5.5	11	–	
Input Capacitance (C_{IN})		–	5	7.5	pF

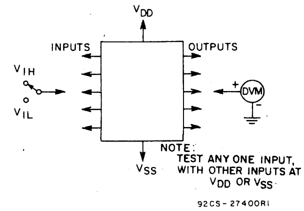


Fig. 13 – Input-voltage test circuit.

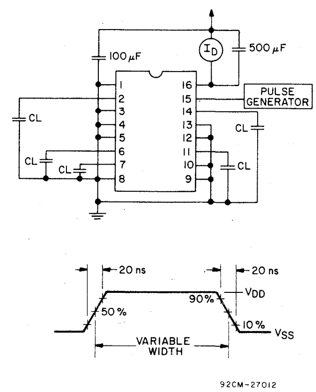


Fig. 14 – Power-dissipation test circuit and input waveform.

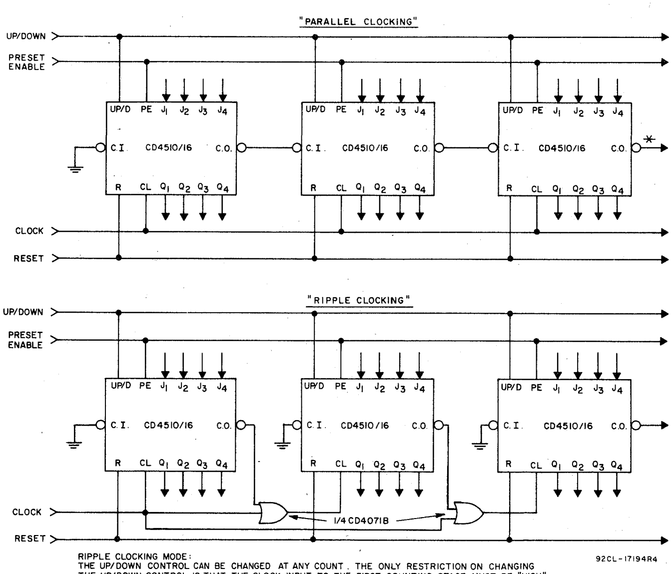


Fig. 15 – Cascading counter packages.

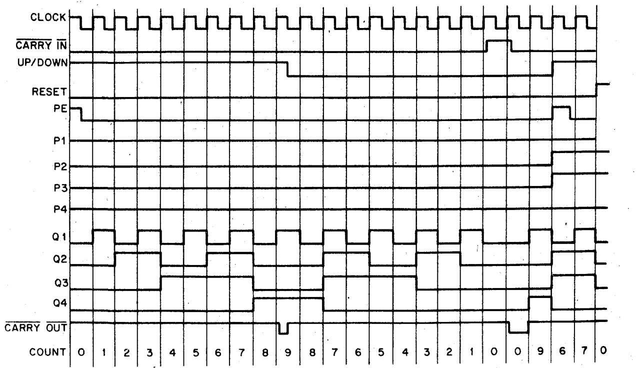


Fig. 16 – Timing Diagram for CD4510B.

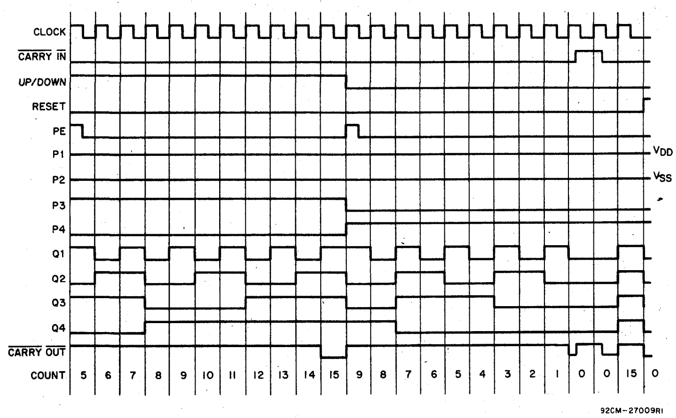
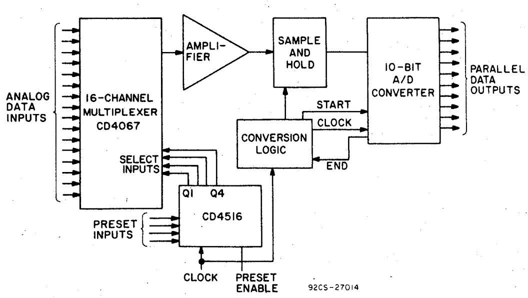


Fig. 17 – Timing diagram for CD4516B.



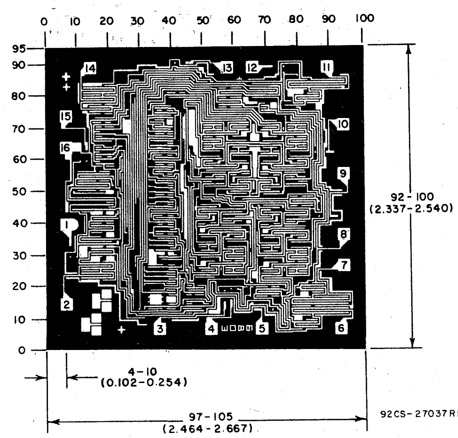
This acquisition system can be operated in the random access mode by jamming in the channel number at the present inputs, or in the sequential mode by clocking the CD4516B.

Fig. 18 – Typical 16-channel, 10-bit data aquisition system.

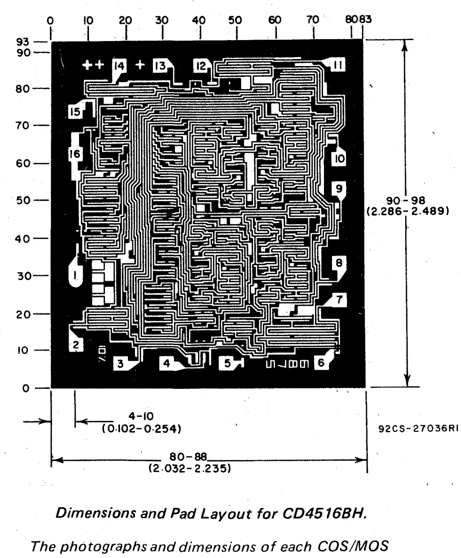
CL	$\overline{CI}$	U/D	PE	R	ACTION
X	1	X	0	0	NO COUNT
⎍	0	1	0	0	COUNT UP
⎍	0	0	0	0	COUNT DOWN
X	X	X	1	0	PRESET
X	X	X	X	1	RESET

X = DON'T CARE

TRUTH TABLE



Dimensions and Pad Layout for CD4510BH.



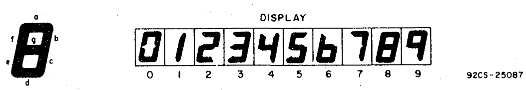
Dimensions and Pad Layout for CD4516BH.

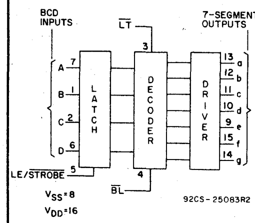
The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

COS/MOS BCD-to-7-Segment Latch Decoder Drivers

High-Voltage Types (20-Volt Rating)



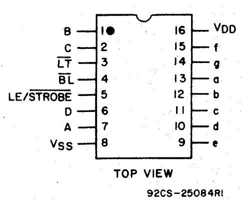


FUNCTIONAL DIAGRAM

The CD4511B types are BCD-to-7-segment latch decoder drivers constructed with COS/MOS logic and n-p-n bipolar transistor output devices on a single monolithic structure. These devices combine the low quiescent power dissipation and high noise immunity features of RCA COS/MOS with n-p-n bipolar output transistors capable of sourcing up to 25 mA. This capability allows the CD4511B types to drive LED's and other displays directly.

Lamp Test ($\overline{LT}$), Blanking ($\overline{BL}$), and Latch Enable or Strobe inputs are provided to test the display, shut off or intensity-modulate it, and store or strobe a BCD code, respectively. Several different signals may be multiplexed and displayed when external multiplexing circuitry is used. The CD4511B is supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

These devices are similar to the type MC14511.



CD4511B
TERMINAL ASSIGNMENT

Features:

- **High-output-sourcing capability . . . . up to 25 mA**
- **Input latches for BCD Code storage**
- **Lamp Test and Blanking capability**
- **7-segment outputs blanked for BCD input codes > 1001**
- **100% tested for quiescent current at 20 V**
- **Max. input current of 1 µA at 18 V, over full package-temperature range, 100 nA at 18 V and 25°C**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

- **Driving common-cathode LED displays**
- **Multiplexing with common-cathode LED displays**
- **Driving incandescent displays**
- **Driving low-voltage fluorescent displays**

MAXIMUM RATINGS, ***Absolute-Maximum Values:***

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

OPERATING CONDITIONS AT T_A = 25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

Characteristic	V_{DD}	Min.	Max.	Units
Supply-Voltage Range (T_A): (Full Package-Temperature Range)	–	3	18	V
Set-Up Time (t_S)	5	150	–	ns
	10	70	–	ns
	15	40	–	ns
Hold Time (t_H)	5	0	–	ns
	10	0	–	ns
	15	0	–	ns
Strobe Pulse Width (t_W)	5	400	–	ns
	10	160	–	ns
	15	100	–	ns

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions				Limits at Indicated Temperatures (°C) Values at –55, +25, +125 for D, F, H Packages; Values at –40, +25, +85 for E Packages							Units
	I_{OH} (mA)	V_o (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current: I_{DD} Max.	–	–	–	5	5	5	150	150	–	0.04	5	μA
	–	–	–	10	10	10	300	300	–	0.04	10	
	–	–	–	15	20	20	600	600	–	0.04	20	
	–	–	–	20	100	100	3000	3000	–	0.08	100	
Output Voltage: Low-Level V_{OL} Max.	–	–	0,5	5	0.05				–	0	0.05	V
	–	–	0,10	10	0.05				–	0	0.05	
	–	–	0,15	15	0.05				–	0	0.05	
High-Level V_{OH} Min.	–	–	0,5	5	4	4	4.2	4.2	4.1	4.55	–	V
	–	–	0,10	10	9	9	9.2	9.2	9.1	9.55	–	
	–	–	0.15	15	14	14	14.2	14.2	14.1	14.55	–	
Input Low Voltage, V_{IL} Max.	–	0.5,3.8		5	1.5				–	–	1.5	V
	–	1,8.8	–	10	3				–	–	3	
	–	1.5,13.8		15	4				–	–	4	
Input High Voltage, V_{IH} Min.	–	0.5,3.8		5	3.5				3.5	–	–	V
	–	1,8.8		10	7				7	–	–	
	–	1.5,13.8		15	11				11	–	–	
Output Drive Voltage: High Level V_{OH} Min.	0			5	4.0	4.0	4.20	4.20	4.10	4.55	–	V
	5						–	–	–	4.25	–	
	10				3.80	3.80	3.90	3.90	3.90	4.10	–	
	15						3.50	3.50	–	3.95	–	
	20				3.55	3.55	–	–	3.40	3.75	–	
	25				3.40	3.40	–	–	3.10	3.55	–	
	0			10	9.0	9.0	9.20	9.20	9.10	9.55	–	V
	5						–	–	–	9.25	–	
	10	–	–		8.85	8.85	9.00	9.00	9.00	9.15	–	
	15	–	–		–	–	–	–	–	9.05	–	
	20	–	–		8.70	8.70	8.40	8.40	8.60	8.90	–	
	25	–	–		8.60	8.60	–	–	8.30	8.75	–	
	0	–	–	15	14.0	14.0	14.20	14.20	14.10	14.55	–	V
	5	–	–		–	–	–	–	–	14.30	–	
	10	–	–		13.90	13.90	14.0	14.0	14.0	14.20	–	
	15	–	–		–	–	–	–	–	14.10	–	
	20	–	–		13.75	13.75	13.50	13.50	13.70	13.95	–	
	25	–	–		13.65	13.65	–	–	13.50	13.80	–	
Output Low (Sink) Current, I_{OL} Min.	–	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	–	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	–	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Input Current, I_{IN} Max.	–	0,18	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

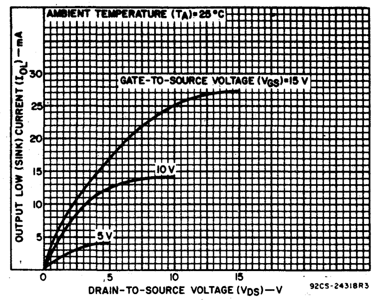


Fig. 1 – Typical output low (sink) current characteristics.

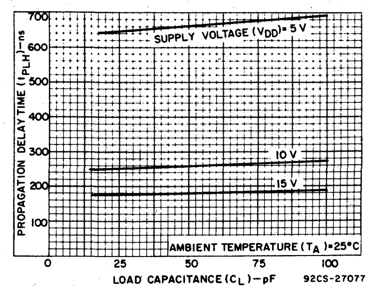


Fig. 2 – Typical data-to-output, low-to-high-level propagation delay time as a function of load capacitance.

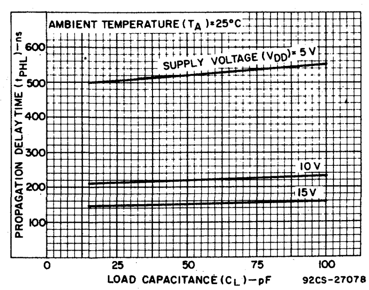


Fig. 3 – Typical data-to-output, high-to-low-level propagation delay time as a function of load capacitance.

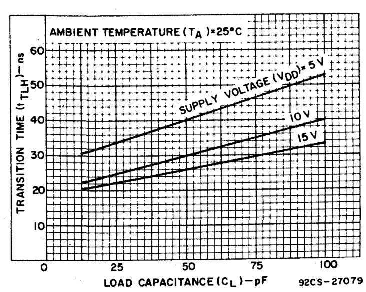


Fig. 4 – Typical low-to-high-level transition time as a function of load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	Test Conditions V_{DD} Volts	LIMITS All Packages Min.	Typ.	Max.	UNITS
Propagation Delay Time: (Data) High-to-Low Level, t_{PHL}	5	–	520	1040	ns
	10	–	210	420	
	15	–	150	300	
Low-to-High Level, t_{PLH}	5	–	660	1320	ns
	10	–	260	520	
	15	–	180	360	
Propagation Delay Time: ($\overline{BL}$) High-to-Low Level, t_{PHL}	5	–	350	700	ns
	10	–	175	350	
	15	–	125	250	
Low-to-High Level, t_{PLH}	5	–	400	800	ns
	10	–	175	350	
	15	–	150	300	
Propagation Delay Time: ($\overline{LT}$) High-to-Low Level, t_{PHL}	5	–	250	500	ns
	10	–	125	250	
	15	–	85	170	
Low-to-High Level, t_{PLH}	5	–	150	300	ns
	10	–	75	150	
	15	–	50	100	
Transition Time: Low-to-High Level, t_{TLH}	5	–	40	80	ns
	10	–	30	60	
	15	–	25	50	
High-to-Low Level, t_{THL}	5	–	125	310	ns
	10	–	75	185	
	15	–	65	160	
Minimum Set-Up Time, t_S	5	150	75	–	ns
	10	70	35	–	
	15	40	20	–	
Minimum Hold Time, t_H	5	0	–75	–	ns
	10	0	–35	–	
	15	0	–20	–	
Strobe Pulse Width, t_W	5	400	200	–	ns
	10	160	80	–	
	15	100	50		
Input Capacitance, C_{IN}		–	5	7.5	pF

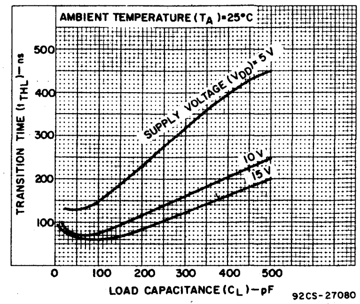


Fig. 5 — Typical high-to-low transition time as a function of load capacitance.

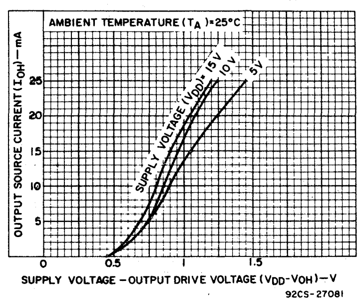


Fig. 6 — Typical voltage drop (V_{DD} to output) vs. output source current as a function of supply.

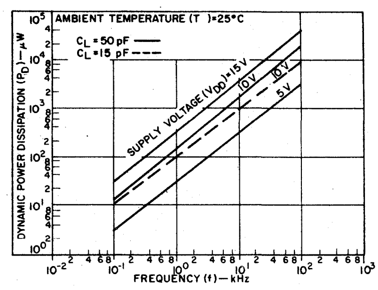


Fig. 7 — Typical dynamic power dissipation characteristics.

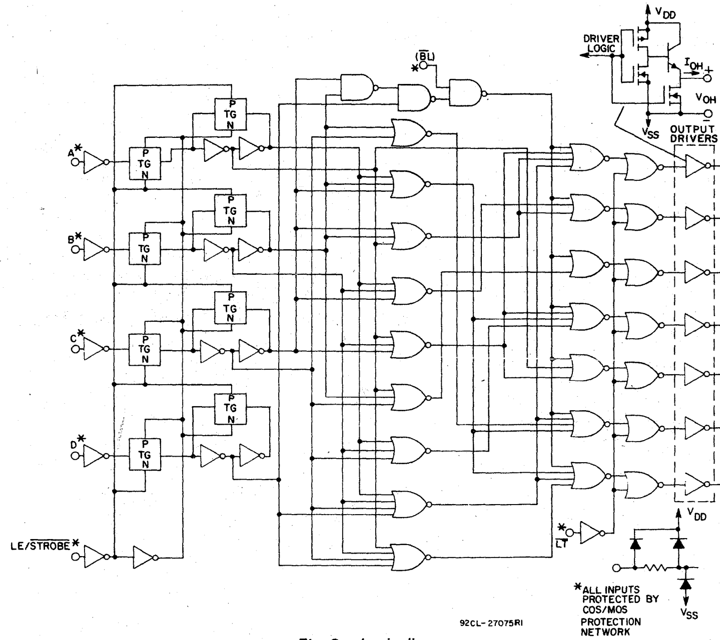


Fig. 8 – Logic diagram.

TRUTH TABLE

LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X	*							*

X ≡ Don't Care * Depends on BCD code previously applied when LE = 0

Note: Display is blank for all illegal input codes (BCD > 1001).

TEST CIRCUITS

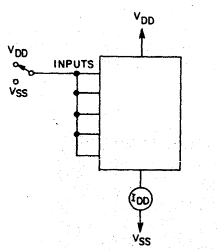


Fig. 9 – Quiescent device current.

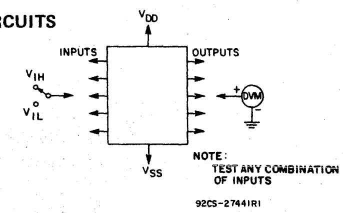
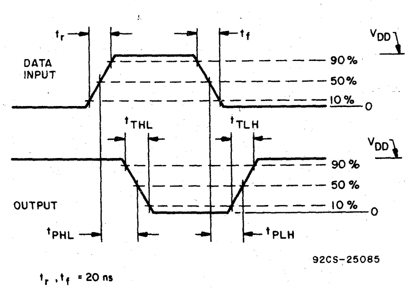


Fig. 10 – Input voltage.



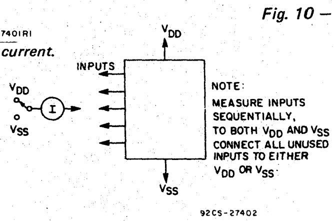


Fig. 11 – Input current.

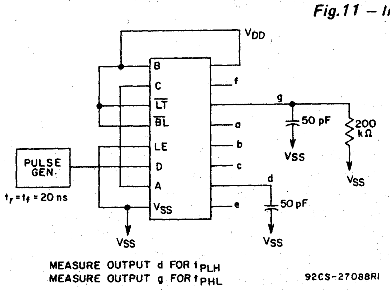


Fig. 12 – Data propagation delay.

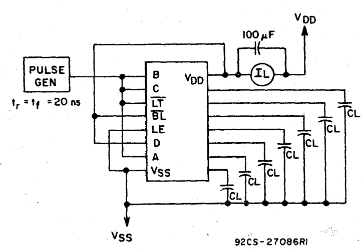


Fig. 13 – Dynamic power dissipation.

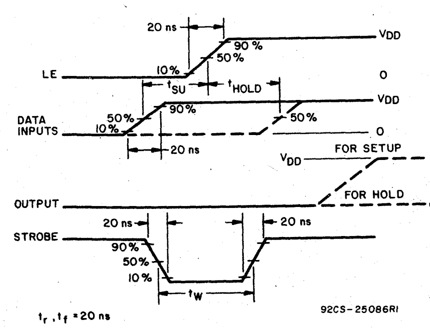
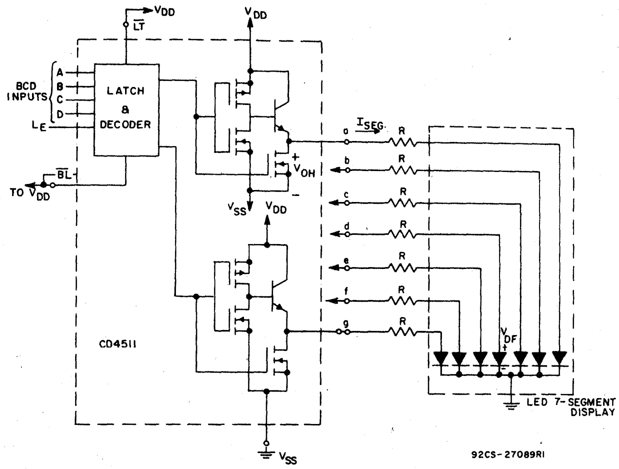


Fig. 14 – Dynamic waveforms.

APPLICATIONS

Interfacing with Various Displays

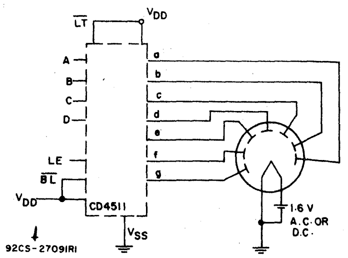


Duty Cycle = 100%

$I_{SEG} = I_{DIODE_{AVG.}}$ = 20 mA at Luminous Intensity/Segment = 250 microcandles

$$R = \frac{V_{OH} - V_{DF}}{I_{SEG}}$$

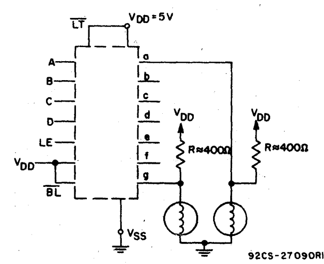
Fig. 15 – Driving common-cathode 7-segment LED displays (example Hewlet-Packard 5082-7740).



A medium-brightness intensity display can be obtained with low-voltage fluorescent displays such as the Tung-Sol Digivac S/G** Series.

**Trademark Tung-Sol Division Wagner Electric Co.

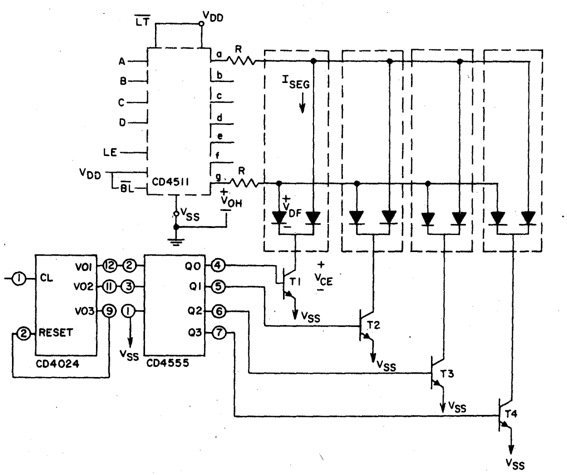
Fig. 16 – Driving low-voltage fluorescent displays.



2 of 7 Segments Shown Connected

Resistors R from V_{DD} to each 7-segment driver output are chosen to keep all Numitron segments slightly on and warm.

Fig. 17 – Driving incandescent displays (RCA Numitron DR2000 series displays).



Multiplexing Scheme Showing 2 of 7 Segments Connected

Transistors T_1–T_4 (RCA-2N3053 or 2N2102) have I_C Max. rating $> 7 \times I_{SEG}$

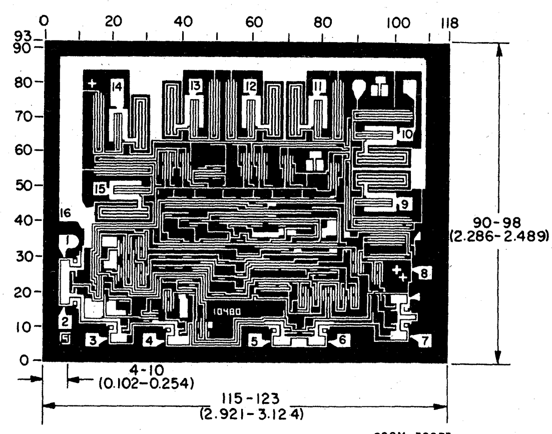
Duty Cycle = 25%

$I_{SEG} = [I_{DIODE_{AVG}}] \times 4$

$$R = \frac{(V_{OH} - V_{DF} - V_{CE})}{I_{SEG}}$$

All unused inputs on CD4555 are connected to V_{DD} or V_{SS}.

Fig. 18 – Multiplexing with common-cathode 7-segment LED displays (example Hewlet-Packard 5082-7404 4 character display or 4 discrete Monosanto Man 3 displays).



Dimensions and pad layout for CD4511B chip.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

COS/MOS 8-Channel Data Selector

High-Voltage Types (20-Volt Rating)

The RCA-CD4512B is an 8-channel data selector featuring a three-state output that can interface directly with, and drive, data lines of bus-oriented systems.

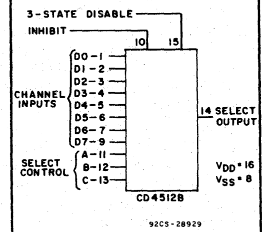
The CD4512B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

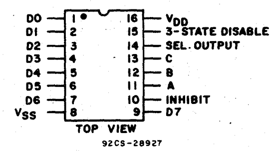
- 3-state output
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Digital multiplexing
- Number-sequence generation
- Signal gating



FUNCTIONAL DIAGRAM



TERMINAL ASSIGNMENT

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

TRUTH TABLE

SEL. CONT.			INH	3-STATE DISABLE	SEL OUTPUT
A	B	C			
0	0	0	0	0	D0
1	0	0	0	0	D1
0	1	0	0	0	D2
1	1	0	0	0	D3
0	0	1	0	0	D4
1	0	1	0	0	D5
0	1	1	0	0	D6
1	1	1	0	0	D7
X	X	X	1	0	0
X	X	X	X	1	High Z

1 = High Level 0 = Low Level
X = Don't Care

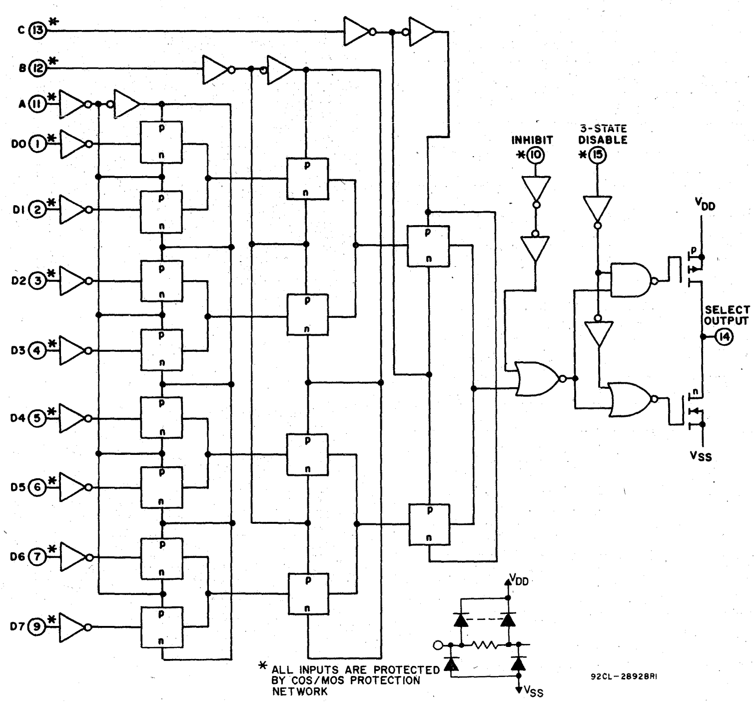


Fig. 1 – Logic diagram.

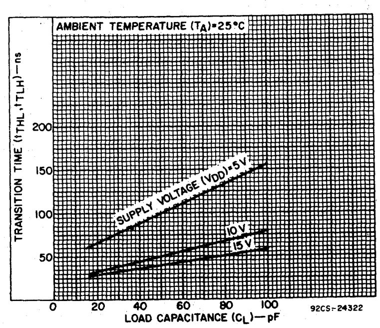


Fig. 2 – Typical transition time as a function of load capacitance.

CD4512B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

STATIC ELECTRICAL CHARACTERISTICS

CHARAC-TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	µA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	µA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm10^{-4}$	±0.4	µA

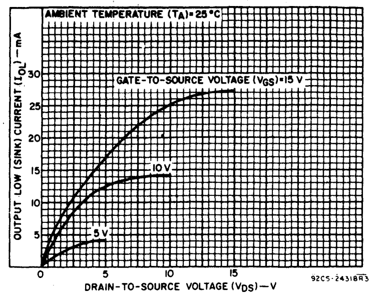


Fig. 3 – Typical output low (sink) current characteristics.

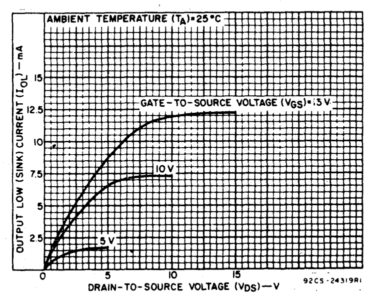


Fig. 4 – Minimum output low (sink) current characteristics.

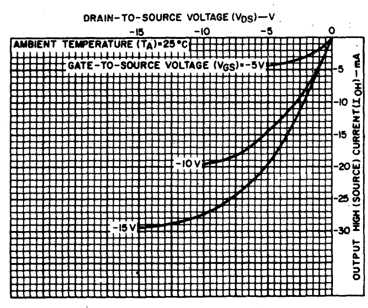


Fig. 5 – Typical output high (source) current characteristics.

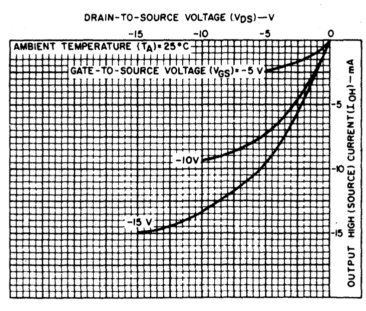


Fig. 6 – Minimum output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH} Inhibit to Output	5	140	280	ns
	10	70	140	
	15	50	100	
"A" Select to Output	5	200	400	
	10	85	170	
	15	60	120	
Data to Output	5	180	360	
	10	75	150	
	15	55	110	
3-State Disable Delay Time: t_{PZL}, t_{PLZ}, t_{PHZ}, t_{PZH}	5	60	120	ns
	10	30	60	
	15	20	40	
Transition Time, t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN} (Any Input)		5	7.5	pF

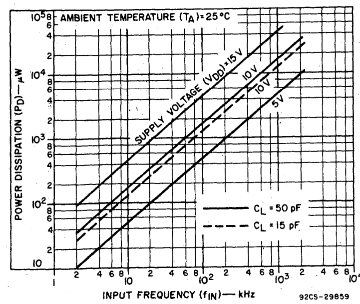


Fig. 7 – Typical dyanamic power dissipation as a function of frequency.

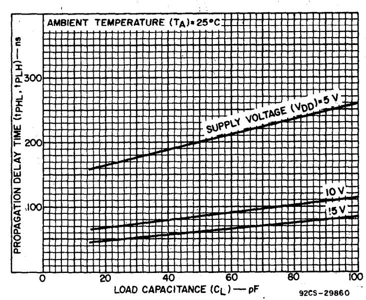


Fig. 8 – Typical propagation delay time as a function of load capacitance ("A" select to output).

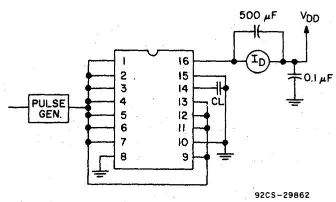


Fig. 9 – Dynamic power dissipation test circuit.

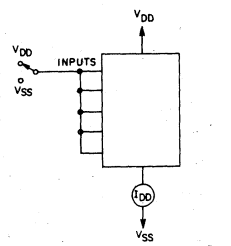


Fig. 10 – Quiescent device current test circuit.

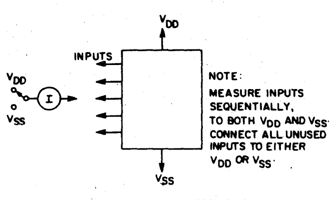


Fig. 11 – Input current test circuit.

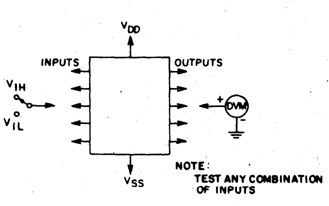
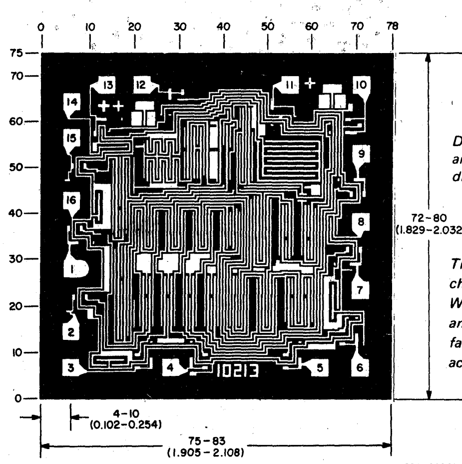


Fig. 12 – Input voltage test circuit.



Dimensions and pad layout for CD4512BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4514B, CD4515B Types

COS/MOS 4-Bit Latch/4-to-16 Line Decoders

High-Voltage Types (20-Volt Rating)
CD4514B Output "High" on Select
CD4515B Output "Low" on Select

The RCA-CD4514B and -CD4515B consist of a 4-bit strobed latch and a 4-to-16-line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 0(CD4514B) or 1(CD4515B) regardless of the state of the data or strobe inputs.

The decode truth table indicates all combinations of data inputs and appropriate selected outputs.

These devices are similar to industry types MC14514 and MC14515.

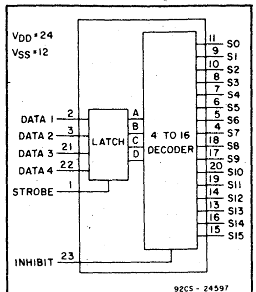
The CD4514B and CD4515B types are supplied in 24-lead hermetic dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Strobed input latch**
- **Inhibit control**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package temperature range):**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics.**
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- **Digital multiplexing**
- **Address decoding**
- **Hexadecimal/BCD decoding**
- **Program-counter decoding**
- **Control decoder**



CD4514B, CD4515B FUNCTIONAL DIAGRAM

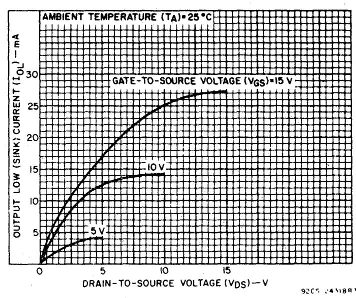


Fig. 1 — Typical output low (sink) current characteristics.

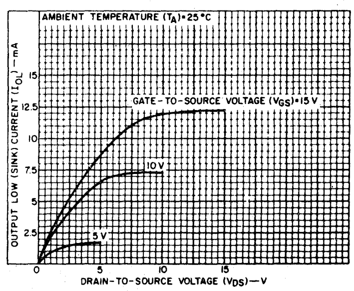


Fig. 2 — Minimum output low (sink) current characteristics.

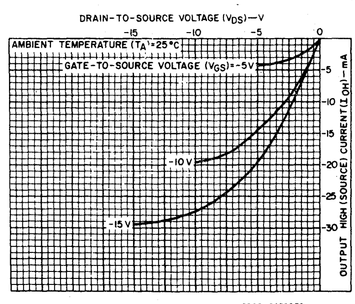


Fig. 3 — Typical output high (source) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . −55 to +125°C
PACKAGE TYPE E . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5 10 15	150 70 40	– – –	ns
Strobe Pulse Width, t_W	5 10 15	250 100 75	– – –	ns

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

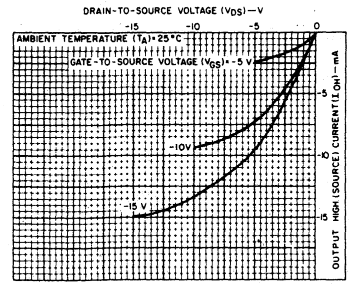


Fig. 4 — Minimum output high (source) current characteristics.

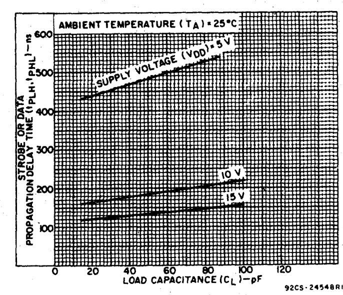


Fig. 5 — Typical strobe or data propagation delay time vs. load capacitance.

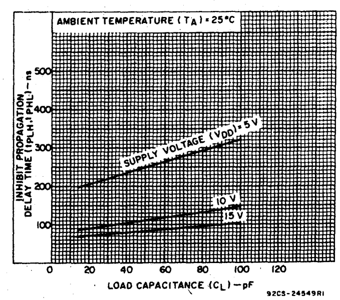


Fig. 6 — Typical inhibit propagation delay time vs. load capacitance.

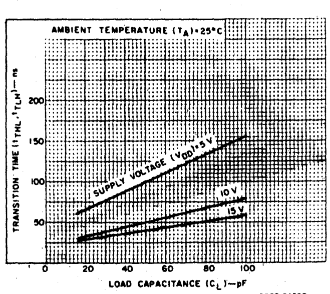


Fig. 7 — Typical low-to-high transition time vs. load capacitance.

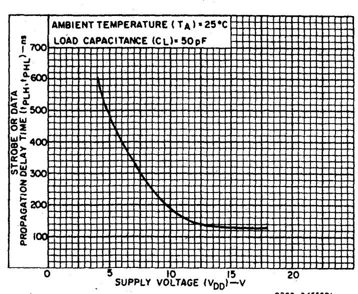


Fig. 8 — Typical strobe or data propagation delay time vs. supply voltage.

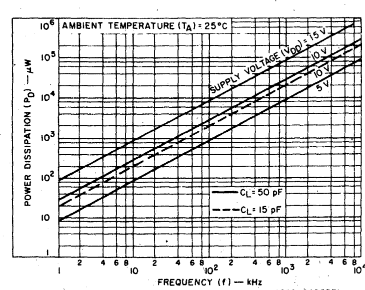


Fig. 9 — Typical power dissipation vs. frequency.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
		V_{DD} V	Typ.	Max.	
Propagation Delay Time: t_{PHL}, t_{PLH} Strobe or Data		5	485	970	ns
		10	185	370	
		15	135	270	
Inhibit		5	250	500	
		10	110	220	
		15	85	170	
Transition Time, t_{TLH}, t_{THL}		5	100	200	
		10	50	100	
		15	40	80	
Minimum Strobe Pulse Width, t_W		5	125	250	ns
		10	50	100	
		15	40	75	
Minimum Data Setup Time, t_S		5	75	150	ns
		10	35	70	
		15	20	40	
Input Capacitance, C_{IN}	Any Input	–	5	7.5	pF

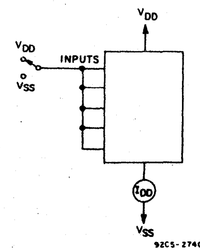


Fig. 10 — Quiescent device current test circuit.

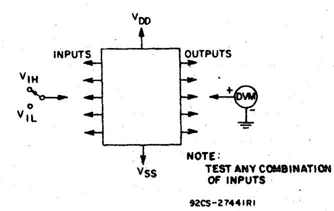


Fig. 11 — Input voltage test circuit.

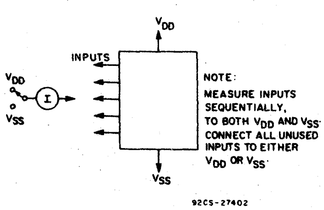


Fig. 12 — Input current test circuit.

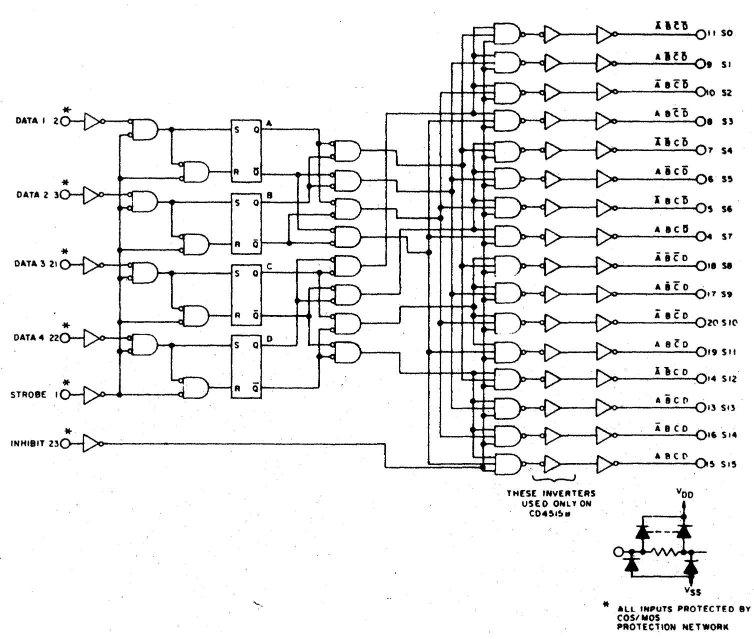


Fig. 13 — Logic diagram for CD4514B and CD4515B.

DECODE TRUTH TABLE (Strobe = 1)

INHIBIT	DECODER INPUTS D	C	B	A	SELECTED OUTPUT CD4514B = Logic 1 (High) CD4515B = Logic 0 (Low)
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD4514B All Outputs = 1, CD4515B

X = Don't Care Logic 1 = high Logic 0 = low

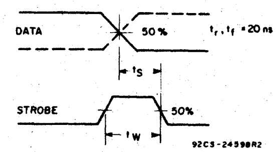
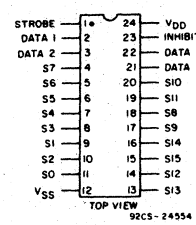
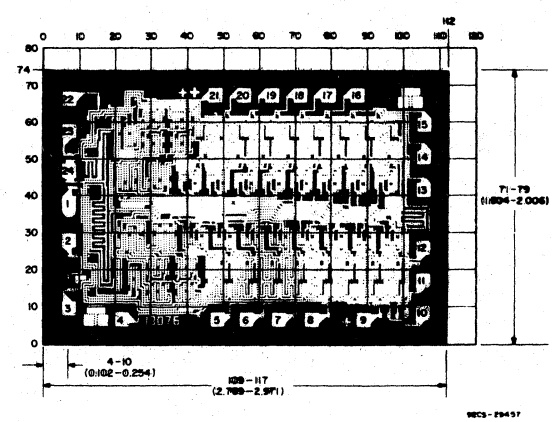


Fig. 14 — Waveforms for setup time and strobe pulse width.



CD4514B
CD4515B
TERMINAL ASSIGNMENT



Dimensions and Pad Layout for CD4515B Chip
(Dimensions and pad layout for the CD4514B are identical)

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4517B Types

COS/MOS Dual 64-Stage Static Shift Register

High-Voltage Types (20-Volt Rating)

The RCA-CD4517B dual 64-stage static shift register consists of two independent registers each having a clock, data, and write enable input and outputs accessible at taps following the 16th, 32nd, 48th, and 64th stages. These taps also serve as input points allowing data to be inputted at the 17th, 33rd, and 49th stages when the write enable input is a logic 1 and the clock goes through a low-to-high transition. The truth table indicates how the clock and write enable inputs control the operation of the CD4517B. Inputs at the intermediate taps allow entry of 64 bits into the register with 16 clock pulses. The 3-state outputs permit connection of this device to an external bus.

The CD4517B is supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

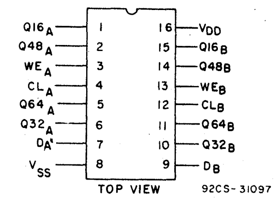
Features:

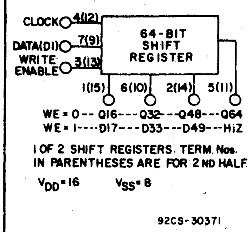
- **Low quiescent current — 10 nA/pkg (typ.) at V_{DD} = 5 V**
- **Clock frequency 12 MHz (typ.) at V_{DD} = 10 V**
- **Schmitt trigger clock inputs allow operation with very slow clock rise and fall times**
- **Capable of driving two low-power TTL loads, one low- power Schottky TTL load, or two HTL loads**
- **Three-state outputs**
- **100% tested for quiescent current at 20 V**
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Time-delay circuits**
- **Scratch-pad memories**
- **General-purpose serial shift-register applications**

TERMINAL ASSIGNMENT





TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

TRUTH TABLE

Clock	Write Enable	Data	Stage 16 Tap	Stage 32 Tap	Stage 48 Tap	Stage 64 Tap
0	0	X	Q16	Q32	Q48	Q64
0	1	X	Z	Z	Z	Z
1	0	X	Q16	Q32	Q48	Q64
1	1	X	Z	Z	Z	Z
↑	0	DI In	Q16	Q32	Q48	Q64
↑	1	DI In	D17 In	D33 In	D49 In	Z
↓	0	X	Q16	Q32	Q48	Q64
↓	1	X	Z	Z	Z	Z

X = Don't Care **Z = High Impedance**

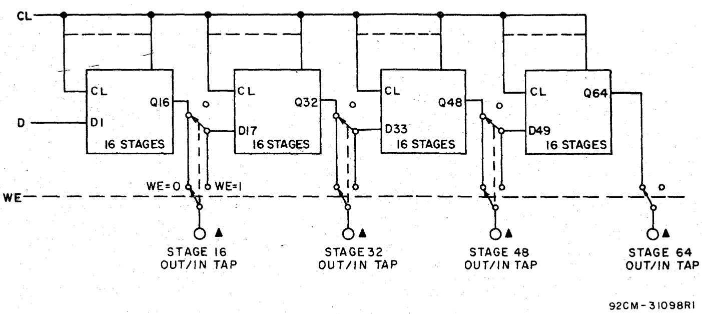


Fig. 1—CD4517B functional block diagram (one half).

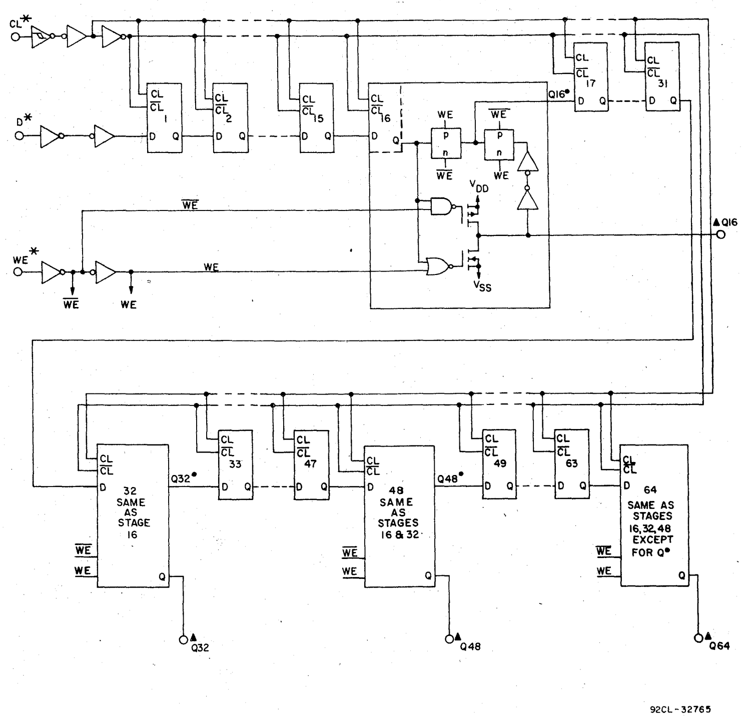
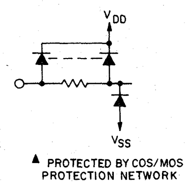
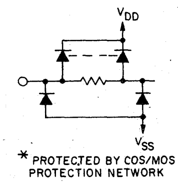


Fig. 2—CD4517B logic block diagram (one half).





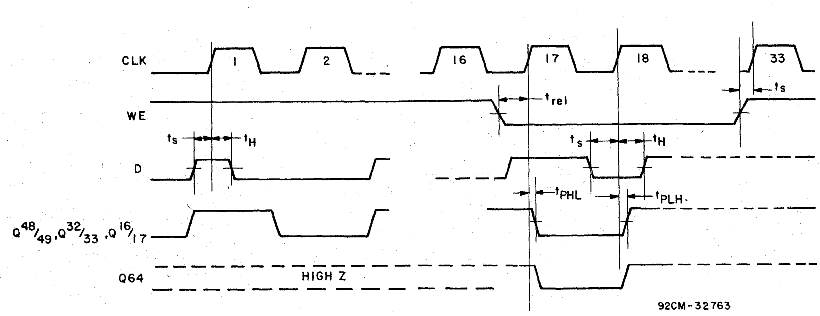


Fig. 3—Dynamic test waveforms.

CD4517B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm10^{-4}$	±0.4	μA

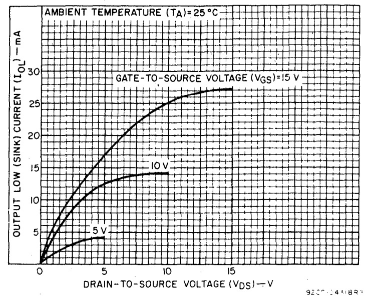


Fig. 4—Typical n-channel output low (sink) current characteristics.

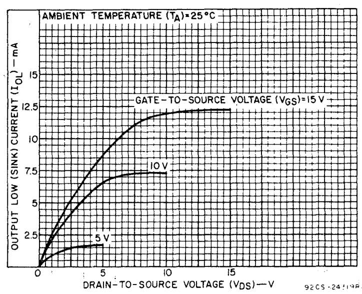


Fig. 5—Minimum n-channel output low (sink) current characteristics.

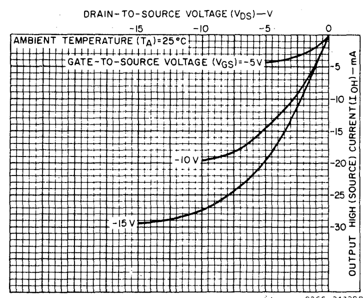


Fig. 6—Typical p-channel output high (source) current characteristics.

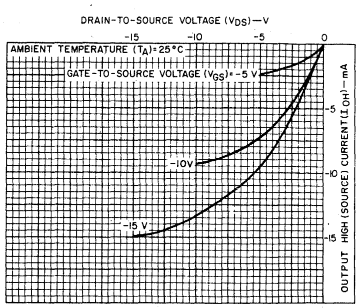


Fig. 7—Minimum p-channel output high (source) current characteristics.

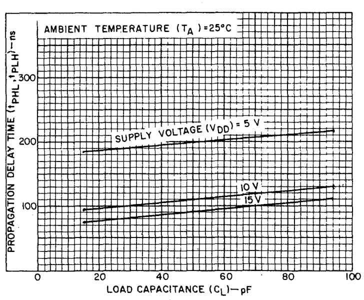


Fig. 8—Typical propagation delay time as a function of load capacitance.

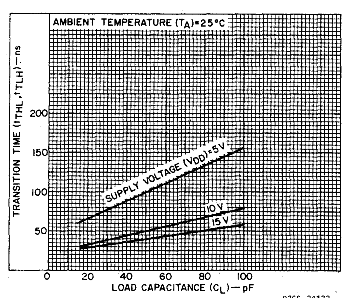


Fig. 9—Typical transition time a a function of load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ*

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time: CL to Bit 16 Tap t_{PHL}, t_{PLH}		5	—	200	400	ns
		10	—	110	220	
		15	—	90	180	
3-State Output, WE to Bit 16 Tap t_{PHZ}, t_{PLZ}; t_{PZH}, t_{PZL} (See Note)		5	—	75	150	ns
		10	—	40	80	
		15	—	30	60	
Output Transition Time t_{THL}, t_{TLH}		5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Write Enable-to-Clock Setup Time		5	−100	−50	—	ns
		10	−50	−25	—	
		15	−30	−15	—	
Data-to-Clock Setup Time, t_S		5	−100	−50	—	ns
		10	−60	−30	—	
		15	−30	−15	—	
Write Enable-to-Clock Release Time		5	—	50	100	ns
		10	—	25	50	
		15	—	20	40	
Data-to-Clock Hold Time, t_H		5	—	100	200	ns
		10	—	50	100	
		15	—	25	50	
Minimum Clock Pulse Width, t_W		5	—	90	180	ns
		10	—	40	80	
		15	—	25	50	
Maximum Clock Input Frequency, f_{CL}		5	3	6	—	MHz
		10	6	12	—	
		15	8	15	—	
Maximum Clock Input Rise or Fall Time, t_{fCL} t_{rCL}		5, 10, 15	UNLIMITED			μs
Input Capacitance C_{IN}	Any Input		—	5	7.5	pF

NOTE: Measured at the point of 10% change in output with an output load of 50 pF, RL = 1 kΩ to V_{DD} for t_{PZL}, t_{PLZ} and R_L = 1 kΩ to V_{SS} for t_{PZH}, t_{PHZ}.

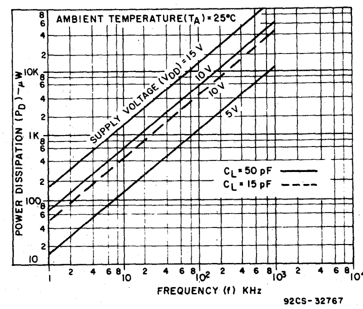


Fig. 10—Typical power dissipation as a function of frequency.

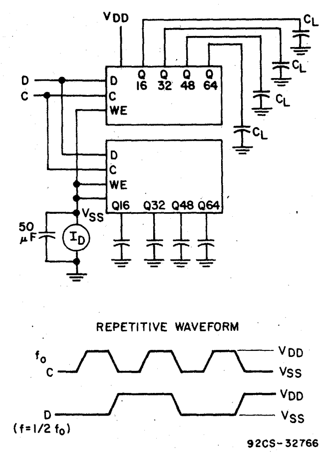


Fig. 11—Dynamic power dissipation test circuit and waveforms.

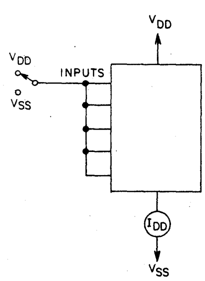


Fig. 12—Quiescent-device-current test circuit.

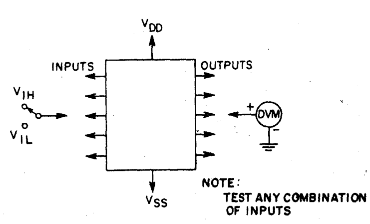


Fig. 13—Input-voltage test circuit.

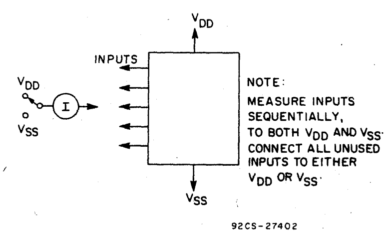
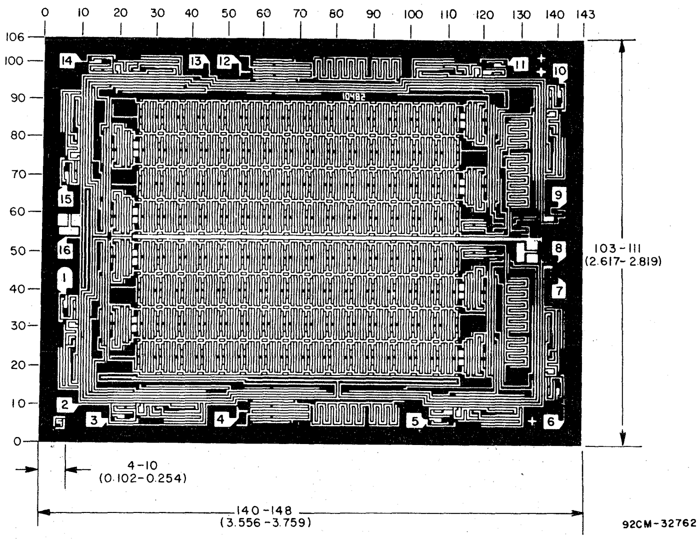


Fig. 14—Input current test circuit.



Dimensions and pad layout for CD4517B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Dual Up-Counters

High-Voltage Types (20-Volt Rating)

CD4518B Dual BCD Up-Counter
CD4520B Dual Binary Up-Counter

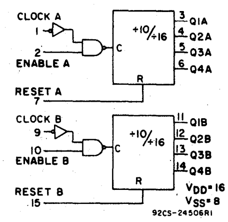
The RCA-CD4518 Dual BCD Up-Counter and CD4520 Dual Binary Up-Counter each consist of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or negative-going transition. For single-unit operation the ENABLE input is maintained high and the counter advances on each positive-going transition of the CLOCK. The counters are cleared by high levels on their RESET lines.

The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the CLOCK input of the latter is held low.

The CD4518B and CD4520B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Medium-speed operation – 6-MHz typical clock frequency at 10 V**
- **Positive- or negative-edge triggering**
- **Synchronous internal carry propagation**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin(over full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



CD4518B, CD4520B FUNCTIONAL DIAGRAM

Applications:

- **Multistage synchronous counting**
- **Multistage ripple counting**
- **Frequency dividers**

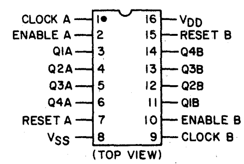
TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
↓	X	0	No Change
X	↑	0	No Change
↑	0	0	No Change
1	↓	0	No Change
X	X	1	Q1 thru Q4 = 0

X = Don't Care 1 ≡ High State 0 ≡ Low State

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F) . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . –55 to +125°C
PACKAGE TYPE E . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . +265°C



CD4518B, CD4520B TERMINAL ASSIGNMENT

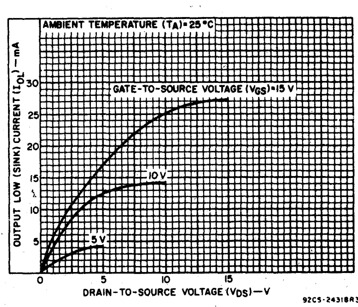


Fig. 1 – Typical output low (sink) current characteristics.

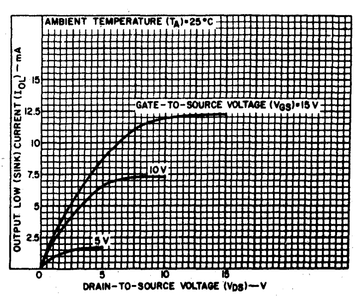


Fig. 2 – Minimum output low (sink) current characteristics.

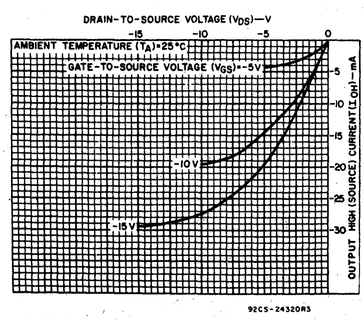


Fig. 3 – Typical output high (source) current characteristics.

CD4518B, CD4520B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages Values at −40, +25, +85 Apply to E Package −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

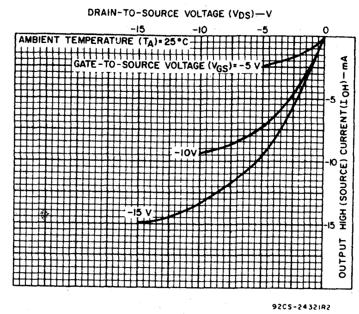


Fig. 4 — Minimum output high (source) current characteristics.

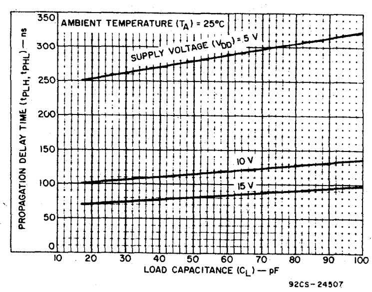


Fig. 5 — Typical propagation delay vs. load capacitance, clock or enable to output.

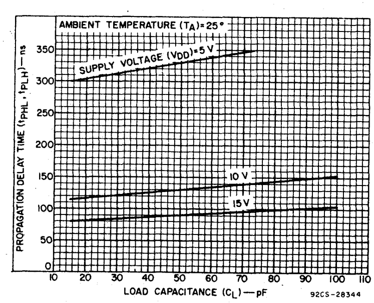


Fig. 6 — Typical propagation delay time vs. load capacitance, reset to output.

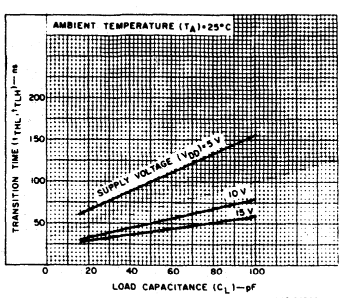


Fig. 7 — Typical transition time vs. load capacitance.

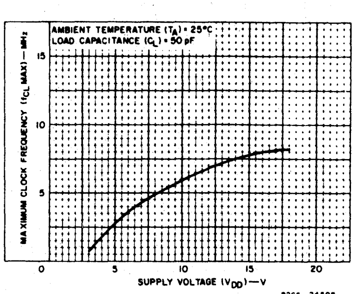


Fig. 8 — Typical maximum-clock-frequency vs. supply voltage.

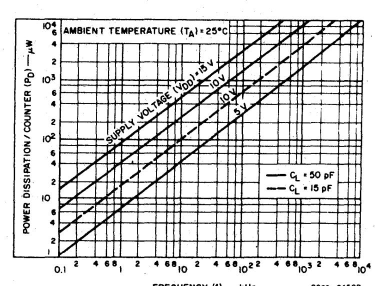


Fig. 9 — Typical power dissipation characteristics.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	18	V
Enable Pulse Width, t_W	5 10 15	400 200 140	– – –	ns
Clock Pulse Width, t_W	5 10 15	200 100 70	– – –	ns
Clock Input Frequency, f_{CL}	5 10 15	dc	1.5 3 4	MHz
Clock Rise or Fall Time, t_rCL or t_fCL:	5 10 15	– –	15 5 5	μs
Reset Pulse Width, t_W	5 10 15	250 110 80	– – –	ns

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C;
Input t_r,t_f=20 ns, C_L=50 pF, R_L=200 KΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} V	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH}: Clock or Enable to Output		5 10 15	– – –	280 115 80	560 230 160	ns
Reset to Output		5 10 15	– – –	330 130 90	650 225 170	ns
Transition Time, t_{THL}, t_{TLH}		5 10 15	– – –	100 50 40	200 100 80	ns
Maximum Clock Input Frequency, f_{CL}		5 10 15	1.5 3 4	3 6 8	– – –	MHz
Minimum Clock Pulse Width, t_W		5 10 15		100 50 35	200 100 70	ns
Clock Rise or Fall Time, t_r or t_f:		5,10 15	– –	– –	15 5	μs
Minimum Reset Pulse Width, t_W		5 10 15	– – –	125 55 40	250 110 80	ns
Minimum Enable Pulse Width, t_W		5 10 15	– – –	200 100 70	400 200 140	ns
Input Capacitance, C_{IN}	Any Input		–	5	7.5	pF
Clock Input Rise or Fall Time, t_{rcl}, t_{rcf}		5 10 15	– – –	– – –	15 5 5	μs

TEST CIRCUITS

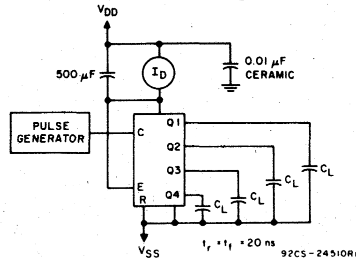


Fig. 10 – Dynamic power dissipation.

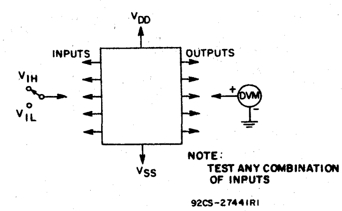


Fig. 11 – Input voltage.

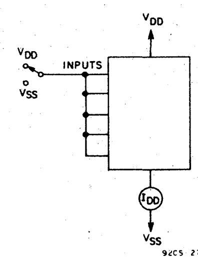


Fig. 12 – Quiescent device current test circuit.

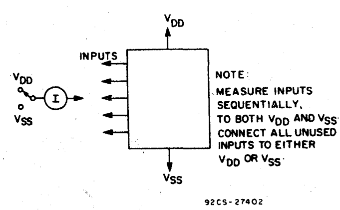


Fig. 13 – Input leakage-current test circuit.

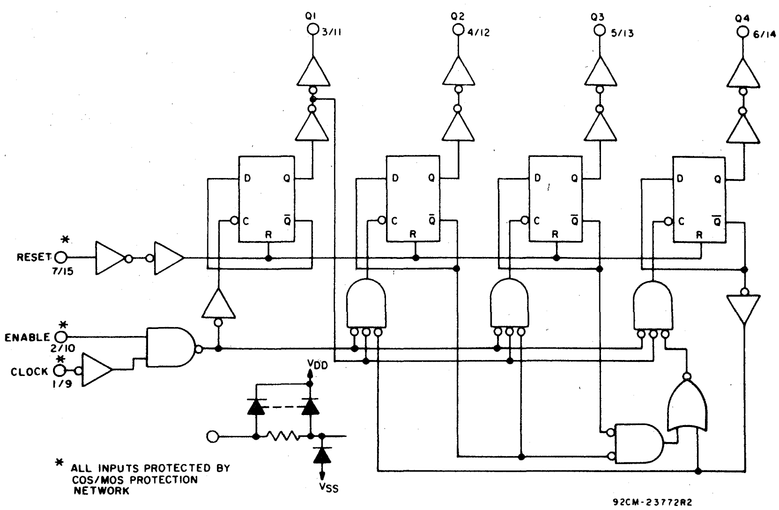


Fig. 14 — Decade counter (CD4518B) logic diagram for one of two identical counters.

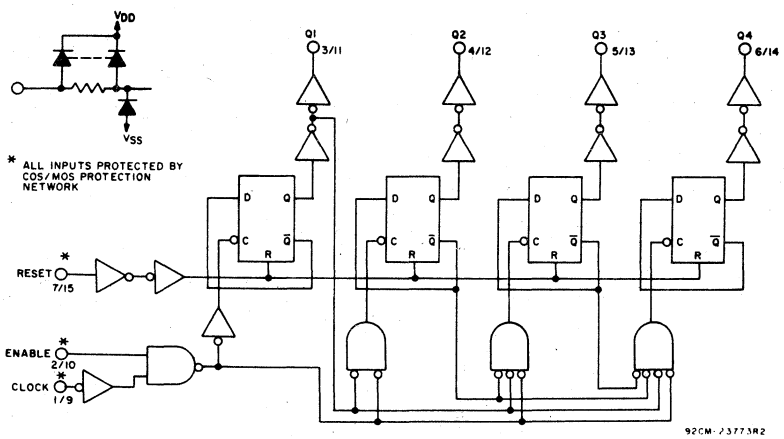


Fig. 15 — Binary counter (CD4520B) logic diagram for one of two identical counters.

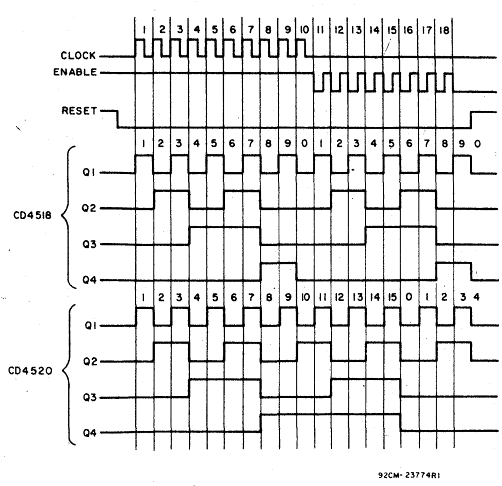


Fig.16 — Timing diagrams for CD4518B and CD4520B.

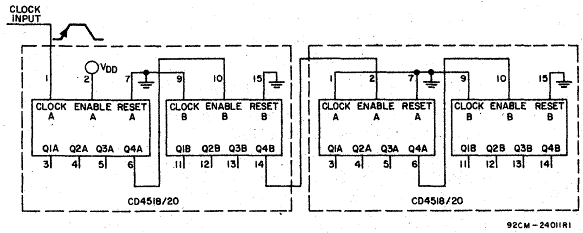
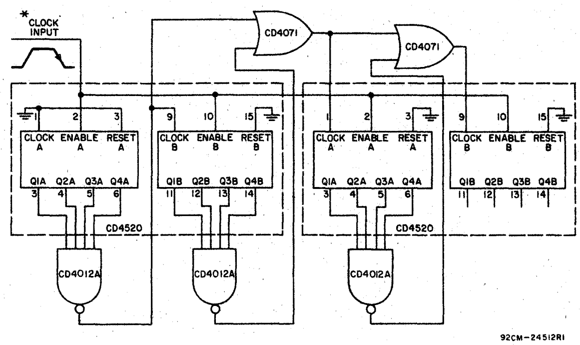
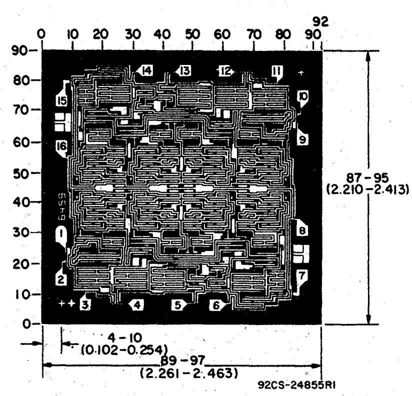


Fig.17 – Ripple cascading of four counters with positive edge triggering.

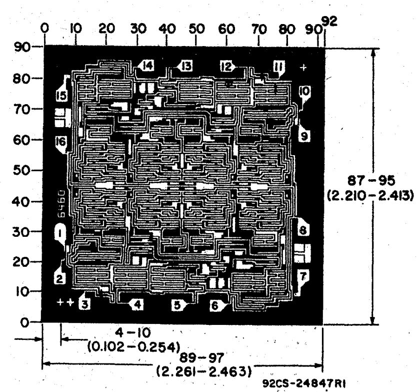


*NOTE:
FOR SYNCHRONOUS CASCADING, THE CLOCK TRANSITION TIME SHOULD BE MADE LESS THAN OR EQUAL TO THE SUM OF THE FIXED PROPAGATION DELAY AT 15 pF AND THE TRANSITION TIME OF THE OUTPUT DRIVER STAGE FOR THE ESTIMATED CAPACITATIVE LOAD.

Fig.18 – Synchronous cascading of four binary counters with negative edge triggering.



Dimensions and pad layout for CD4518BH chip.



Dimensions and pad layout for CD4520BH chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4527B Types

COS/MOS BCD Rate Multiplier

High-Voltage Types (20-Volt Rating)

The RCA-CD4527B is a low-power 4-bit digital rate multiplier that provides an output-pulse rate which is the clock-input-pulse rate multiplied by 1/10 times the BCD input. For example, when the BCD input is 8, there will be 8 output pulses for every 10 input pulses. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversion, and frequency division.

For fractional multipliers with more than one digit, CD4527B devices may be cascaded in two different modes: the Add mode and the Multiply mode. (See Figs.12 and 15). In the Add mode,

$$\text{Output Rate} = (\text{Clock Rate})\left[\begin{array}{l}0.1\ BCD_1 + 0.01\ BCD_2 + \\ 0.001\ BCD_3 + \cdots\end{array}\right]$$

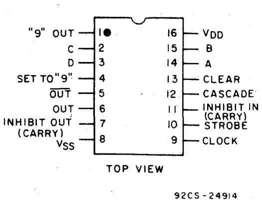
In the Multiply mode, the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second one,

e.g. $\frac{9}{10} \times \frac{4}{10} = \frac{36}{100}$ or 36 output pulses for every 100 clock input pulses.

The CD4527B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

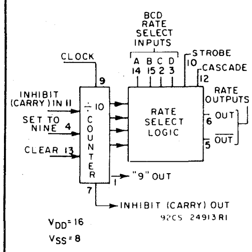
- **Numerical control**
- **Instrumentation**
- **Digital filtering**
- **Frequency synthesis**



TERMINAL ASSIGNMENT

Features:

- **Cascadable in multiples of 4-bits**
- **Set to "9" input and "9" detect output**
- **100% test for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics**
- **Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) =**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS AT T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Set or Clear Pulse Width, t_W	5	160	–	ns
	10	90	–	
	15	60	–	
Clock Pulse Width, t_W	5	330	–	ns
	10	170	–	
	15	100	–	
Clock Frequency, f_{CL}	5	dc	1.2	MHz
	10		2.5	
	15		3.5	
Clock Rise or Fall Time, t_{rCL} or t_{fCL}	5,10,15	–	15	µs
Inhibit In Setup Time, t_{SU}	5	100	–	ns
	10	40	–	
	15	20	–	
Inhibit In Removal Time, t_{REM}	5	240	–	ns
	10	130	–	
	15	110	–	
Set Removal Time, t_{REM}	5	150	–	ns
	10	80	–	
	15	50	–	
Clear Removal Time, t_{REM}	5	60	–	ns
	10	40	–	
	15	30	–	

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

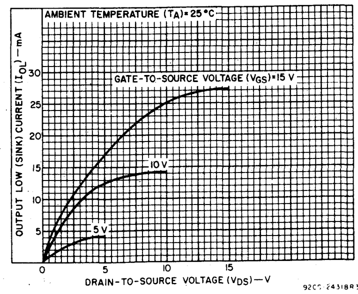


Fig.1 – Typical output low (sink) current characteristics.

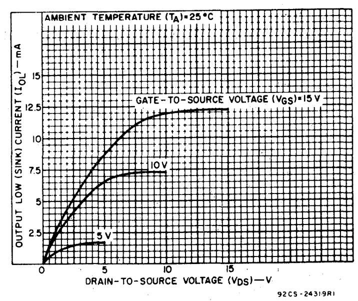


Fig.2 – Minimum output low (sink) current characteristics.

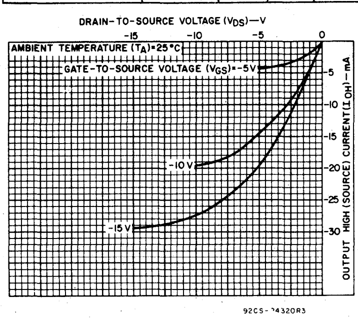


Fig.3 – Typical output high (source) current characteristics.

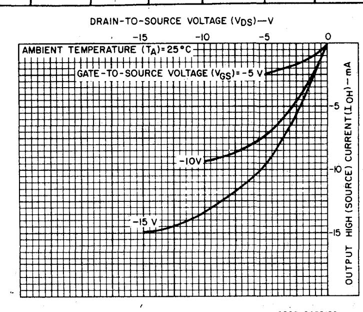


Fig.4 – Minimum output high (source) current characteristics.

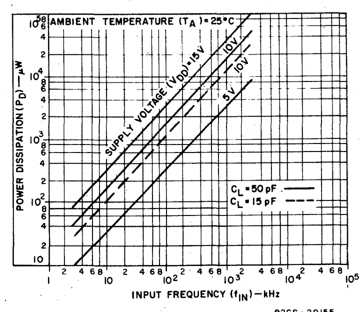


Fig.5 – Typical dynamic power dissipation as a function of input frequency.

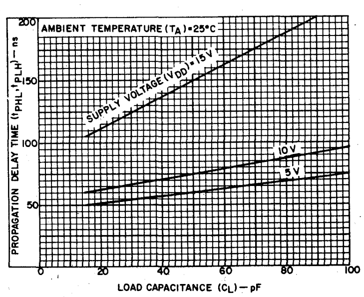


Fig.6 – Typical propagation delay time as a function of load capacitance (Clock or Strobe to Out).

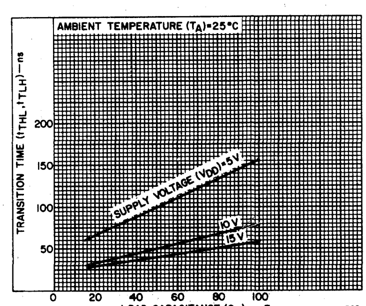


Fig.7 – Typical transition time as a function of load capacitance.

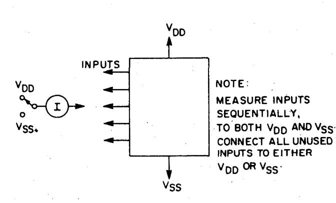


Fig.8 – Input current test circuit.

CD4527B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C:
Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
		V_{DD} (V)	Min.	Typ.	Max.	
Propagation Delay Time, t_{PHL}, t_{PLH} Clock to $\overline{Out}$		5	–	110	220	ns
		10	–	55	110	
		15	–	45	90	
Clock or Strobe to Out		5	–	150	300	
		10	–	75	150	
		15	–	60	120	
Clock to Inhibit Out High Level to Low Level		5	–	320	640	ns
		10	–	145	290	
		15	–	100	200	
Low Level to High Level		5	–	250	500	
		10	–	100	200	
		15	–	75	150	
Clear to Out		5	–	380	760	ns
		10	–	175	350	
		15	–	130	260	
Clock to "9" or "15" Out		5	–	300	600	
		10	–	125	250	
		15	–	90	180	
Cascade to Out		5	–	90	180	ns
		10	–	45	90	
		15	–	35	70	
Inhibit In to Inhibit Out		5	–	130	260	
		10	–	60	120	
		15	–	45	90	
Set to Out		5	–	330	660	ns
		10	–	150	300	
		15	–	110	220	
Transition Time, t_{THL}, t_{TLH}		5	–	100	200	
		10	–	50	100	
		15	–	40	80	
Maximum Clock Frequency, f_{CL}		5	1.2	2.4	–	MHz
		10	2.5	5	–	
		15	3.5	7	–	
Minimum Clock Pulse Width, t_W		5	–	165	330	ns
		10	–	85	170	
		15	–	50	100	
Clock Rise or Fall Time, t_{rCL}, t_{fCL}		5	–	–	15	μs
		10	–	–	15	
		15	–	–	15	
Minimum Set or Clear Pulse Width, t_W		5	–	80	160	ns
		10	–	45	90	
		15	–	30	60	
Minimum Inhibit In Setup Time, t_{SU}		5	–	50	100	
		10	–	20	40	
		15	–	10	20	
Minimum Inhibit In Removal Time, t_{REM}		5	–	120	240	ns
		10	–	65	130	
		15	–	55	110	
Minimum Set Removal Time, t_{REM}		5	–	75	150	
		10	–	40	80	
		15	–	25	50	
Minimum Clear Removal Time, T_{REM}		5	–	30	60	ns
		10	–	20	40	
		15	–	15	30	
Input Capacitance, C_{IN}	Any Input		–	5	7.5	pF

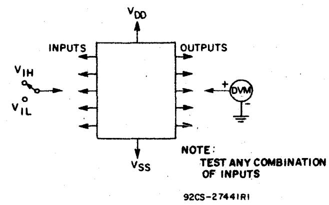


Fig.9 – Input voltage test circuit.

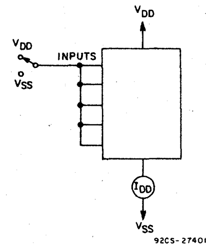


Fig.10 – Quiescent device current test circuit.

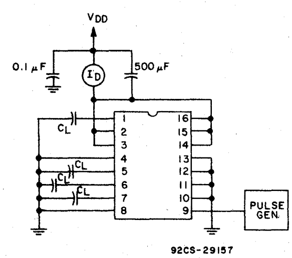


Fig.11 – Dynamic power dissipation test circuit.

APPLICATIONS

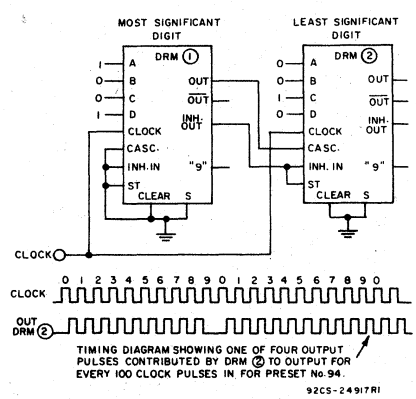


Fig.12 – Two CD4527B's cascaded in the "Add" mode with a preset number of 94 $\left(\frac{9}{10} + \frac{4}{100} = \frac{94}{100}\right)$.

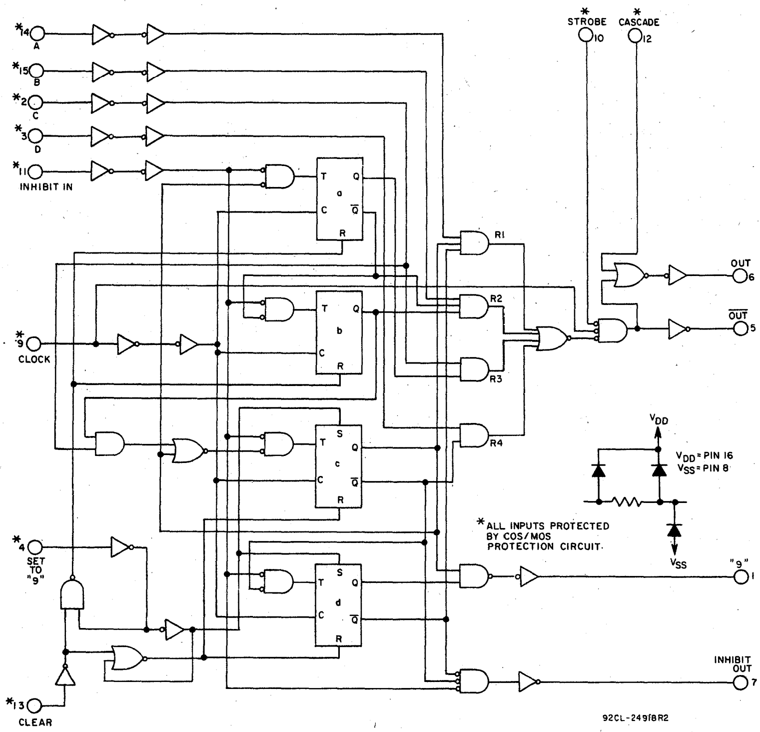


Fig. 13 – Logic diagram.

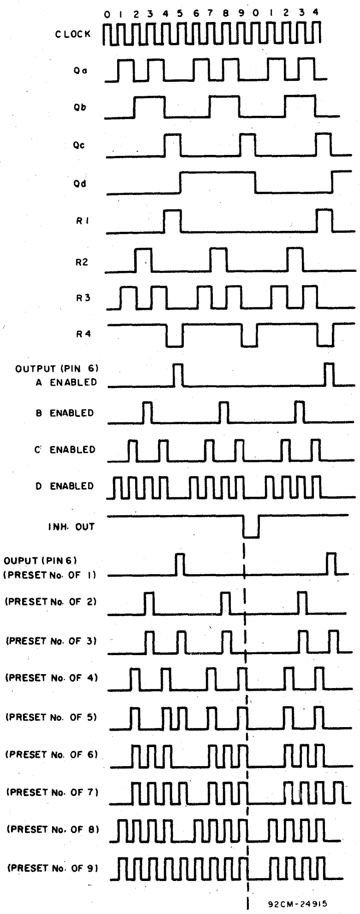
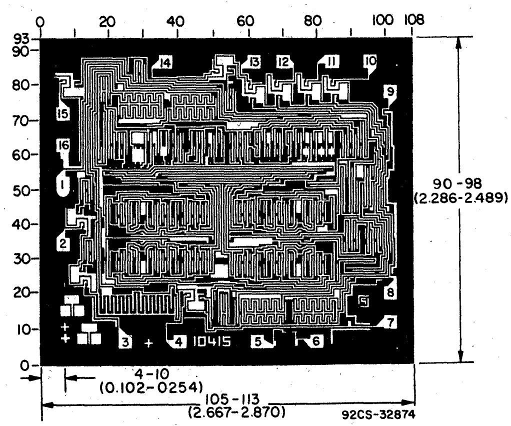


Fig. 14 – Timing diagram (See Logic Diagram).



Dimensions and Pad Layout for CD4527BH

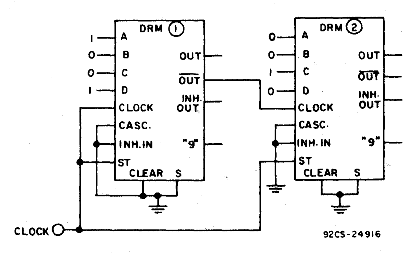


Fig. 15 – Two CD4527B's cascaded in the "Multiply" mode with a preset number of 36 $\left(\frac{9}{10} \times \frac{4}{10} = \frac{36}{100}\right)$.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD4527B Types

TRUTH TABLE

INPUTS										OUTPUTS			
Number of Pulses or Input Logic Level (0 = Low; 1 = High; X = Don't Care)										Number of Pulses or Output Logic Level (L = Low; H = High)			
D	C	B	A	CLK	INH IN	STR	CAS	CLR #	SET #	OUT	$\overline{OUT}$	INH OUT	"9" OUT
0	0	0	0	10	0	0	0	0	0	L	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	†	†	H	†
X	X	X	X	10	0	1	0	0	0	L	H	1	1
X	X	X	X	10	0	0	1	0	0	H	*	1	1
1	X	X	X	10	0	0	0	1	0	10	10	H	L
0	X	X	X	10	0	0	0	1	0	L	H	H	L
X	X	X	X	10	0	0	0	0	1	L	H	L	H

* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).
† Depends on internal state of counter.
#Clear and Set Inputs should not be high at the same time; device draws increased quiescent current when in this non-valid state.

COS/MOS 8-Bit Priority Encoder

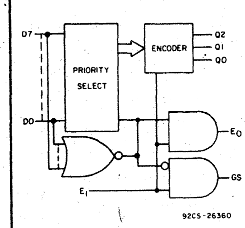
High-Voltage Types (20-Volt Rating)

The RCA-CD4532B consists of combinational logic that encodes the highest priority input (D7-D0) to a 3-bit binary code. The eight inputs, D7 through D0, each have an assigned priority; D7 is the highest priority and D0 is the lowest. The priority encoder is inhibited when the chip-enable input E_I is low. When E_I is high, the binary representation of the highest-priority input appears on output lines Q2-Q0, and the group select line GS is high to indicate that priority inputs are present. The enable-out (E_O) is high when no priority inputs are present. If any one input is high, E_O is low and all cascaded lower-order stages are disabled.

The CD4532B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:
- **Converts from 1 of 8 to binary**
- **Provides cascading feature to handle any number of inputs**
- **Group select indicates one or more priority inputs**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 µA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range):**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:
- **Priority encoder**
- **Binary or BCD encoder (keyboard encoding)**
- **Floating point arithmetic**



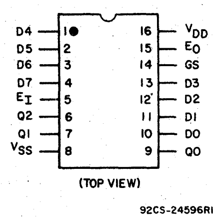
FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	Min.	Max.	Units
Supply Voltage Range (for T_A = Full Package Temp. Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C



TERMINAL ASSIGNMENT

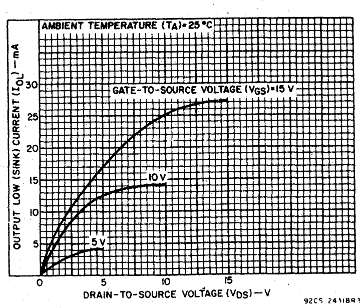


Fig. 1 — Typical output low (sink) current characteristics.

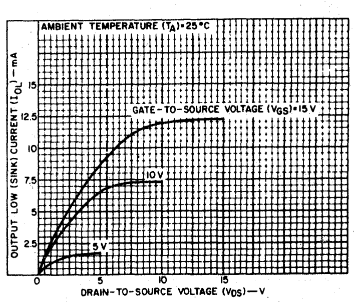


Fig. 2 — Minimum output low (sink) current characteristics.

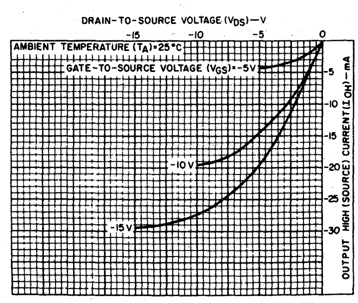


Fig. 3 — Typical output high (source) current characteristics.

CD4532B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages Values at –40, +25, +85 Apply to E Package –55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; C_L=50 pF, Input t_r,t_f= 20 ns, R_L=200 KΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} VOLTS	LIMITS ALL TYPES TYP.	MAX.	UNITS
Propagation Delay Time t_{PHL}, t_{PLH} E_I to E_O, E_I to GS	5	110	220	ns
	10	55	110	
	15	45	85	
E_I to Qm, Dn to GS	5	170	340	
	10	85	170	
	15	65	125	
Dn to Q_M	5	220	440	
	10	110	220	
	15	85	160	
Transition Time t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance C_{IN}	Any Input	5	7.5	pF

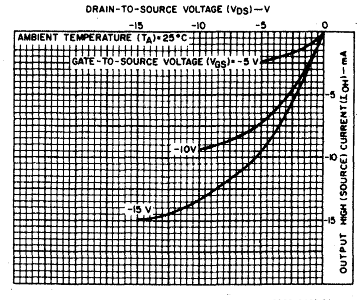


Fig. 4 — Minimum output high (source) current characteristics.

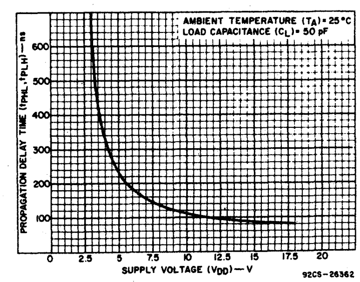


Fig. 5 — Typical propagation delay (Dn to Qm) vs. supply voltage.

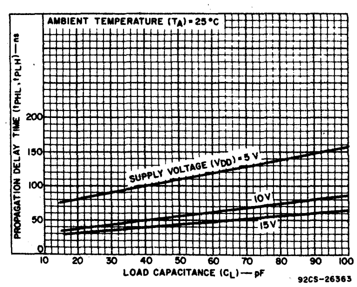


Fig. 6 — Typical propagation delay (E_I to GS, E_I to E_O) vs. load capacitance.

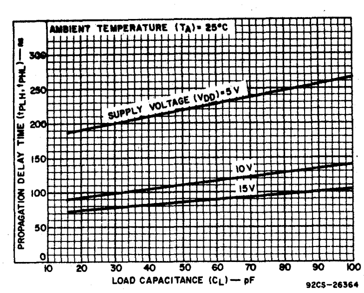


Fig. 7 — Typical propagation delay (Dn to Qm) vs. load capacitance.

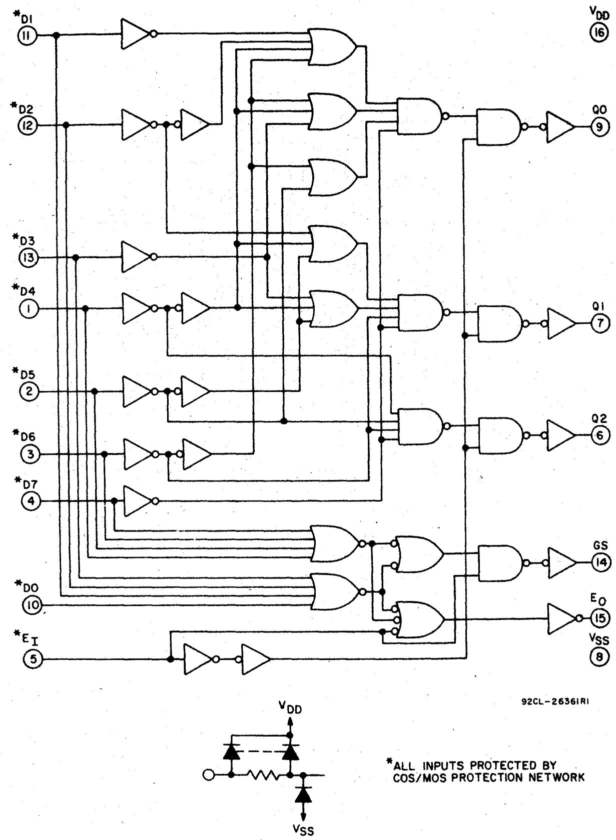


Fig. 8 — CD4532 logic diagram.

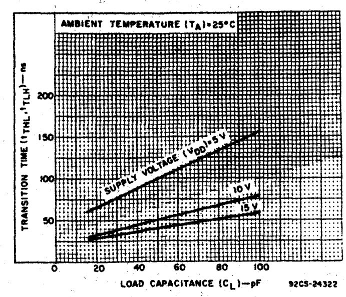


Fig.9 — Typical transition time vs. load capacitance.

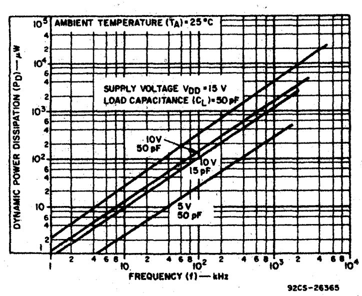


Fig.10 — Typical dynamic power dissipation vs. frequency.

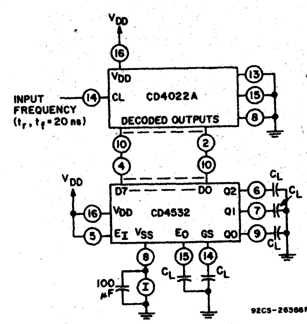


Fig.11 — Dynamic power dissipation test circuit.

TRUTH TABLE

Input									Output				
E_I	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_O
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care   Logic 1 ≡ High   Logic 0 ≡ Low

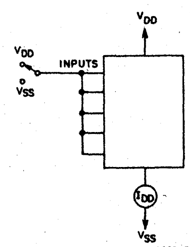


Fig.12 — Quiescent device current test circuit.

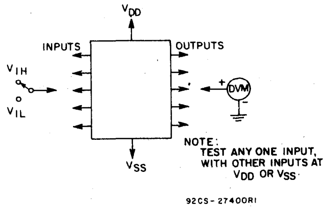


Fig. 13 – Input voltage test circuit.

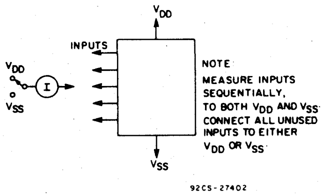
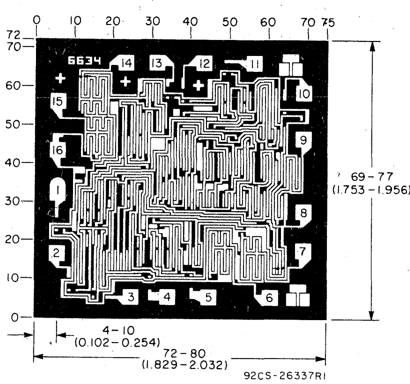


Fig. 14 – Input current test circuit.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for CD4532BH.

APPLICATIONS

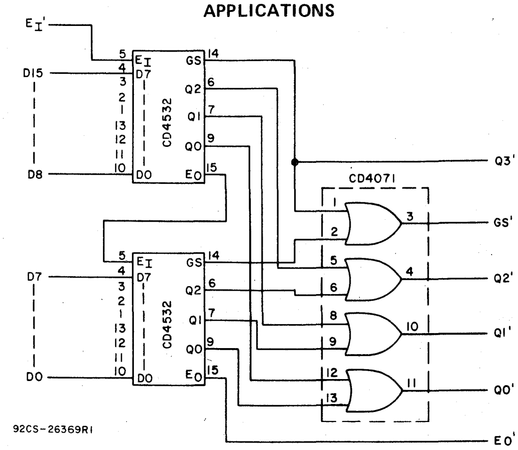
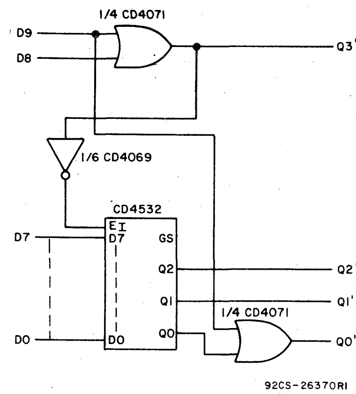


Fig. 15 – 16-level priority encoder.



TRUTH TABLE

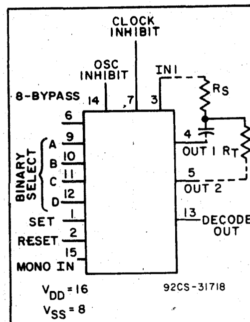
Input										Output				
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q3'	Q2'	Q1'	Q0'
1	X	X	X	X	X	X	X	X	X	0	1	0	0	1
0	1	X	X	X	X	X	X	X	X	0	1	0	0	0
0	0	1	X	X	X	X	X	X	X	1	0	1	1	1
0	0	0	1	X	X	X	X	X	X	1	0	1	1	0
0	0	0	0	1	X	X	X	X	X	1	0	1	0	1
0	0	0	0	0	1	X	X	X	X	1	0	1	0	0
0	0	0	0	0	0	1	X	X	X	1	0	0	1	1
0	0	0	0	0	0	0	1	X	X	1	0	0	1	0
0	0	0	0	0	0	0	0	1	X	1	0	0	0	1
0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care Logic 1 ≡ High Logic 0 ≡ Low

Fig. 16 – 0-to-9 keyboard encoder.

COS/MOS Programmable Timer

High-Voltage Types (20-Volt Rating)



FUNCTIONAL DIAGRAM

The RCA-CD4536B is a programmable timer consisting of 24 ripple-binary counter stages. The salient feature of this device is its flexibility. The device can count from 1 to 2^{24} or the first 8 stages can be bypassed to allow an output, selectable by a 4-bit code, from any one of the remaining 16 stages. It can be driven by an external clock or an RC oscillator that can be constructed using on-chip components. Input IN1 serves as either the external clock input or the input to the on-chip RC oscillator. OUT1 and OUT2 are connection terminals for the external RC components. In addition, an on-chip monostable circuit is provided to allow a variable pulse width output. Various timing functions can be achieved using combinations of these capabilities.

A logic 1 on the 8-BYPASS input enables a bypass of the first 8 stages and makes stage 9 the first counter stage of the last 16 stages. Selection of 1 of 16 outputs is accomplished by the decoder and the BCD inputs A, B, C and D. MONO IN is the timing input for the on-chip monostable oscillator. Grounding of the MONO IN terminal through a resistor of 10K ohms or higher, disables the one-shot circuit and connects the decoder directly to the DECODE OUT terminal. A resistor to V_{DD} and a capacitor to ground from the MONO IN terminal enables the one-shot circuit and controls its pulse width.

A fast test mode is enabled by a logic 1 on 8-BYPASS, SET, and RESET. This mode divides the 24-stage counter into three 8-stage sections to facilitate a fast test sequence.

The CD4536B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **24 flip-flop stages — counts from 2^0 to 2^{24}**
- **Last 16 stages selectable by BCD select code**
- **Bypass input allows bypassing first 8 stages**
- **On-chip RC oscillator provision**
- **Clock inhibit input**
- **Schmitt-trigger in clock line permits operation with very long rise and fall times**
- **On-chip monostable output provision**
- **Typical f_{CL} = 3 MHz at V_{DD} = 10 V**
- **Test mode allows fast test sequence**
- **Set and reset inputs**
- **Capable of driving two low power TTL loads, one lower-power Schottky load, or two HTL loads over the rated temperature range**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F,) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . . +265°C

DECODE OUT SELECTION TABLE

D	C	B	A	NUMBER OF STAGES IN DIVIDER CHAIN	
				8-BYPASS = 0	8-BYPASS = 1
0	0	0	0	9	1
0	0	0	1	10	2
0	0	1	0	11	3
0	0	1	1	12	4
0	1	0	0	13	5
0	1	0	1	14	6
0	1	1	0	15	7
0	1	1	1	16	8
1	0	0	0	17	9
1	0	0	1	18	10
1	0	1	0	19	11
1	0	1	1	20	12
1	1	0	0	21	13
1	1	0	1	22	14
1	1	1	0	23	15
1	1	1	1	24	16

0 = Low Level 1 = High Level

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages; Values at −40, +25, +85 Apply to E Package: −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

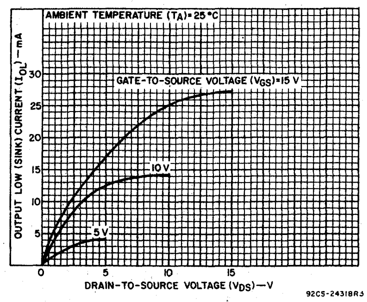


Fig. 2—Typical output low (sink) current characteristics.

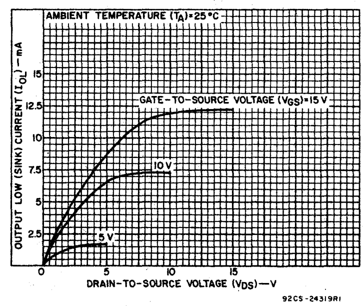


Fig. 3—Minimum output low (sink) current characteristics.

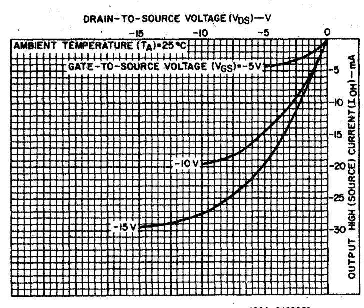


Fig. 4—Typical output high (source) current characteristics.

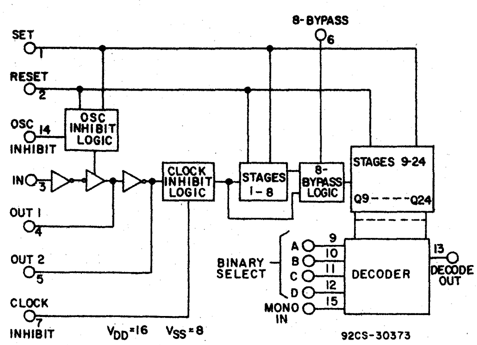


Fig. 1 — Functional block diagram.

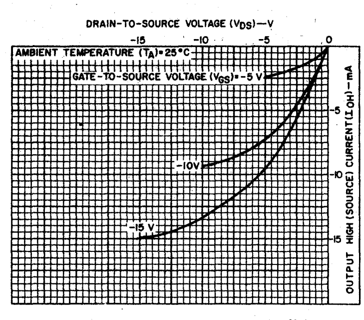


Fig. 5—Minimum output high (source) current characteristics.

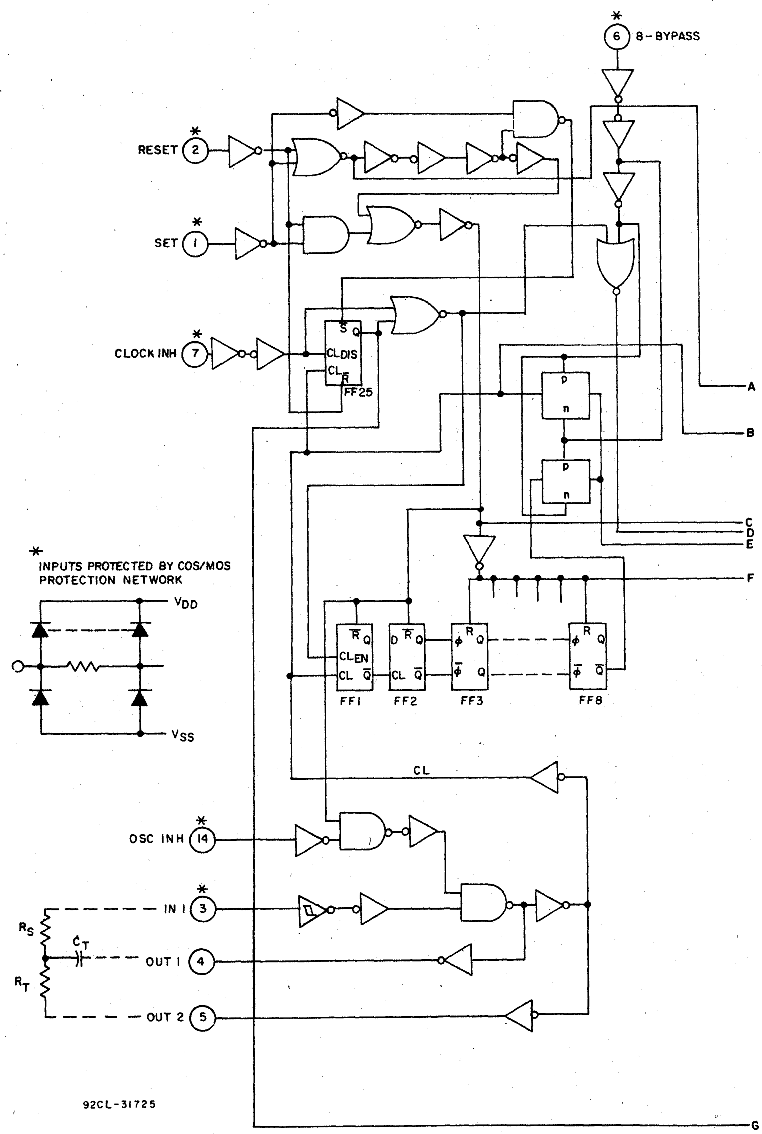


Fig.6 - Logic diagram for CD4536B [continued on next page].

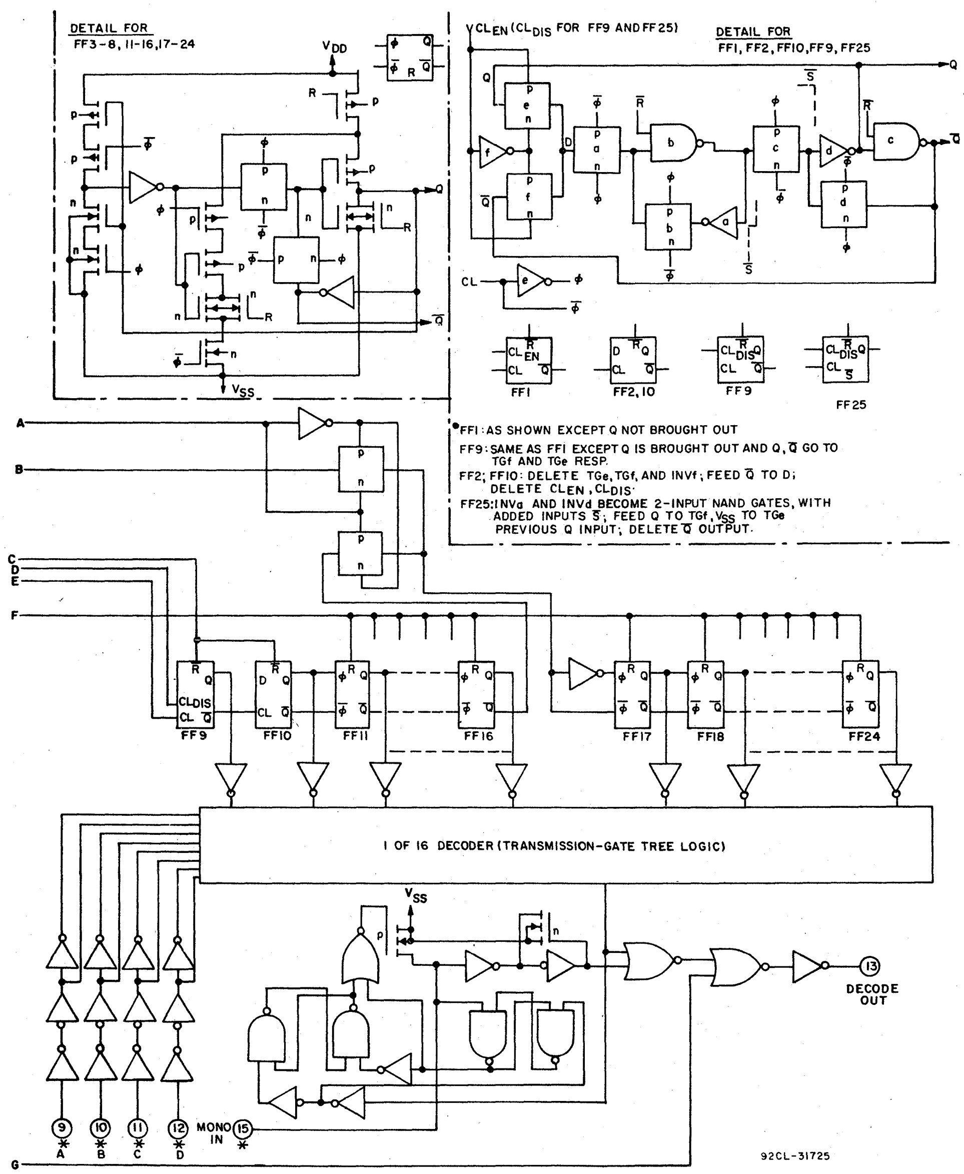
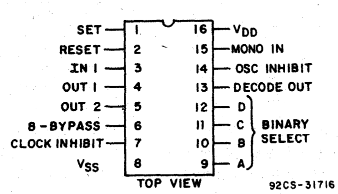


Fig.6 - Logic diagram for CD4536B [continued from previous page].

DYNAMIC ELECTRICAL CHARACTERISTICS, *at $T_A = 25°C$, Input t_r, $t_f = 20$ ns, C_L = 50 pF, R_L = 200 kΩ*

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Times: Clock to Q1, 8-Bypass High t_{PHL}, t_{PLH}	5	—	1	2	μs
	10	—	0.5	1	
	15	—	0.35	0.7	
Clock to Q1, 8-Bypass Low t_{PHL}, t_{PLH}	5	—	2.5	5	μs
	10	—	0.8	1.6	
	15	—	0.6	1.2	
Clock to Q16, T_{PHL} t_{PLH}	5	—	4	8	μs
	10	—	1.5	3	
	15	—	1	2	
Q_n to Q_{n+1}, t_{PHL}, t_{PLH}	5	—	150	300	ns
	10	—	75	150	
	15	—	50	100	
Set to Q_n, t_{PLH}	5	—	300	600	ns
	10	—	125	250	
	15	—	80	160	
Reset to Q_n, t_{PHL}	5	—	3	6	μs
	10	—	1	2	
	15	—	0.75	1.5	
Transition Time, t_{THL}, t_{TLH}	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Minimum Pulse Widths: Clock	5	—	200	400	ns
	10	—	75	150	
	15	—	50	100	
Set	5	—	200	400	ns
	10	—	100	200	
	15	—	60	120	
Reset	5	—	3	6	μs
	10	—	1	2	
	15	—	0.75	1.5	
Minimum Set Recovery Time,	5	—	2.5	5	μs
	10	—	1	2	
	15	—	0.6	1.6	
Minimum Reset Recovery Time,	5	—	3.5	7	μs
	10	—	1.5	3	
	15	—	1	2	
Maximum Clock Pulse Input Frequency, f_{CL}	5	0.5	1	—	MHz
	10	1.5	3	—	
	15	2.5	5	—	
Maximum Clock Pulse Input Rise or Fall Time, t_r, t_f	5,10,15		Unlimited		μs



Terminal Assignment

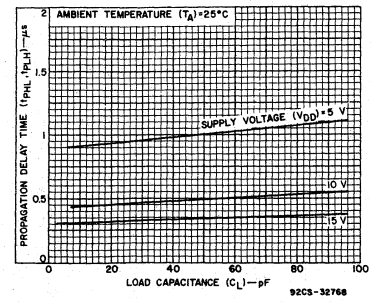


Fig. 7—Typical propagation delay time as a function of load capacitance (CLOCK to Q_1, 8-BYPASS high).

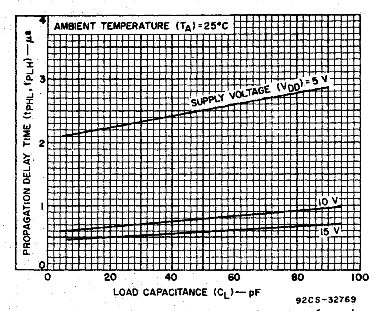


Fig. 8—Typical propagation delay time as a function of load capacitance (CLOCK to Q_1, 8-BYPASS low).

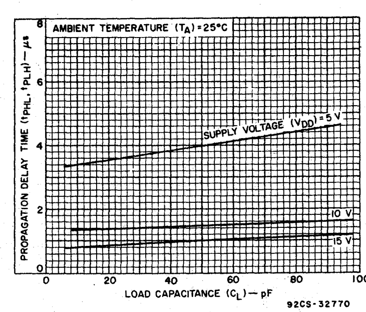


Fig. 9—Typical propagation delay time as a function of load capacitance (CLOCK to Q_{16}, 8-BYPASS high).

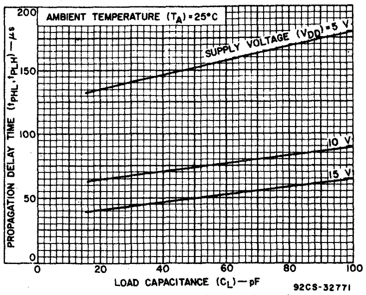


Fig. 10—Typical propagation delay time as a function of load capacitance (Q_N to Q_{N+1}).

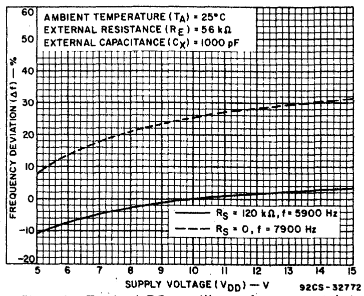


Fig. 11—Typical RC oscillator frequency deviation as a function of supply voltage.

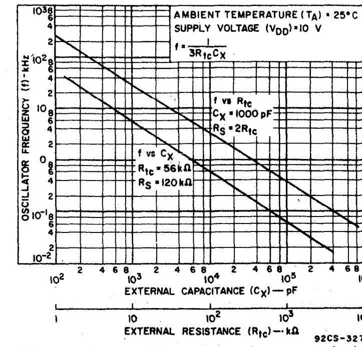


Fig. 12—Typical RC oscillator frequency deviation as a function of time constant resistance and capacitance.

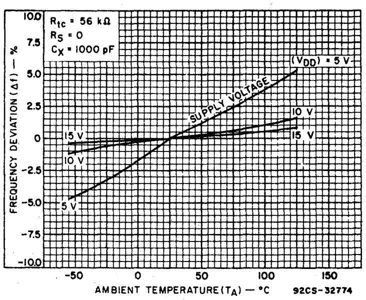


Fig. 13—Typical RC oscillator frequency deviation as a function of ambient temperature (R_S = 0).

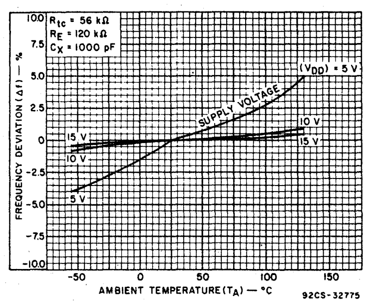


Fig. 14—Typical RC oscillator frequency deviation as a function of ambient temperature (R_S = 120 kΩ).

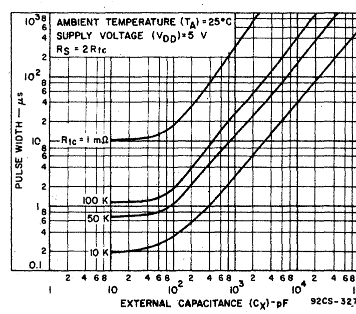


Fig. 15—Typical pulse width as a function of external capacitance (V_{DD} = 5 V).

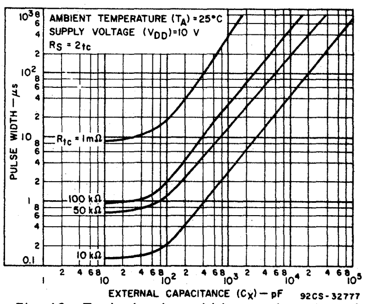


Fig. 16—Typical pulse width as a function of external capacitance (V_{DD} = 10 V).

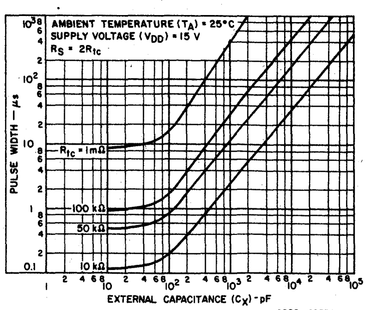


Fig. 17—Typical pulse width as a function of external capacitance (V_{DD} = 15 V).

Functional Test Sequence

Inputs				Outputs	Comments
In_1	Set	Reset	8-Bypass	Decade Out Q1 thru Q24	All 24 steps are in Reset mode
1	0	1	1	0	
1	1	1	1	0	Counter is in three 8-stage section in parallel mode
0	1	1	1	0	First "1" to "0" transition of clock
1 0 — — —	1	1	1		255 "1" to "0" transitions are clocked in the counter
0	1	1	1	1	The 255 "1" to "0" transition
0	0	0	0	1	Counter converted back to 24 stages in series mode Set and Reset must be connected together and simultaneously go from "1" to "0"
1	0	0	0	1	In_1 Switches to a "1"
0	0	0	0	0	Counter Ripples from an all "1" state to an all "0" state

FUNCTIONAL TEST SEQUENCE

Test Function (Figure 11) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a "1". The counter is now returned to the normal 24-steps in series configuration. One more pulse is entered into In_1 which will cause the counter to ripple from an all "1" state to an all "0" state.

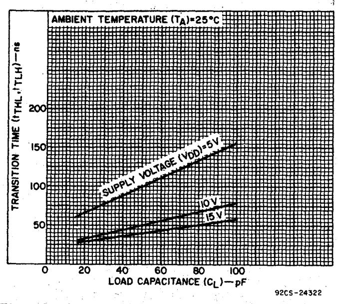


Fig. 18—Typical transition time as a function of load capacitance.

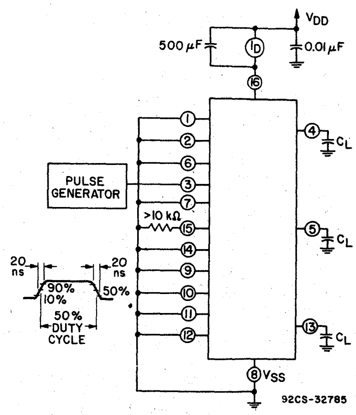


Fig. 20—Dynamic power dissipation test circuit and waveform.

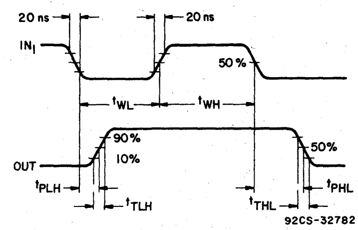
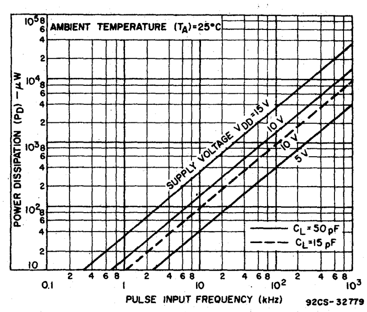


Fig. 22—Input waveforms for switching-time test circuit.



19 —Typical dynamic power dissipation as a function of input pulse frequency.

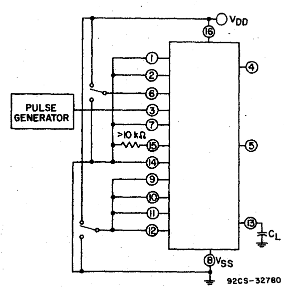


Fig. 21—Switching time test circuit.

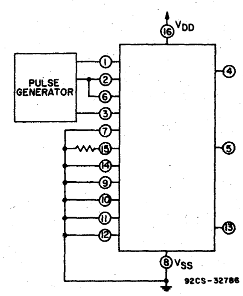


Fig. 23—Functional test circuit.

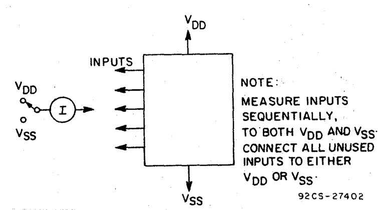


Fig. 24—Input-current test circuit.

TRUTH TABLE

IN1	SET	RESET	CLOCK INH	OSC INH	OUT1	OUT2	DECODE OUT
_/¯	0	0	0	0	_/¯	¯_	No Change
¯_	0	0	0	0	¯_	_/¯	Advance to Next State
X	1	0	0	0	0	1	1
X	0	1	0	0	0	1	0
X	0	0	1	0			No Change
0	0	0	0	X	0	1	No Change
1	0	0	0	_/¯	¯_	_/¯	Advance to Next State

0 = Low Level   1 = High Level   X = Don't Care

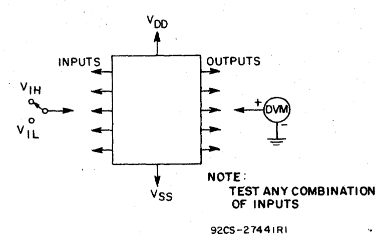


Fig. 25—Input-voltage test circuit.

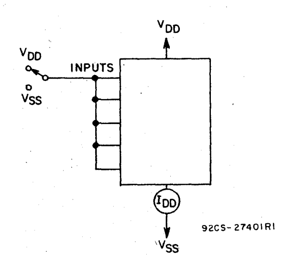


Fig. 26—Quiescent-device current test circuit.

APPLICATIONS

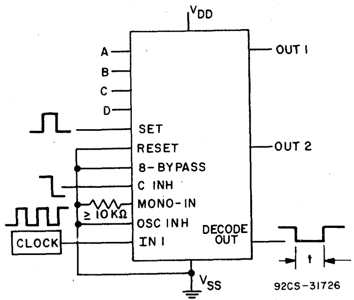


Fig. 27—Time interval configuration using external clock; set and clock inhibit functions.

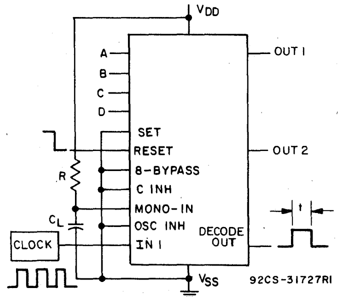


Fig. 28—Time interval configuration using external clock; reset and output monostable to achieve a pulse output.

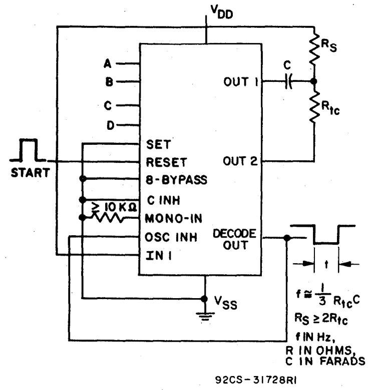


Fig. 29—Time interval configuration using on-chip RC oscillator and reset input to initiate time interval.

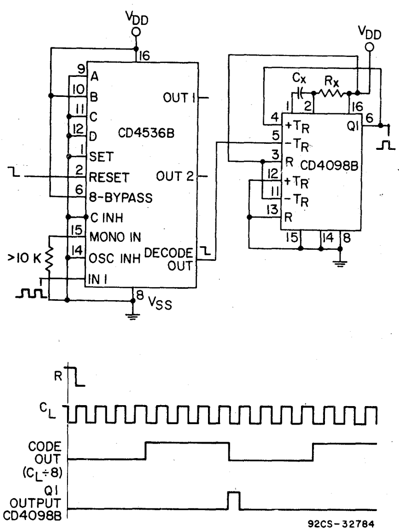


Fig.30 – Application showing use of CD4098B and CD4536B to get decode pulse 8 clock pulses after Reset pulse.

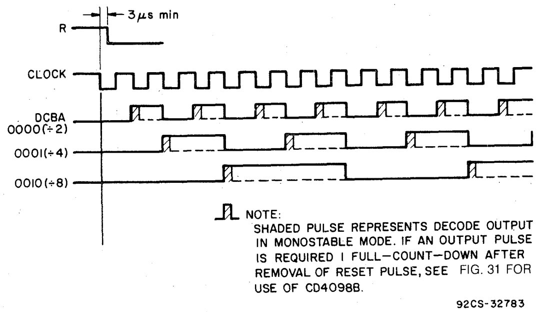
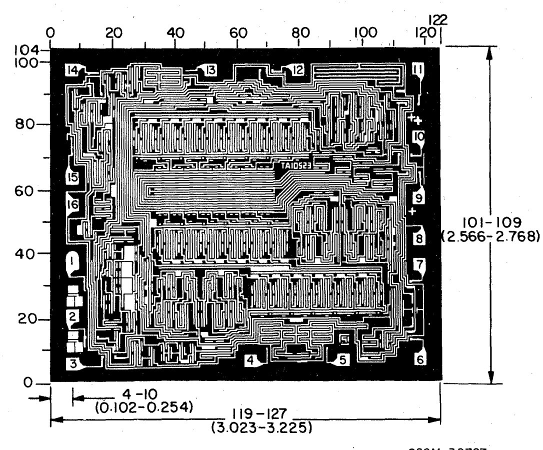


Fig.31 — CD4536B Timing Diagram.

Dimensions and pad layout for CD4536BH.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Dual Precision Monostable Multivibrator

High-Voltage Types (20-Volt Rating)

The RCA-CD4538B dual precision monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor (R_X) and an external capacitor (C_X) control the timing and accuracy for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_X and C_X. Precision control of output pulse widths is achieved through linear CMOS techniques.

Leading-edge-triggering (+TR) and trailing-edge-triggering (−TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to V_{SS}. An unused −TR input should be tied to V_{DD}. A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to V_{DD}. However, if an entire section of the CD4538B is not used, its inputs must be tied to either V_{DD} or V_{SS}. See Table I.

In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse.

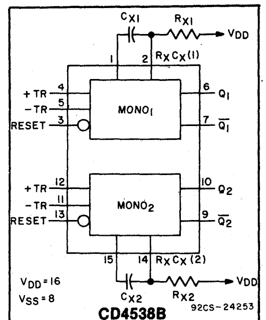
Features:
- *Retriggerable/resettable capability*
- *Trigger and reset propagation delays independent of R_X, C_X*
- *Triggering from leading or trailing edge*
- *Q and $\overline{Q}$ buffered outputs available*
- *Separate resets*
- *Wide range of output-pulse widths*
- *Schmitt trigger input allows unlimited rise and fall times on +TR and −TR inputs*
- *100% tested for maximum quiescent current at 20 V*

For operation in the non-retriggerable mode, $\overline{Q}$ is connected to −TR when leading-edge triggering (+TR) is used or Q is connected to +TR when trailing-edge triggering (−TR) is used. The time period (T) for this multivibrator can be calculated by: $T = R_X C_X$.

The minimum value of external resistance, R_X, is 4 KΩ. The maximum and minimum values of external capacitance, C_X, are 100 μF and 5000 pF, respectively.

The CD4538B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

The CD4538B is similar to type MC14538 and is pin-for-pin compatible with the CD4098B.



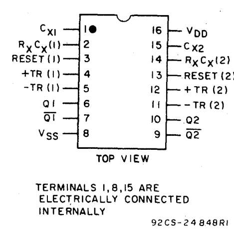
CD4538B Functional Diagram

- *Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C*
- *Noise margin (full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V*
- *5-V, 10-V, and 15-V parametric ratings*
- *Standardized, symmetrical output characteristics*
- *Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices."*

Applications:
- *Pulse delay and timing*
- *Pulse shaping*

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) .... −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT .... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D,F) .... Derate Linearly at 12 MW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) .... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D,F,H .... −55 to +125°C
PACKAGE TYPE E .... −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C



TERMINAL ASSIGNMENT

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operating is always within the following ranges:

CHARACTERISTIC	V_{DD} V	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	—	5	18	V

STATIC ELECTRICAL CHARACTERISTICS (Not Applicable to Pins 2 and 14)

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Pkgs. Values at −40, +25, +85 Apply to E Pkgs.							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current I_{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	—	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	—	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	—	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	—	
Output Voltage: Low-Level, V_{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	—	0,5	5	4.95				4.95	5	—	
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V_{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current, I_{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	$\pm 10^{-5}$	±0.1	μA

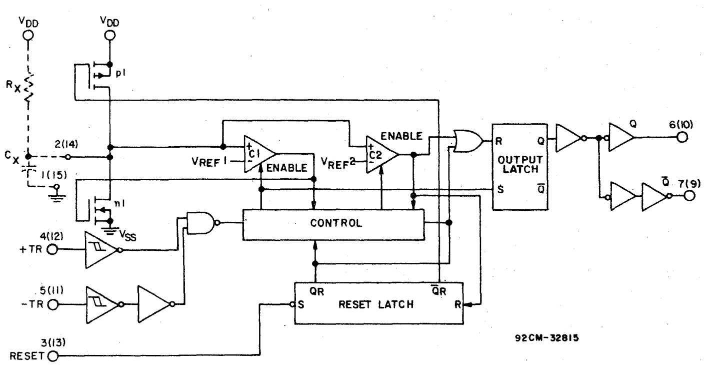


Fig. 1 — Logic diagram (½ of device shown).

DYNAMIC ELECTRICAL CHARACTERISTICS
At $T_A = 25$; Input $t_r, t_f = 20$ ns, $C_L = 50$ pF

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	LIMITS Typ.	UNITS
Transition Time	t_{TLH}, t_{THL}	5	100	ns
		10	50	
		15	40	
Propagation Delay Time: +TR or −TR to Q or $\bar{Q}$	t_{PLH}; t_{PHL}	5	300	
		10	150	
		15	100	
Reset to Q or $\bar{Q}$		5	250	
		10	125	
		15	95	
Minimum Input Pulse Width: +TR, −TR or Reset	t_{WH}, t_{WL}	5	35	
		10	30	
		15	25	
Output Pulse Width − Q or $\bar{Q}$: $C_X = 0.005\ \mu F$, $R_X = 10$ KΩ	T	5	58	μs
		10	55	
		15	55	
$C_X = 0.1\ \mu F$, $R_X = 100$ KΩ		5	9.86	ms
		10	10	
		15	10.14	
$C_X = 10\ \mu F$, $R_X = 100$ KΩ		5	0.965	s
		10	0.98	
		15	0.99	
Pulse Width Match between circuits in same package: $C_X = 0.1\ \mu F$, $R_X = 100$ KΩ	$\frac{100(T_1 - T_2)}{T_1}$	5	±1	%
		10	±1	
		15	±1	

TABLE I
CD4538B FUNCTIONAL TERMINAL CONNECTIONS

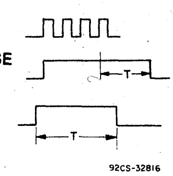
FUNCTION	V_{DD} TO TERM. NO.		V_{SS} TO TERM. NO.		INPUT PULSE TO TERM. NO.		OTHER CONNECTIONS	
	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$
Leading-Edge Trigger/ Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/Non-retriggerable	3	13			4	12	5-7	11-9
Trailing-Edge Trigger/ Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/Non-retriggerable	3	13			5	11	4-6	12-10

NOTES:
1. A RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS AN OUTPUT PULSE WIDTH WHICH IS EXTENDED ONE FULL TIME PERIOD (T) AFTER APPLICATION OF THE LAST TRIGGER PULSE.
2. A NON-RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS A TIME PERIOD (T) REFERENCED FROM THE APPLICATION OF THE FIRST TRIGGER PULSE.

INPUT PULSE TRAIN

RETRIGGERABLE MODE PULSE WIDTH (+TR MODE)

NON-RETRIGGERABLE MODE PULSE WIDTH (+TR MODE)



CD4555B, CD4556B Types

COS/MOS
Dual Binary to 1 of 4 Decoder/Demultiplexers

High-Voltage Types (20-Volt Rating)

CD4555B: Outputs High on Select
CD4556B: Outputs Low on Select

The RCA-CD4555B and CD4556B are dual one-of-four decoders/demultiplexers. Each decoder has two select inputs (A and B), an Enable input ($\overline{E}$), and four mutually exclusive outputs. On the CD4555B the outputs are high on select; on the CD4556B the outputs are low on select.

When the Enable input is high, the outputs of the CD4555B remain low and the outputs of the CD4556B remain high regardless of the state of the select inputs A and B. The CD4555B and CD4556B are similar to types MC14555 and MC14556, respectively.

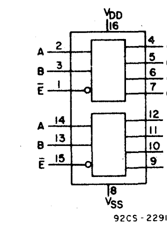
The CD4555B and CD4556B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

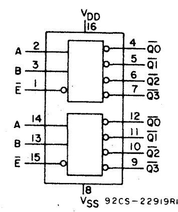
- **Expandable with multiple packages**
- **Standard, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Decoding**
- **Code conversion**
- **Demultiplexing (using Enable input as a data input)**
- **Memory chip-enable selection**
- **Function selection**



CD4555B FUNCTIONAL DIAGRAM



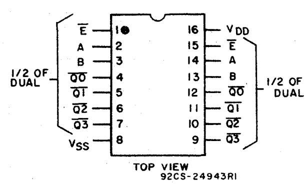
CD4556B FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

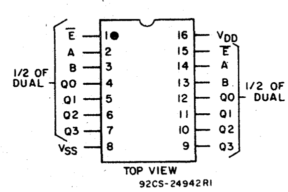
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD}	MIN.	MAX.	UNITS
Supply Voltage Range (For T_A = Full Package Temp. Range)	–	3	18	V

TERMINAL ASSIGNMENTS



CD4556B



CD4555B

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . –0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F,) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . –55 to +125°C
PACKAGE TYPE E . . . . –40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages Values at −40, +25, +85 Apply to E Package −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

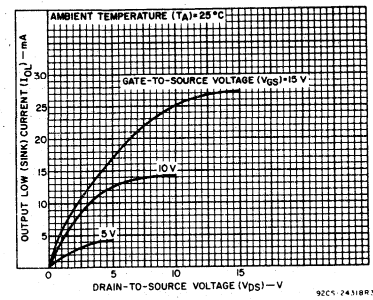


Fig. 1 — Typical output low (sink) current characteristics.

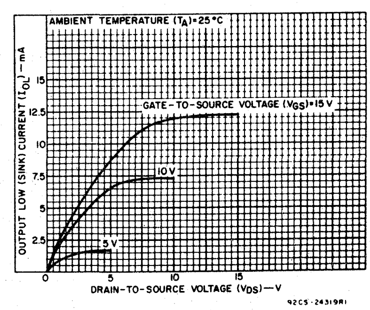


Fig. 2 — Minimum output low (sink) current characteristics.

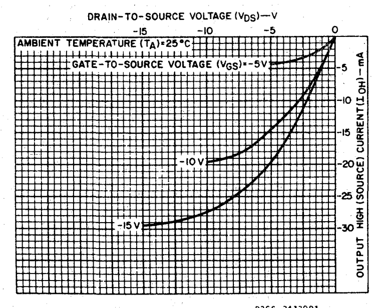


Fig. 3 — Typical output high (source) current characteristics.

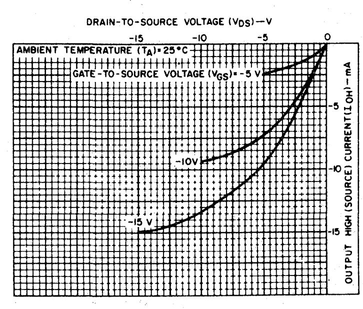


Fig. 4 — Minimum output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25°C$; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ*

CHARACTERISTIC	TEST CONDITIONS	V_{DD} Volts	ALL TYPES LIMITS TYP.	MAX.	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH} A or B Input to Any Output		5	220	440	ns
		10	95	190	
		15	70	140	
$\overline{E}$ Input to Any Output		5	200	400	ns
		10	85	170	
		15	65	130	
Transition Time t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance C_{IN}	Any Input		5	7.5	pF

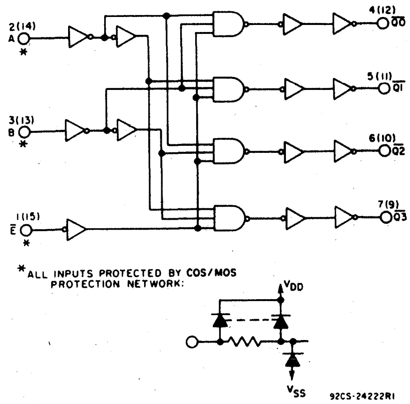


Fig. 5 – CD4556B logic diagram (1 of 2 identical circuits).

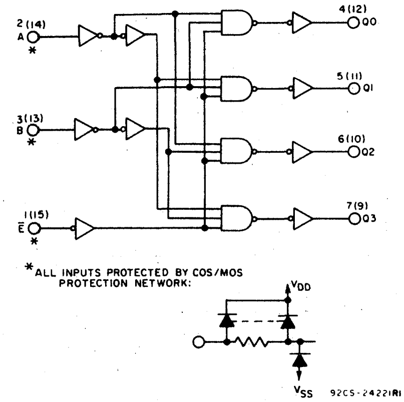


Fig. 6 – CD4555B logic diagram (1 of 2 identical circuits).

TRUTH TABLE

INPUTS ENABLE	SELECT		OUTPUTS CD4555B				OUTPUTS CD4556B			
Ē	B	A	Q3	Q2	Q1	Q0	Q̄3	Q̄2	Q̄1	Q̄0
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = DON'T CARE

LOGIC 1 ≡ HIGH
LOGIC 0 ≡ LOW

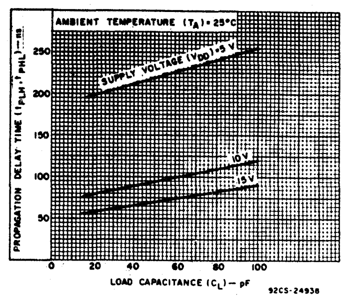


Fig. 7 – Typical propagation delay time vs. load capacitance (A or B input to any output).

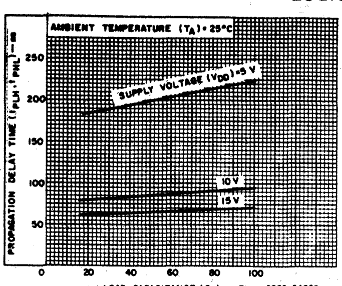


Fig. 8 – Typical propagation delay time vs. load capacitance (Ē input to any output).

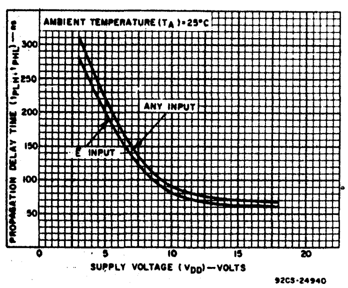


Fig. 9 – Typical propagation delay time vs. supply voltage.

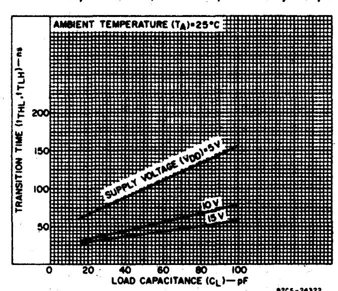


Fig. 10 – Typical transition time vs. load capacitance.

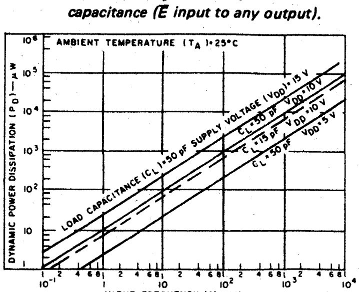


Fig. 11 – Typical dynamic power dissipation vs. frequency.

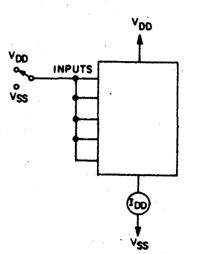


Fig. 12 – Quiescent device current test circuit.

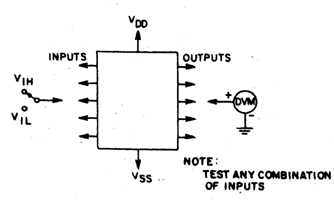


Fig. 13 – Input voltage test circuit.

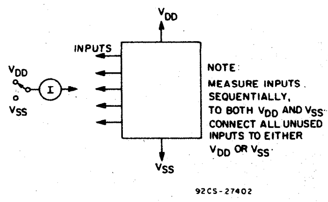


Fig. 14 – Input current test circuit.

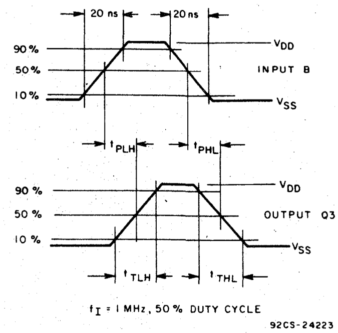


Fig. 15 – CD4555B B input to Q3 output dynamic signal waveforms.

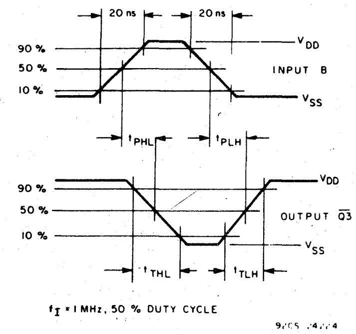


Fig. 16 – CD4556B B input to $\overline{Q3}$ output dynamic signal waveforms.

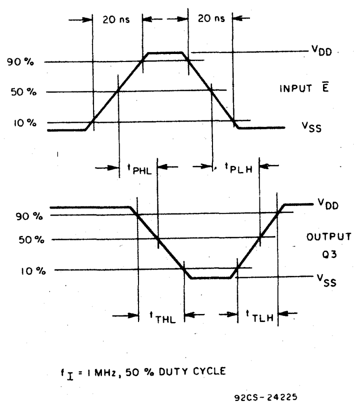


Fig. 17 – CD4555B $\overline{E}$ input to Q3 output dynamic signal waveforms.

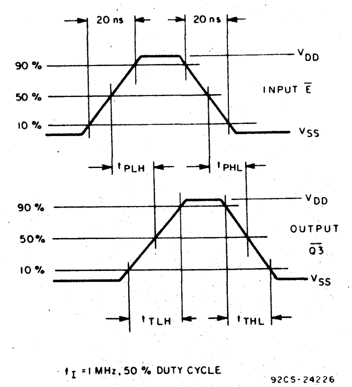
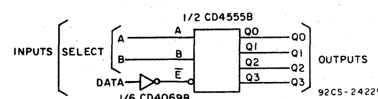


Fig. 18 – CD4556B $\overline{E}$ input to $\overline{Q}_3$ output dynamic signal waveforms.

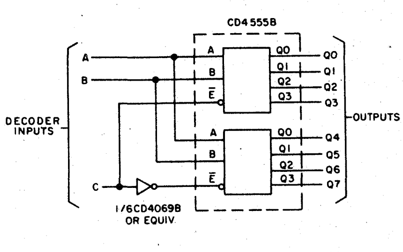
APPLICATIONS



TRUTH TABLE

SELECT INPUTS		OUTPUTS			
B	A	Q0	Q1	Q2	Q3
0	0	DATA	0	0	0
0	1	0	DATA	0	0
1	0	0	0	DATA	0
1	1	0	0	0	DATA

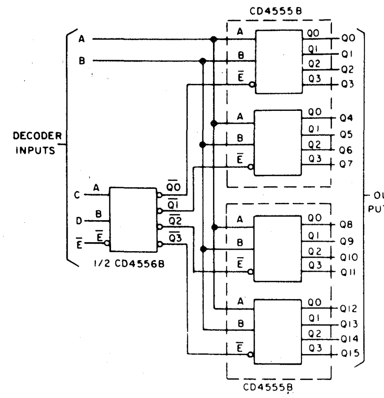
Fig. 19 – 1-of-4 line data demultiplexer using CD4555B.



TRUTH TABLE

INPUTS			Q OUTPUTS							
C	B	A	0	1	2	3	4	5	6	7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Fig. 20 – 1-of-8 decoder using CD4555B.



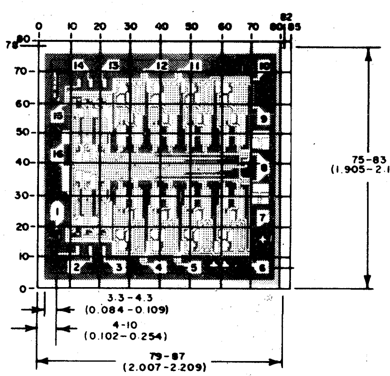
TRUTH TABLE

INPUTS					Q OUTPUTS															
E̅	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

X = don't care

92CS-24228

Fig. 21 — 1-of-16 decoder using CD4555B and CD4556B.



92CS-24922

DIMENSIONS AND PAD LAYOUT FOR CD4555BH. *(Dimensions and pad layout for CD4556BH are identical).*

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS 4-Bit Magnitude Comparator

High Voltage Types (20-Volt Rating)

The RCA-CD4585B is a 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to", or "greater than" a second 4-bit word.

The CD4585B has eight comparing inputs (A3, B3, through A0, B0), three outputs (A <B, A = B, A > B) and three cascading inputs (A < B, A = B, A > B) that permit systems designers to expand the comparator function to 8, 12, 16.......4N bits. When a single CD4585B is used, the cascading inputs are connected as follows: (A < B) = low, (A = B) = high, (A > B) = high.

Cascading these units for comparison of more than 4 bits is accomplished as shown in Fig. 13.

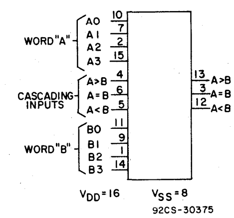
The CD4585B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix). This device is pin-compatible with low-power TTL type 7485 and the CMOS types MC14585 and 40085.

Features:

- **Expansion to 8,12,16......4N bits by cascading units**
- **Medium-speed operation:**
  compares two 4-bit words
  in 180 ns (typ.) at 10 V
- **100% tested for quiescent current at 20 V**
- **Standardized symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package temperature range)**
  range) = 1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Servo motor controls**
- **Process controllers**



FUNCTIONAL DIAGRAM

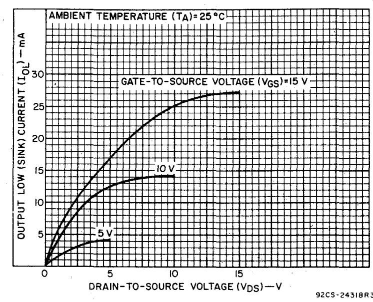


Fig.1 – Typical output low (sink) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

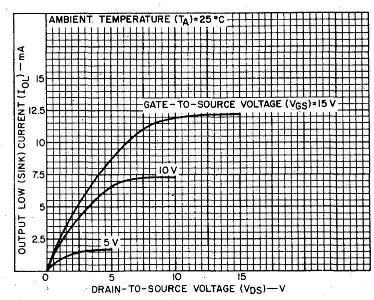


Fig.2 – Minimum output low (sink) current characteristics.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

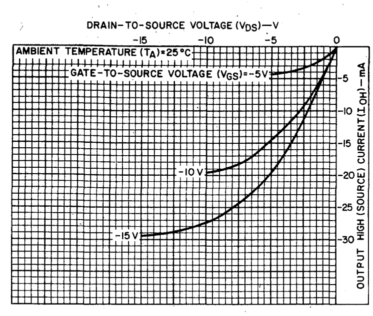


Fig.3 – Typical output high (source) current characteristics.

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A<B	A=B	A>B	A<B	A=B	A>B
A3 > B3	X	X	X	X	X	1	0	0	1
A3 = B3	A2 > B2	X	X	X	X	1	0	0	1
A3 = B3	A2 = B2	A1 > B1	X	X	X	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	X	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	X	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	1	0	0
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	1	0	0
A3 = B3	A2 < B2	X	X	X	X	X	1	0	0
A3 < B3	X	X	X	X	X	X	1	0	0

X = Don't Care Logic 1 = High Level Logic 0 = Low Level

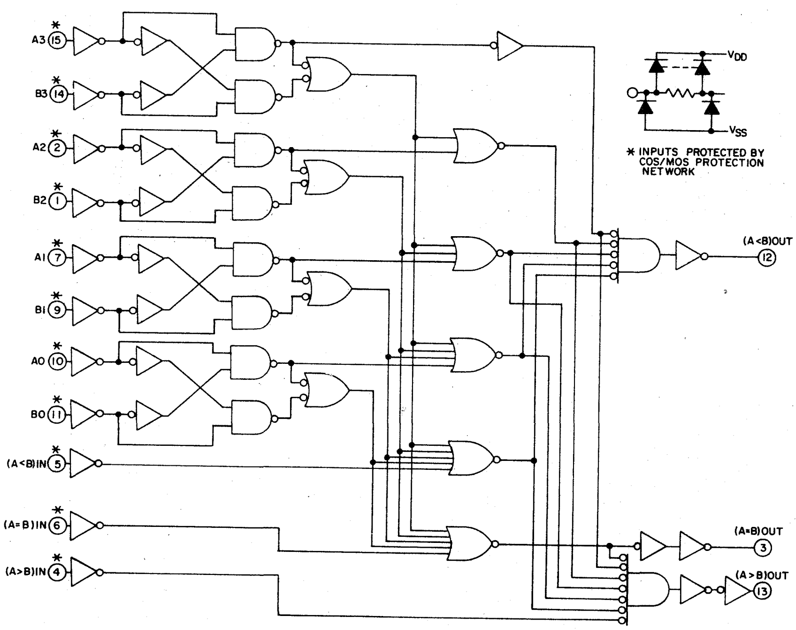
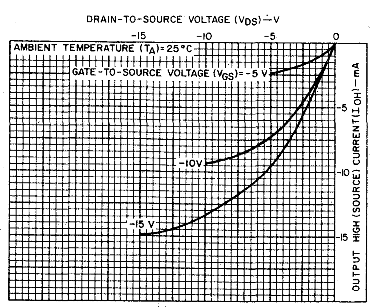
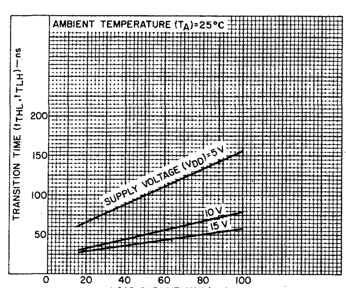


Fig.4 — Logic diagram. 92CL-31008



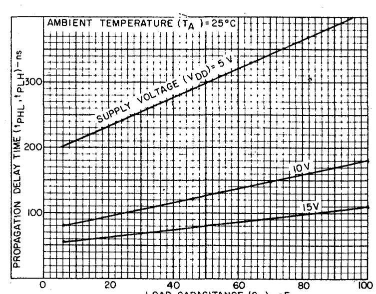
92CS-24321R2

Fig. 5 — Minimum output high (source) current characteristics.



92CS-24322

Fig. 6 — Typical transition time as a function of load capacitance.



92CS-32066

Fig. 7 — Typical propagation delay time ("comparing inputs" to outputs) as a function of load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS
At $T_A = 25°C$; Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} Volts	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time: Comparing Inputs to Outputs, t_{PHL}, t_{PLH}		5	300	600	ns
		10	125	250	
		15	80	160	
Cascading Inputs to Outputs, t_{PHL}, t_{PLH}		5	200	400	
		10	80	160	
		15	60	120	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

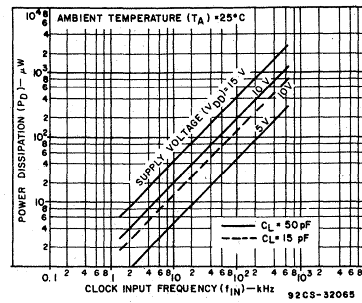


Fig. 8 — Typical dynamic power dissipation as a function of clock input frequency (see Fig. 9—dynamic power dissipation test circuit).

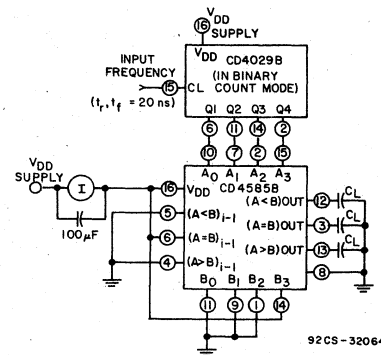


Fig. 9 — Dynamic power dissipation test circuit.

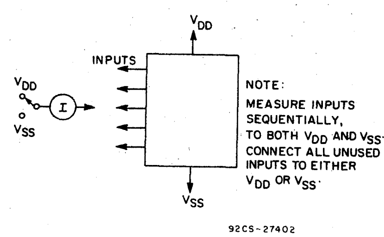


Fig. 10 — Input current test circuit.

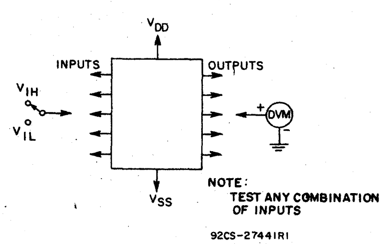


Fig. 11 — Input-voltage test circuit.

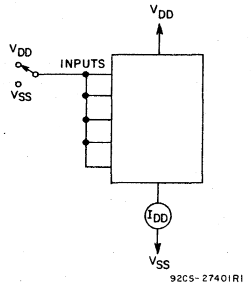
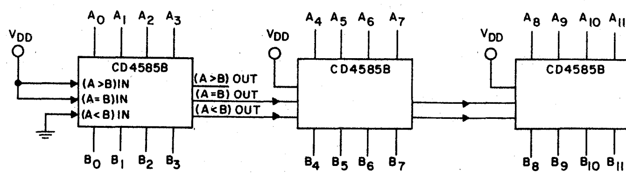


Fig. 12 — Quiescent-device-current test circuit.

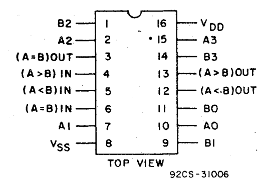


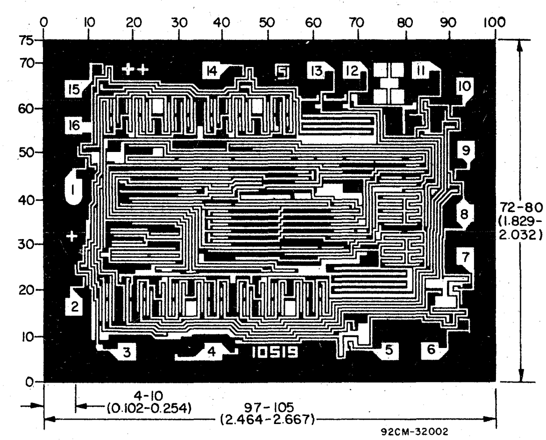
t_p TOTAL = t_p (COMPARE INPUTS) + 2 x t_p (CASCADE INPUTS), AT V_{DD} = 10V
(3 STAGES)

= 120+2(80) = 280 ns (TYP.)

Fig. 13 — Typical speed characteristics of a 12-bit comparator.

TERMINAL ASSIGNMENT





Dimensions and Pad Layout for CD4585BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS 8-Bit Addressable Latch

High-Voltage Types (20-Volt Rating)

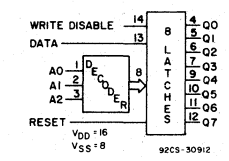
The RCA-CD4724B 8-bit addressable latch is a serial-input, parallel-output storage register that can perform a variety of functions.

Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when WRITE DISABLE is at a low level. When WRITE DISABLE is high, data entry is inhibited; however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs.

A master RESET input is available, which resets all bits to a logic "0" level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1-of-8 demultiplexer; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.

The CD4724B types are supplied in 16-lead hermetic ceramic dual-in-line packages (D and F suffixes), 16-lead plastic dual-in-line packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:
- **Serial data input**
- **Active parallel output**
- **Storage register capability**
- **Master clear**
- **Can function as demultiplexer**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V (full package-temperature range), 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) = 1 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM

Applications:
- **Multi-line decoders**
- **A/D converters**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

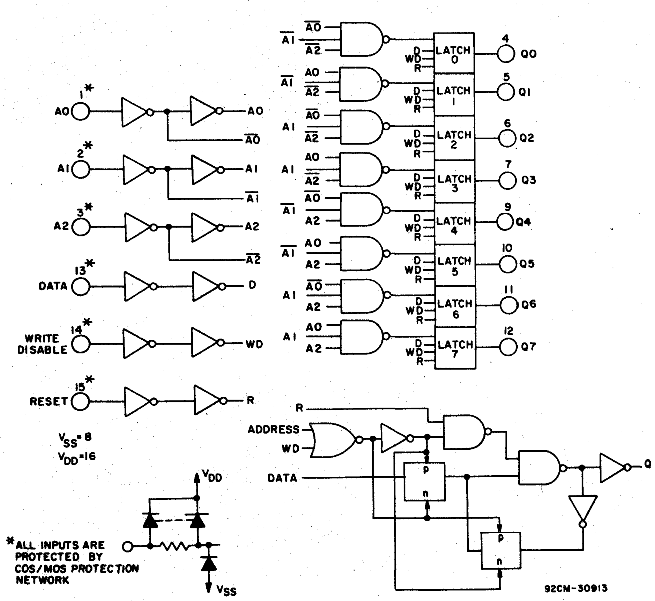
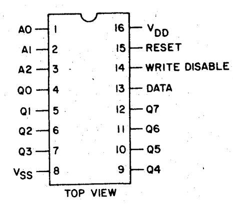


Fig. 1— Logic diagram of CD4724B and detail of 1 of 8 latches.



TERMINAL ASSIGNMENT

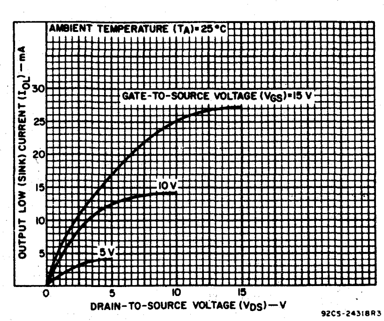


Fig. 2— Typical output low (sink) current characteristics.

RECOMMENDED OPERATING CONDITIONS *at T_A = 25° C (Unless otherwise specified)*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	SEE FIG. 15*	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply Voltage Range: (At T_A = Full Package Temperature Range)			3	18	V
Pulse Width, t_W Data	4	5	200	–	ns
		10	100	–	
		15	80		
Address	8	5	400	–	
		10	200	–	
		15	125	–	
Reset	5	5	150	–	
		10	75	–	
		15	50	–	
Setup Time, t_S Data to WRITE DISABLE	6	5	100	–	ns
		10	50	–	
		15	35	–	
Hold Time, t_H Data to WRITE DISABLE	7	5	150	–	ns
		10	75	–	
		15	50	–	

* Circled numbers refer to times indicated on master timing diagram.

Note: In addition to the above characteristics, a WRITE DISABLE ON time (the time that WRITE DISABLE is at a high level) must be observed during an address change for the total time that the external address lines A0, A1, and A2 are settling to a stable level, to prevent a wrong cell from being addressed.

MODE SELECTION			
WD	R	ADDRESSED LATCH	UNADDRESSED LATCH
0	0	Follows Data	Holds Previous State
0	1	Follows Data (Active High 8-Channel Demultiplexer)	Reset to "0"
1	0	Holds Previous State	
1	1	Reset to "0"	Reset to "0"

WD = WRITE DISABLE R = RESET

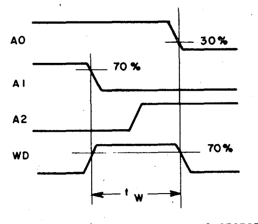


Fig. 3— Definition of WRITE DISABLE ON time.

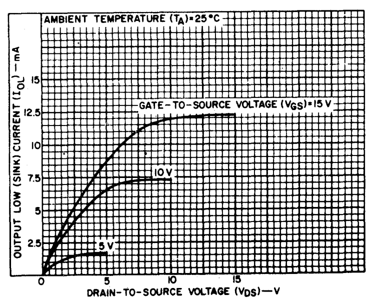


Fig. 4— Minimum output low (sink) current characteristics.

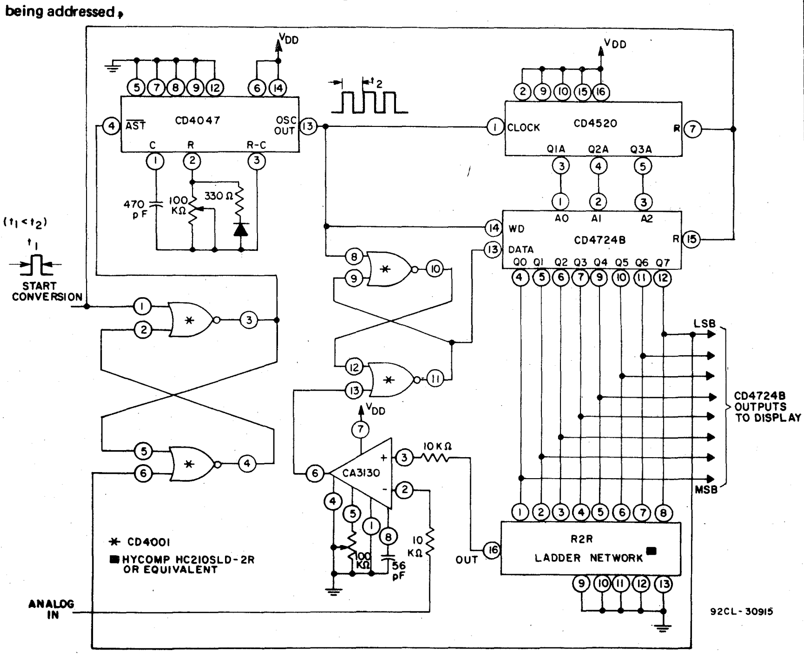


Fig. 5— A/D converter

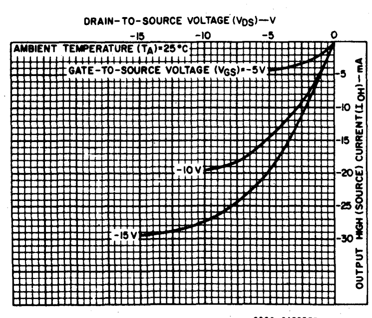
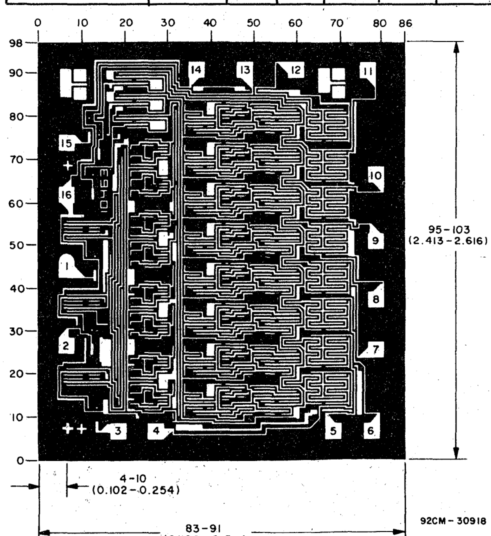


Fig.6 – Typical output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA



CD4724BH DIMENSIONS AND PAD LAYOUT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

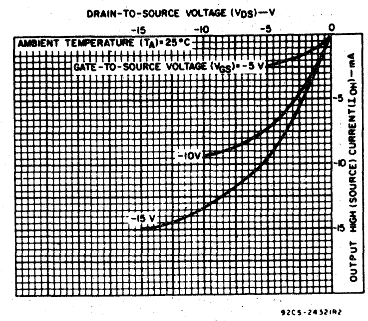


Fig.7 – Minimum output high (source) current characteristics.

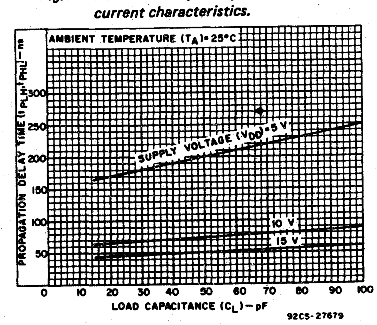


Fig. 8 – Typical propagation delay time (data to Qn) vs. load capacitance.

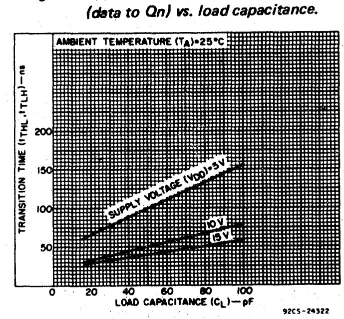


Fig. 9 – Typical transition time vs. load capacitance.

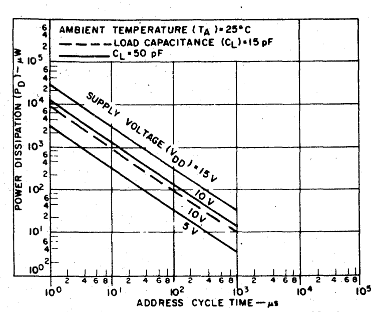


Fig.10 – Typical dynamic power dissipation vs. address cycle time.

CD4724B Types

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25°C$, $C_L = 50\,pF$, Input t_r, $t_f = 20\,ns$, $R_L = 200\,K\Omega$*

CHARACTERISTIC	CONDITIONS SEE Fig. 15*	CONDITIONS V_{DD} (V)	LIMITS ALL PACKAGE TYPES TYP.	LIMITS ALL PACKAGE TYPES MAX.	UNITS
Propagation Delay: t_{PLH}, t_{PHL} Data to Output,	①	5	200	400	ns
		10	75	150	
		15	50	100	
WRITE DISABLE to Output, t_{PLH}, t_{PHL}	②	5	200	400	
		10	80	160	
		15	60	120	
Reset to Output, t_{PHL}	③	5	175	350	
		10	80	160	
		15	65	130	
Address to Output, t_{PLH}, t_{PHL}	⑨	5	225	450	
		10	100	200	
		15	75	150	
Transition Time, t_{THL}, t_{TLH} (Any Output)		5	100	200	ns
		10	50	100	
		15	40	80	
Minimum Pulse Width, t_W Data	④	5	100	200	ns
		10	50	100	
		15	40	80	
Address	⑧	5	200	400	ns
		10	100	200	
		15	65	125	
Reset	⑤	5	75	150	ns
		10	40	75	
		15	25	50	
Minimum Setup Time, t_S Data to WRITE DISABLE	⑥	5	50	100	ns
		10	25	50	
		15	20	35	
Minimum Hold Time, t_H Data to WRITE DISABLE	⑦	5	75	150	ns
		10	40	75	
		15	25	50	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

*Circled numbers refer to times indicated on master timing diagram.

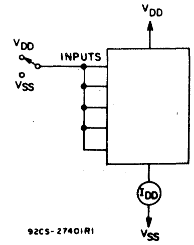


Fig. 11— Quiescent device current test circuit.

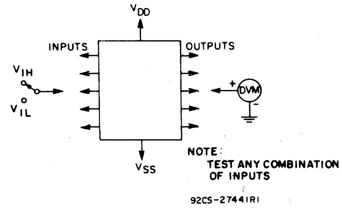


Fig. 12— Input voltage test circuit.

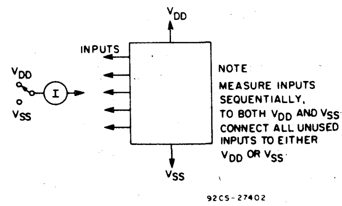


Fig. 13— Input current test circuit.

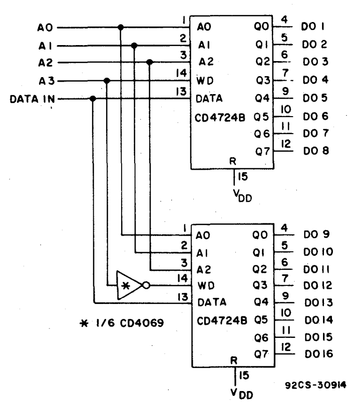


Fig. 14— 1 of 16 decoder/demultiplexer.

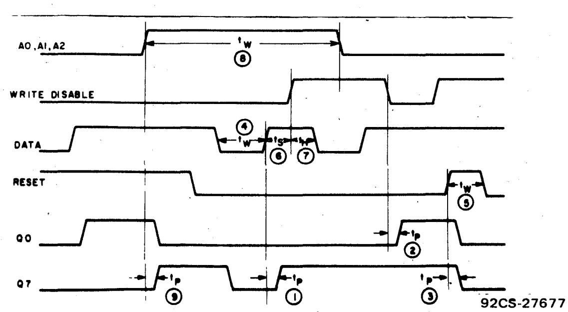


Fig. 15— Master timing diagram.

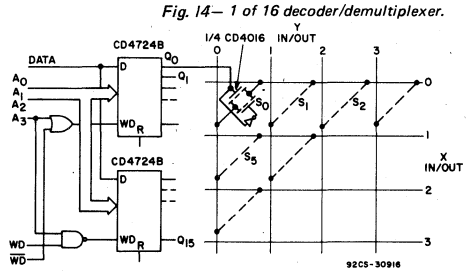


Fig 16— Multiple selection decoding — 4 x 4 crosspoint switch.

COS/MOS 32-Stage Static Left/Right Shift Register

The RCA-CD40100B is a 32-stage shift register containing 32 D-type master-slave flip-flops.

The data present at the SHIFT-RIGHT INPUT is transferred into the first register stage synchronously with the positive CLOCK edge, provided the LEFT/RIGHT CONTROL is at a low level, the RECIRCULATE CONTROL is at a high level, and the CLOCK INHIBIT is low. If the LEFT/RIGHT CONTROL is at a high level and the RECIRCULATE CONTROL is also high, data at the SHIFT-LEFT INPUT is transferred into the 32nd register stage synchronously with the positive CLOCK transition, provided the CLOCK INHIBIT is low. The state of the LEFT/RIGHT CONTROL, RECIRCULATE CONTROL, and CLOCK INHIBIT should not be changed when the CLOCK is high.

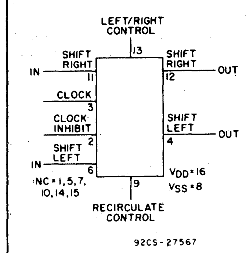
Data is shifted one stage left or one stage right depending on the state of the LEFT/RIGHT CONTROL, synchronously with the positive CLOCK edge. Data clocked into the first or 32nd register states is available at the SHIFT-LEFT or SHIFT-RIGHT OUTPUT respectively, on the next negative CLOCK transition (see Data Transfer Table). No shifting occurs on the positive CLOCK edge if the CLOCK INHIBIT line is at a high level. With the RECIRCULATE CONTROL low, data in the 32nd stage is shifted into the first stage when the LEFT/RIGHT CONTROL is low and from the 1st stage to the 32nd stage when the LEFT/RIGHT CONTROL is high.

The CD40100B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

High-Voltage Types (20-Volt Rating)

Features:

- **Fully static operation**
- **Shift left/Shift right capability**
- **Multiple package cascading**
- **Recirculate capability**
- **LIFO or FIFO capability**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) =**
  - **1 V at V_{DD} = 5 V**
  - **2 V at V_{DD} = 10 V**
  - **2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM

Applications:

- **Serial shift registers**
- **Time delay circuits**
- **Expandable N-bit data storage stack (LIFO operation)**

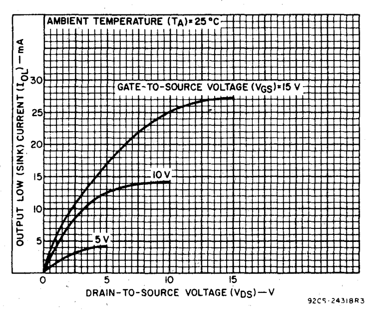


Fig. 1 – Typical output low (sink) current characteristics.

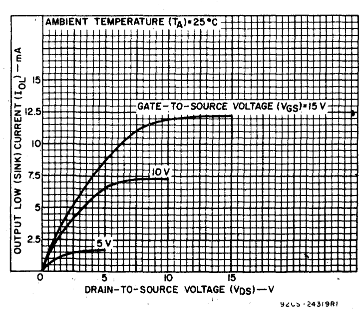


Fig. 2 – Minimum output low (sink) current characteristics.

MAXIMUM RATINGS, ***Absolute-Maximum Values:***

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltages referenced to V_{SS} Terminal)	**−0.5 to +20 V**
INPUT VOLTAGE RANGE, ALL INPUTS	**−0.5 to V_{DD} +0.5 V**
DC INPUT CURRENT, ANY ONE INPUT	**±10 mA**
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	**500 mW**
For T_A = +60 to +85°C (PACKAGE TYPE E)	**Derate Linearly at 12 mW/°C to 200 mW**
For T_A = −55 to +100°C (PACKAGE TYPES D,F)	**500 mW**
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	**Derate Linearly at 12 mW/°C to 200 mW**
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	**100 mW**
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	**−55 to +125°C**
PACKAGE TYPE E	**−40 to +85°C**
STORAGE TEMPERATURE RANGE (T_{stg})	**−65 to +150°C**
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	**+265°C**

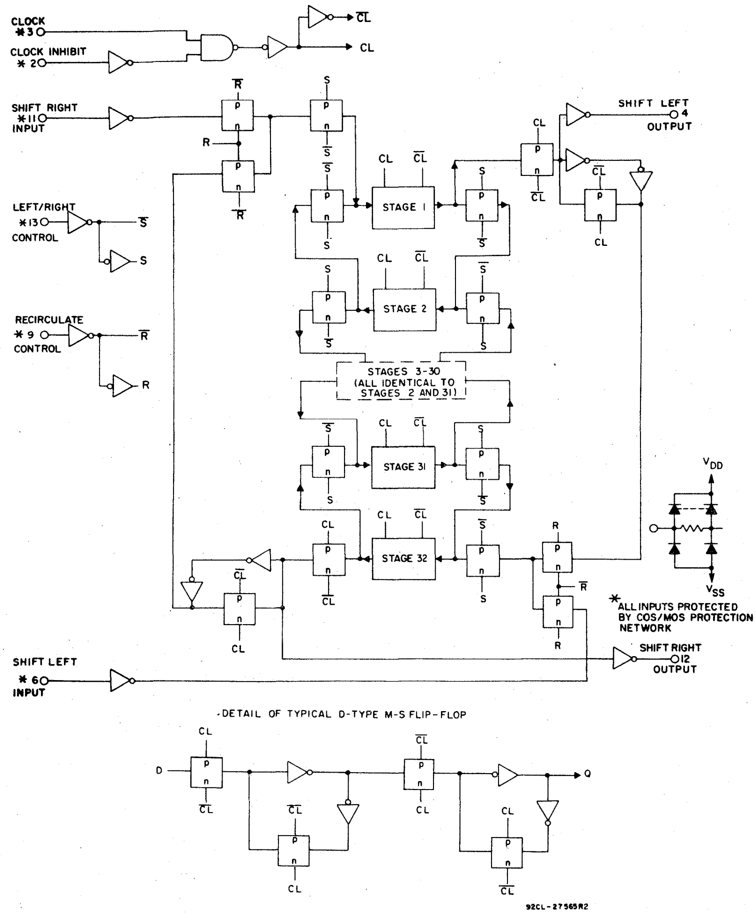


Fig. 3 – Logic diagram.

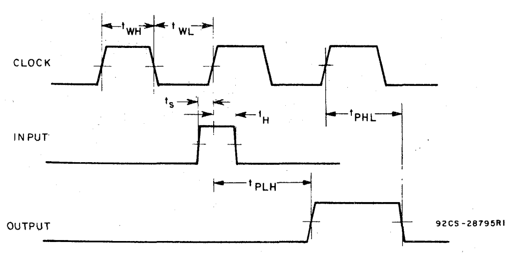


Fig. 4 – Timing diagram defining setup, hold, and propagation delay times.

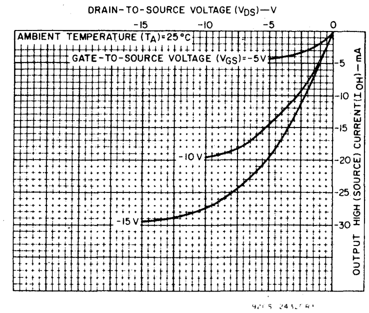


Fig. 5 – Typical output high (source) current characteristics.

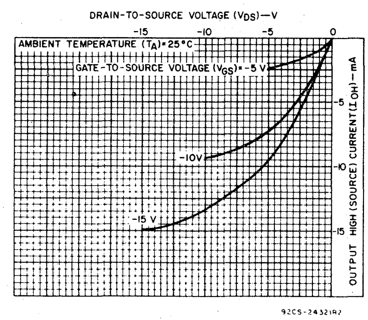


Fig. 6 – Minimum output high (source) current characteristics.

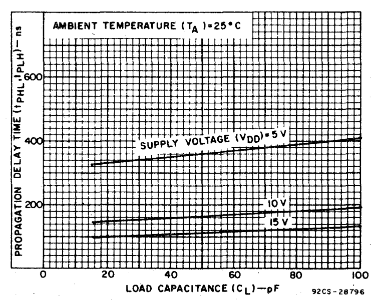


Fig. 7 – Typical propagation delay time (CLOCK to SHIFT LEFT/RIGHT) as a function of load capacitance.

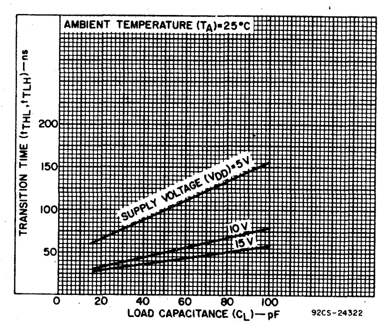


Fig. 8 – Typical transition time as a function of load capacitance.

RECOMMENDED OPERATING CONTITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5 10 15	100 20 10	– – –	ns
Data Hold Time, t_H	5 10 15	275 100 75	– – –	ns
Clock Input Frequency, f_{CL}	5 10 15	dc	1 2.5 3	mHz
Clock Input Rise or Fall Time, t_rCL, t_fCL	5 10 15	– – –	15 15 15	µs
Clock Input Pulse Width: Low Level, t_{WL}	5 10 15	450 230 190	– – –	ns
High Level, t_{WH}	5 10 15	280 150 140	– – –	ns

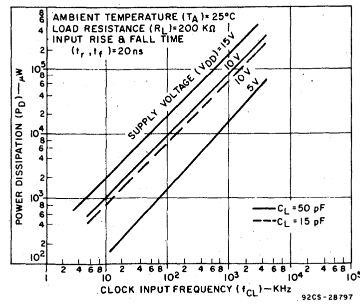


Fig. 9 – Typical dynamic power dissipation as a function of CLOCK frequency.

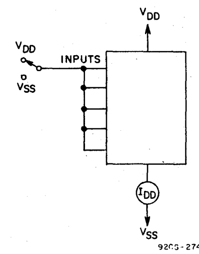


Fig. 10 – Quiescent-device-current test circuit.

CONTROL TRUTH TABLE

LEFT/RIGHT CONTROL	CLOCK INHIBIT	RECIRCULATE CONTROL	ACTION	INPUT BIT ORIGIN
1	0	1	Shift left	Shift left input
1	0	0	Shift left	Stage 1
0	0	1	Shift right	Shift right input
0	0	0	Shift right	Stage 32
X	1	X	No shift	–

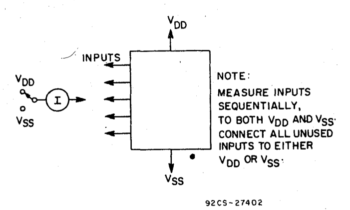


Fig. 11 – Input-current test circuit.

DATA TRANSFER TABLE*

INITIAL STATE DATA INPUT	CLOCK INHIBIT	INTERNAL STAGE	CLOCK LEVEL CHANGE	RESULTING STATE INTERNAL STAGE Q	OUTPUT
0	0	X	_/‾	0	NC
X	0	0	‾_	NC	0
1	0	X	_/‾	1	NC
X	0	1	‾_	NC	1
X	1	1	X	NC	NC

0 = Low level   1 = High level   X = Don't care   NC = No change

* For Shift-Right Mode
Data Input = SHIFT-RIGHT INPUT (Term. 11)
Internal Stage = Stage 1 (Q_1)
Output = SHIFT-LEFT OUTPUT (Term. 4)

For Shift-Left Mode
Data Input = SHIFT-LEFT INPUT (Term. 6)
Internal Stage = Stage 32 (Q_{32})
Output = SHIFT-RIGHT OUTPUT (Term. 12)

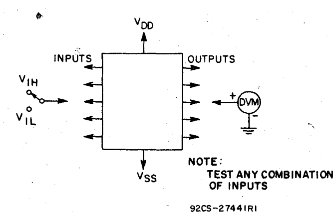
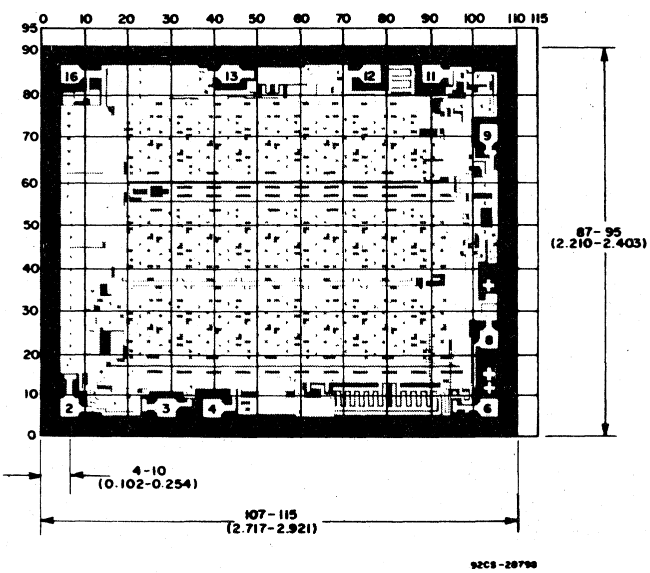


Fig. 12 – Input-voltage test circuit.

CD40100B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER-ISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages Values at –40, +25, +85 Apply to E Package –55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				–	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA



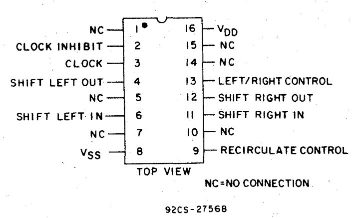
Dimensions and pad layout for CD40100BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
		V_{DD} V	Min.	Typ.	Max.	
Propagation Delay Time: Clock to Shift Left/Right Output, t_{PLH}, t_{PHL}		5		360	720	ns
		10		165	330	
		15		115	230	
Transition Time, t_{THL}, t_{TLH}		5		100	200	ns
		10		50	100	
		15		40	80	
Minimum Data Setup Time, t_S		5		50	100	ns
		10		10	20	
		15		5	10	
Minimum Data Hold Time, t_H		5		170	275	ns
		10		75	100	
		15		50	75	
Maximum Clock Input Frequency, f_{CL}		5	1	2		MHz
		10	2.5	5		
		15	3	6		
Minimum Clock Input Pulse Width: Low Level, t_{WL}		5		225	450	ns
		10		115	230	
		15		95	190	
High Level, t_{WH}		5		140	280	ns
		10		75	150	
		15		70	140	
Input Capacitance, C_{IN}	Any Input	–		5	7.5	pF



TERMINAL ASSIGNMENT

CD40101B Types

COS/MOS 9-Bit Parity Generator/Checker

High-Voltage Types (20-Volt Rating)

The RCA-CD40101B is a 9-bit (8 data bits plus 1 parity bit) parity generator/checker. It may be used to detect errors in data transmission or data retrieval. Odd and even outputs facilitate odd or even parity generation and checking.

When used as a parity generator, a parity bit is supplied along with the data to generate an even or odd parity output.

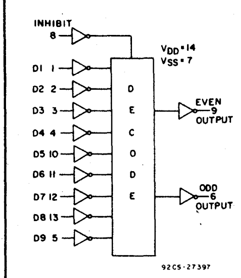
When used as a parity checker, the received data bits and parity bits are compared for correct parity. The even or odd outputs are used to indicate an error in the received data.

Word-length capability is expandable by cascading. The CD40101B is also provided with an inhibit control. If the inhibit control is set at logical "1", the even and odd outputs go to a logical "0".

The CD40101B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **100% tested for maximum quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics**
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of 'B' Series CMOS Devices."**

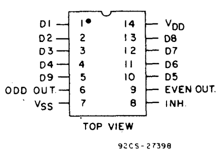


FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	–0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	–55 to +125°C
PACKAGE TYPE E	–40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	–65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

TERMINAL ASSIGNMENT



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

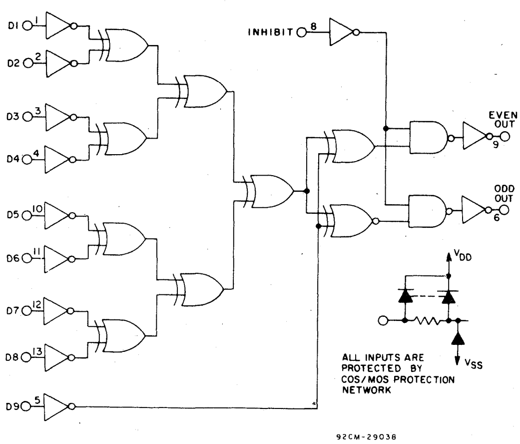


Fig.1 – CD40101B logic diagram.

Truth Table

Inputs		Outputs	
D1-D9	Inhibit	Even	Odd
Σ 1's=Even	0	1	0
Σ 1's=Odd	0	0	1
X	1	0	0

X = Don't Care
Logic 1 = High
Logic 0 = Low

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	µA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	µA

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS Typ.	LIMITS Max.	UNITS
Data Propagation Delay Time, t_{PHL}, t_{PLH}		5	350	700	ns
		10	150	300	
		15	100	200	
Inhibit-to-Output Propagation Delay Time, t_{PHL}, t_{PLH}		5	140	280	
		10	70	140	
		15	50	100	
Transition Time, t_{THL}, t_{TLH}		5	100	200	
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

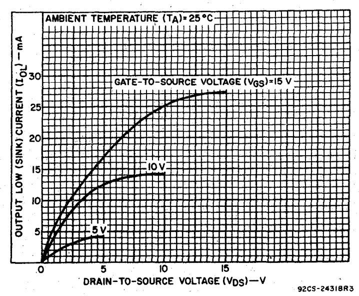


Fig.2 – Typical output low (sink) current characteristics.

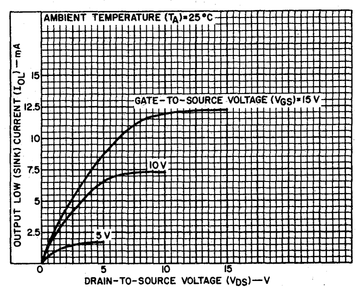


Fig.3 – Minimum output low (sink) current characteristics.

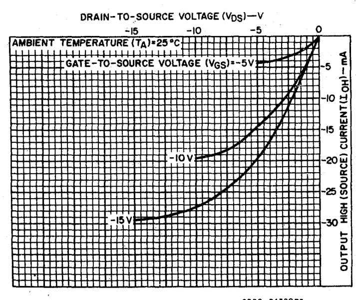


Fig.4 – Typical output high (source) current characteristics.

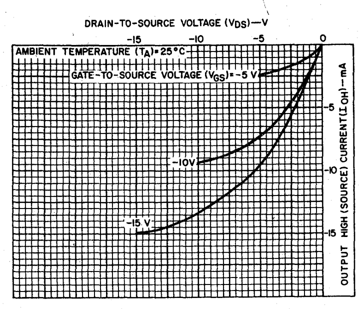


Fig.5 – Minimum output high (source) current characteristics.

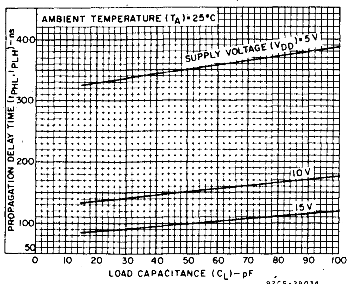


Fig.6 – Typical propagation delay time as a function of load capacitance.

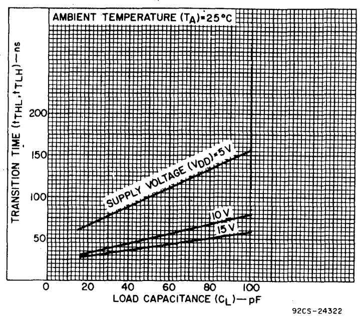


Fig. 7 – Typical transition time as a function of load capacitance.

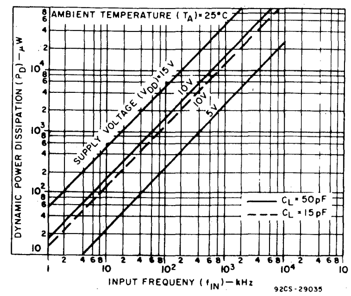


Fig. 8 – Typical dynamic power dissipation as a function of input frequency.

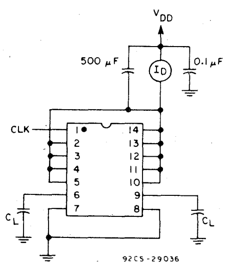


Fig.9 – Dynamic power dissipation test circuit.

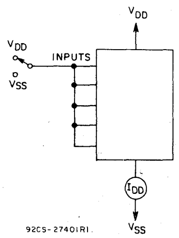


Fig. 10 – Quiescent-device-current test circuit.

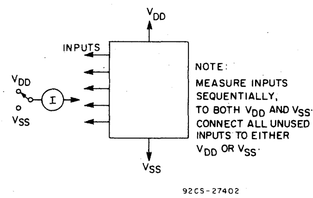


Fig. 11 – Input-leakage current.

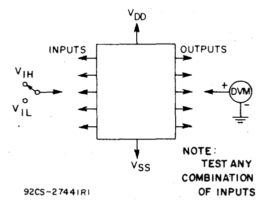
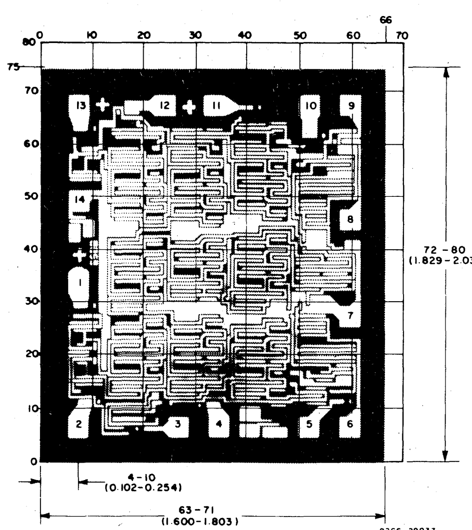


Fig. 12 – Input-voltage test circuit.

DIMENSIONS AND PAD LAYOUT FOR CD40101B



The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

COS/MOS 8-Stage Presettable Synchronous Down Counters

High-Voltage Types (20-Volt Rating)

CD40102B – 2-Decade BCD Type
CD40103B – 8-Bit Binary Type

The RCA-CD40102B, and CD40103B consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The CD40102B is configured as two cascaded 4-bit BCD counters, and the CD40103B contains a single 8-bit binary counter. Each type has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the CARRY-OUT/ZERO-DETECT output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the CLOCK. Counting is inhibited when the CARRY-IN/COUNTER ENABLE ($\overline{CI/CE}$) input is high. The CARRY-OUT/ZERO-DETECT ($\overline{CO/ZD}$) output goes low when the count reaches zero if the $\overline{CI/CE}$ input is low, and remains low for one full clock period.

When the SYNCHRONOUS PRESET-ENABLE ($\overline{SPE}$) input is low, data at the JAM input is clocked into the counter on the next positive clock transition regardless of the state of the $\overline{CI/CE}$ input. When the ASYNCHRONOUS PRESET-ENABLE ($\overline{APE}$) input is low, data at the JAM inputs is asynchronously forced into the counter regardless of the state of the $\overline{SPE}$, $\overline{CI/CE}$, or CLOCK inputs. JAM inputs J0-J7 represent two 4-bit BCD words for the CD40102B and a single 8-bit binary word for the CD40103B.

When the CLEAR ($\overline{CLR}$) input is low, the counter is asynchronously cleared to its maximum count (99_{10} for the CD40102B and 255_{10} for the CD40103B) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table.

If all control inputs are high at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 or 256 clock pulses long.

The CD40102B and CD40103B may be cascaded using the $\overline{CI/CE}$ input and the $\overline{CO/ZD}$ output, in either a synchronous or ripple mode as shown in Figs.21 and 22.

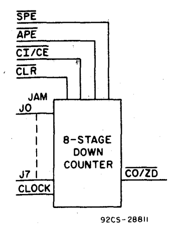
The CD40102B and CD40103B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Synchronous or asynchronous preset**
- **Medium-speed operation: f_{CL} = 3.6 MHz (typ.) @ V_{DD} = 10 V**
- **Cascadable**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) = 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V**
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Divide-by-"N" counters**
- **Programmable timers**
- **Interrupt timers**
- **Cycle/program counter**



CD40102B, CD40103B FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS AT T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	LIMITS		Units
		Min.	Max.	
Supply Voltage Range (At T_A = Full Package-Temperature Range)		3	18	V
Clock Pulse Width, t_W	5	300	–	ns
	10	180	–	
	15	80	–	
$\overline{Clear}$ Pulse Width, t_W	5	320	–	ns
	10	160	–	
	15	100	–	
$\overline{APE}$ Pulse Width, t_W	5	360	–	ns
	10	160	–	
	15	120	–	
Clock Input Frequency, f_{CL}	5	–	0.7	MHz
	10	–	1.8	
	15	–	2.4	
Clock Rise and Fall Time, t_rCL, t_fCL	5	–	15	μs
	10	–		
	15	–		
$\overline{SPE}$ Setup Time, t_{SU}	5	280	–	ns
	10	140	–	
	15	100	–	
Jam Setup Time, t_{SU}	5	200	–	ns
	10	80	–	
	15	60	–	
$\overline{CI/CE}$ Setup Time, t_{SU}	5	500	–	ns
	10	250	–	
	15	150	–	

CD40102B, CD40103B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F,) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F,) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

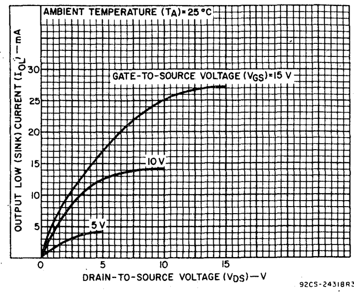


Fig. 1 — Typical output low (sink) current characteristics.

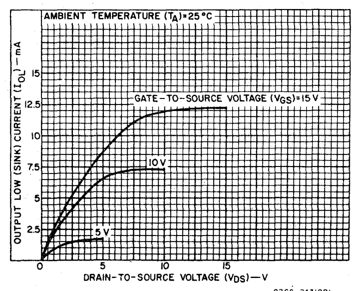


Fig. 2 — Minimum output low (sink) current characteristics.

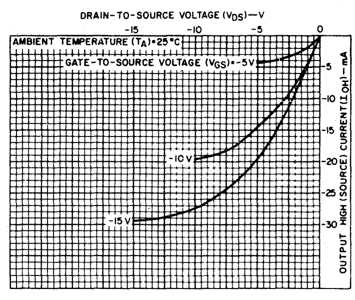


Fig. 3 — Typical output high (source) current characteristics.

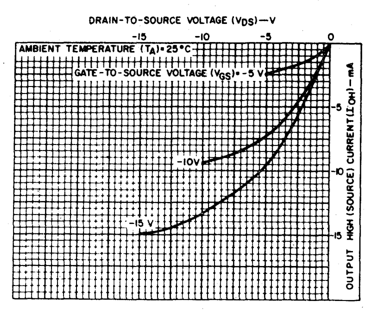


Fig. 4 — Minimum output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages; Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, $C_L = 50$ pF, Input t_r, $t_f = 20$ ns, $R_L = 200$ kΩ

Characteristic	Conditions V_{DD} (V)	Limits All Packages Min.	Typ.	Max.	Units
Propagation Delay Time (t_{PHL}, t_{PLH}): Clock-to-Output (See Fig.10)	5	–	300	600	ns
	10	–	130	260	
	15	–	95	190	
Carry In/Counter Enable-to-Output	5	–	200	400	
	10	–	90	180	
	15	–	65	130	
Asynchronous Preset Enable-to-Output	5	–	650	1300	
	10	–	300	600	
	15	–	200	400	
$\overline{Clear}$-to-Output	5	–	375	750	
	10	–	180	360	
	15	–	100	200	
Transition Time (t_{THL}, t_{TLH})	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Minimum Clock Pulse Width, (t_W)	5	–	150	300	ns
	10	–	90	180	
	15	–	40	80	
Minimum $\overline{CLR}$ Pulse Width (t_W)	5	–	160	320	
	10	–	80	160	
	15	–	50	100	
Minimum $\overline{APE}$ Pulse Width (t_W)	5	–	180	360	
	10	–	80	160	
	15	–	60	120	
Minimum $\overline{SPE}$ Set-Up Time (t_{SU})	5	–	140	280	
	10	–	70	140	
	15	–	50	100	
Minimum $\overline{CI/CE}$ Setup Time (t_{SU})	5	–	250	500	
	10	–	125	250	
	15	–	75	150	
Minimum JAM Set-Up Time (t_{SU})	5	–	100	200	
	10	–	40	80	
	15	–	30	60	
Maximum Clock Input Frequency (f_{CL}) (See Fig.11)	5	0.7	1.4	–	MHz
	10	1.8	3.6	–	
	15	2.4	4.8	–	
Input Capacitance (C_{IN})		–	5	7.5	pF

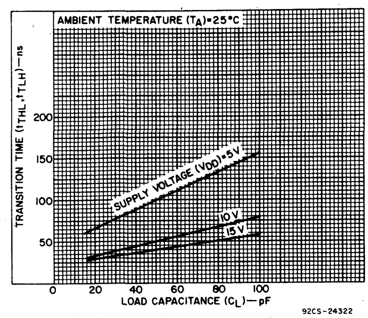


Fig. 5 — Typical transition time as a function of load capacitance.

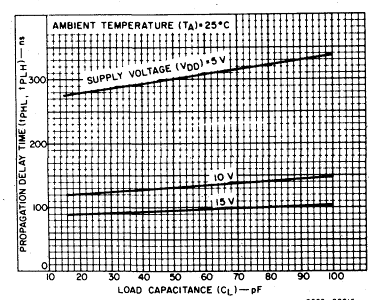


Fig. 6 — Typical propagation delay time as a function of load capacitance (clock to CO/ZD).

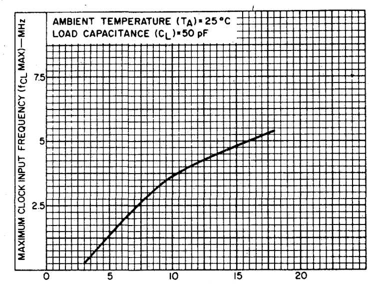


Fig. 7 — Typical maximum clock input frequency as a function of supply voltage.

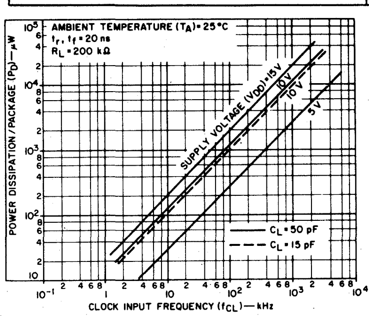


Fig. 8 — Typical dynamic power dissipation as a function of frequency.

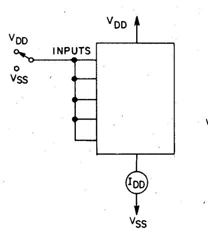


Fig. 9 — Quiescent device current test circuit.

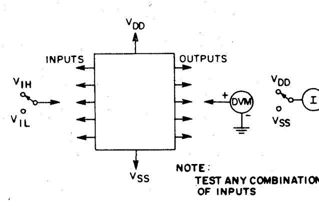


Fig. 10 — Input voltage test circuit.

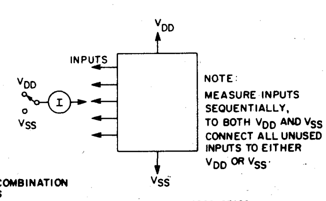


Fig. 11 — Input current test circuit.

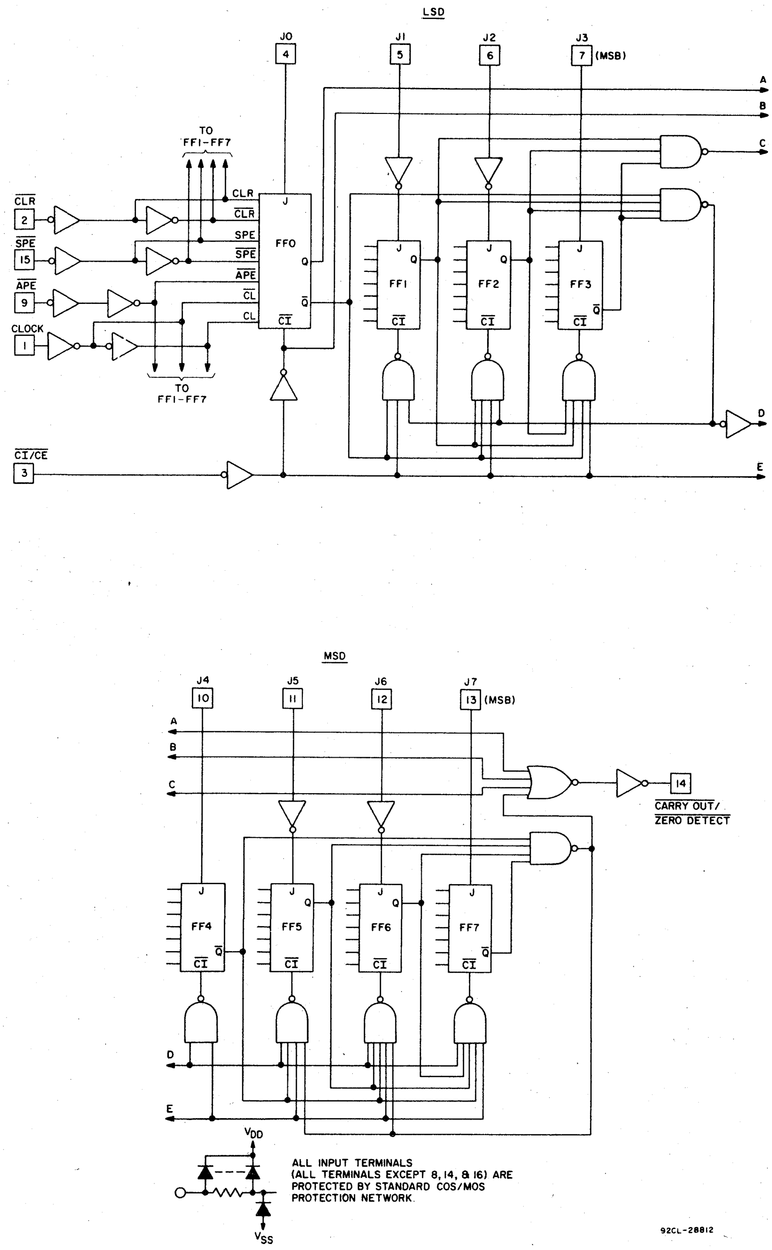


Fig. 12 – Logic diagram for CD40102B.

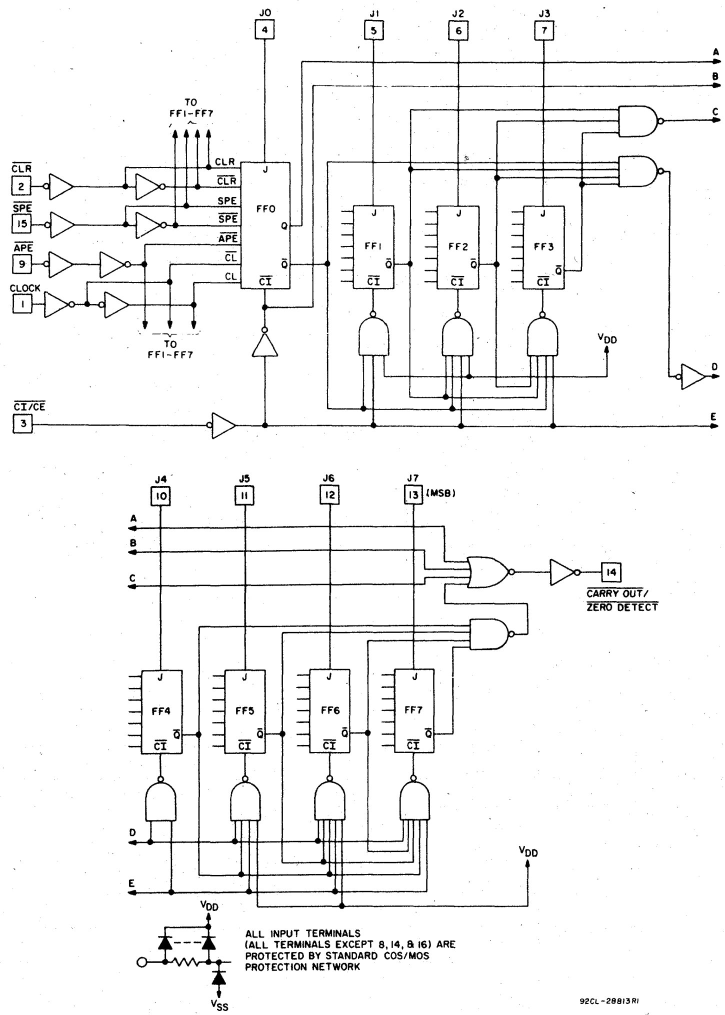


Fig. 13 — Logic diagram for CD40103B.

TRUTH TABLE

CONTROL INPUTS				PRESET MODE	ACTION
$\overline{CLR}$	$\overline{APE}$	$\overline{SPE}$	$\overline{CI}/\overline{CE}$		
1	1	1	1	Synchronous	Inhibit counter
1	1	1	0		Count down
1	1	0	X		Preset on next positive clock transition
1	0	X	X	Asynchronous	Preset asynchronously
0	X	X	X		Clear to maximum count

Notes: 1. 0 = Low level
1 = High level
X = Don't care

2. Clock connected to clock input
3. Synchronous operation: changes occur on negative-to-positive clock transitions
4. JAM inputs: CD40102B BCD; MSD = J7,J6,J5,J4 (J7 is MSB)
LSD = J3,J2,J1,J0 (J3 is MSB)
CD40103B Binary; MSB = J7, LSB = J0

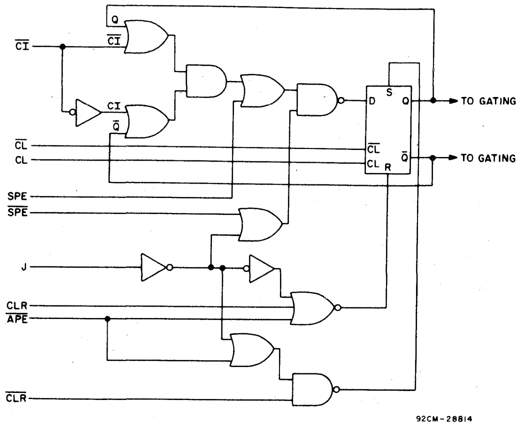


Fig. 14 – Detail logic diagram for flip-flops, FFO – FF7, used in logic diagrams for CD40102B and CD40103B.

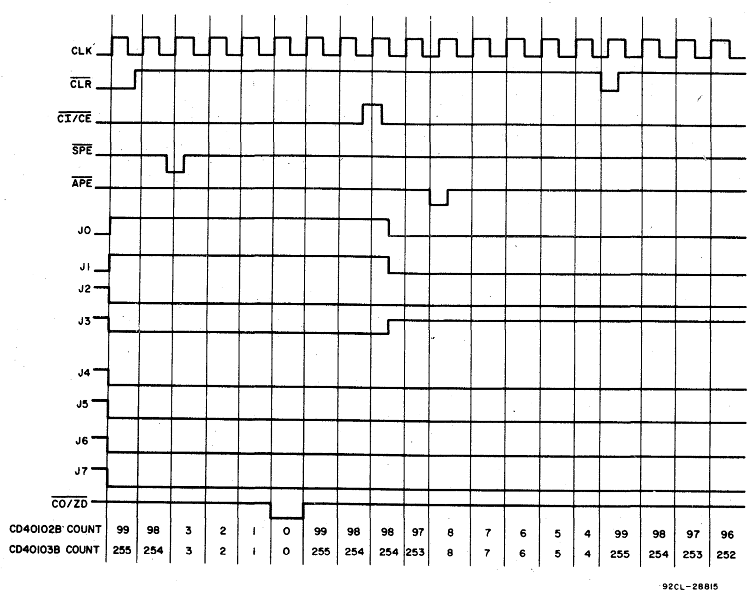
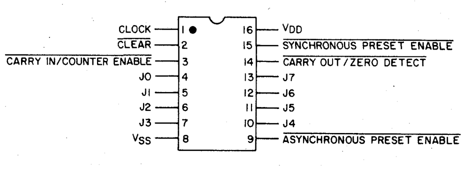


Fig. 15 – Timing diagram for CD40102B and CD40103B.



CD40102B, CD40103B TERMINAL ASSIGNMENT

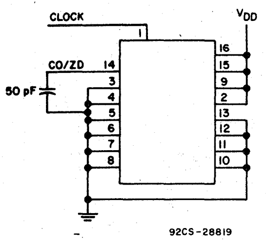


Fig.16 – Maximum clock frequency test circuit.

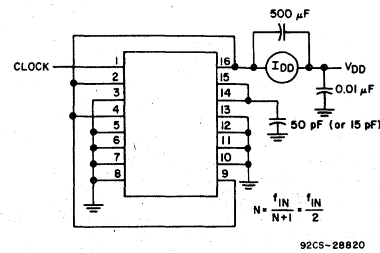


Fig.17 – Dynamic power dissipation test circuit (÷2 mode).

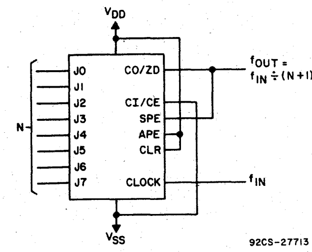


Fig.18 – Divide-by-"N" counter.

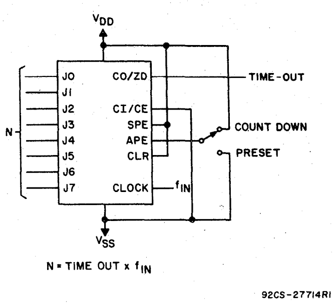


Fig.19 – Programmable timer.

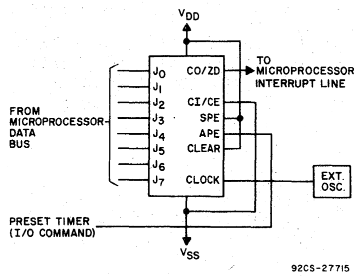
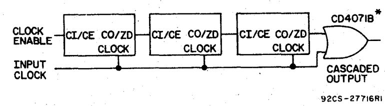


Fig.20 – Microprocessor interrupt timer.



* An output spike (160 ns @ V_{DD} = 5 V) occurs whenever two or more devices are cascaded in the parallel-clocked mode because the clock-to-carry out delay is greater than the carry-in-to-carry out delay. This spike is eliminated by gating the output of the last device with the clock as shown.

Fig.21 – Synchronous cascading.

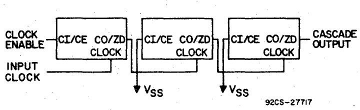
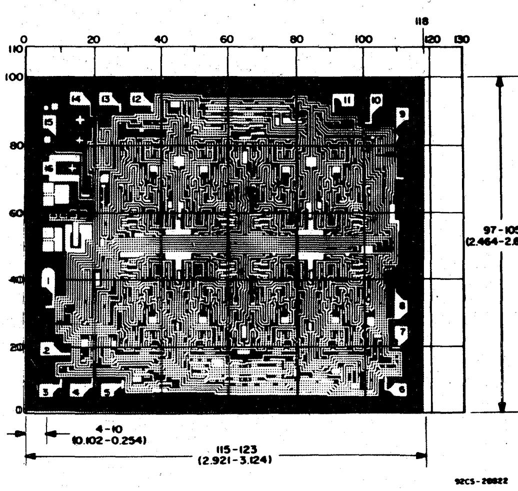


Fig.22 – Ripple cascading.

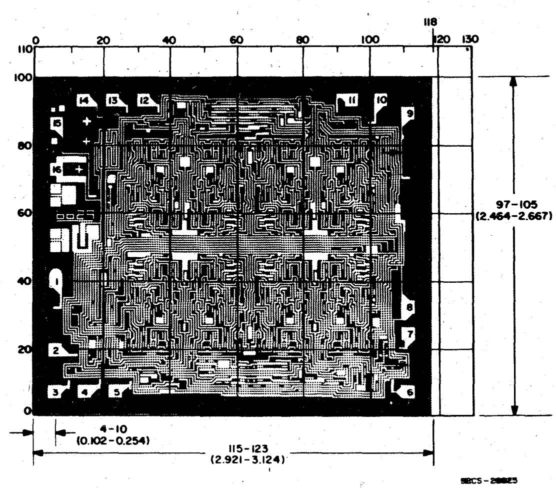
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

Dimensions and pad layout for CD40102B.



Dimensions and pad layout for CD40103B.



COS/MOS 4-Bit Bidirectional Universal Shift Register

High-Voltage Types (20 Volt Rating)

The RCA-CD40104B is a universal shift register featuring parallel inputs, parallel outputs, SHIFT RIGHT and SHIFT LEFT serial inputs, and a high-impedance third output state allowing the device to be used in bus-organized systems.

In the parallel-load mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift-right and shift-left are accomplished synchronously on the positive clock edge with serial data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clearing the register is accomplished by setting both mode controls low and clocking the register. When the output enable input is low, all outputs assume the high impedance state.

The RCA-CD40194B is a universal shift register featuring parallel inputs, parallel outputs SHIFT RIGHT and SHIFT LEFT serial inputs, and a direct overriding clear input. In the parallel-load mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right and shift left are accomplished synchronously on the positive clock edge with data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. **Clocking of the register is inhibited when both mode control inputs are low. When low, the $\overline{RESET}$ input resets all stages and forces all outputs low.**

Features:

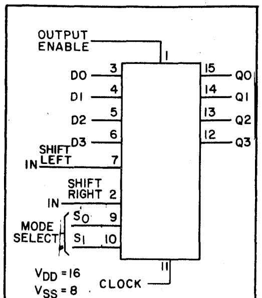
- **Medium-speed: f_{CL} = 12 MHz (typ.) @ V_{DD} = 10 V**
- **Fully static operation**
- **Synchronous parallel or serial operation**
- **Three-state outputs (CD40104B)**
- **Asynchronous master reset (CD40194B)**
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices**

Applications:

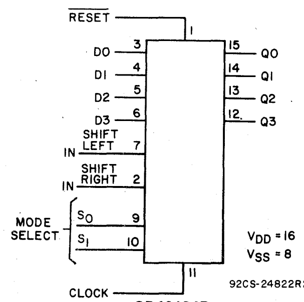
- **Arithmetic unit bus registers**
- **Serial/parallel conversions**
- **General-purpose register for bus-organized systems**
- **General-purpose registers**

The CD40104B and CD40194B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

The CD40194B is similar to industry types 340194 and MC40194.



92CS-24816R2 **CD40104B FUNCTIONAL DIAGRAM**



CD40194B FUNCTIONAL DIAGRAM

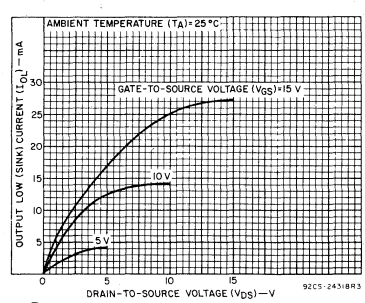


Fig. 1—Typical n-channel output low (sink) current characteristics.

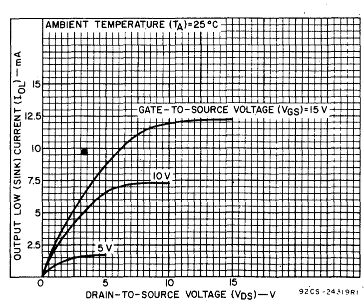


Fig. 2—Minimum n-channel output low (sink) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) .... —0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS .... —0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT .... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A —40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/°C to 200 mW
For T_A = —55 to +100°C (PACKAGE TYPES D, F) .... 500 mW
For T_A = +100 to +125°C (PACAKGE TYPES D, F) .... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) .... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H .... —55 to +125°C
PACKAGE TYPE E .... —40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... —65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		VDD (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For Package-Temperature Range)			3	18	V
Setup Time, D0, D3, SR_{IN}, SL_{IN} to clock	t_S	5	100	—	ns
		10	70	—	
		15	50	—	
SELECT 0, SELECT 1 to clock		5	400	—	
		10	220	—	
		15	130	—	
Hold Time, D0, D03, SR_{IN}' SL_{IN} to clock	t_H	5	0	—	
		10	0	—	
		15	0	—	
SELECT 0, SELECT 1 to clock		5	0	—	
		10	0	—	
		15	0	—	
Clock Pulse Width,	t_W	5	180	—	
		10	80	—	
		15	50	—	
Clock Input Frequency	f_{CL}	5	—	3	MHz
		10	—	6	
		15	—	8	
Clock Input Rise or Fall Time,	t_rCL, t_fCL	5	1000	—	µs
		10	100	—	
		15	100	—	
Reset Pulse Width,*	t_{WR}	5	300	—	ns
		10	200	—	
		15	140	—	

* For CD40194B series only.

CONTROL TRUTH TABLE FOR CD40194B SERIES

CLOCK▲	MODE SELECT S_0	MODE SELECT S_1	OUTPUT ENABLE	ACTION
⌠ (rising)	0	0	1	Reset
⌠ (rising)	1	0	1	Shift right (Q_0 toward Q_3)
⌠ (rising)	0	1	1	Shift left (Q_3 toward Q_0)
⌠ (rising)	1	1	1	Parallel load
X	X	X	0	Operations occur as shown above, but outputs assume high impedance

CONTROL TRUTH TABLE FOR CD40194B SERIES

CLOCK	MODE SELECT S_0	MODE SELECT S_1	$\overline{RESET}$	ACTION
X	0	0	1	No Change
⌠ (rising)	1	0	1	Shift Right (Q0 toward Q3)
⌠ (rising)	0	1	1	Shift Left (Q3 toward Q0)
⌠ (rising)	1	1	1	Parallel Load
X	X	X	0	Reset

1 = High level
0 = Low level
X = Don't care
▲ = Level change

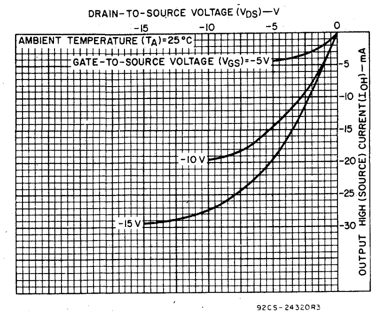


Fig. 3—Typical p-channel output high (source) current characteristics.

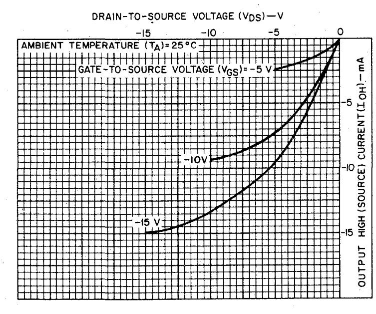


Fig. 4—Minimum p-channel output high (source) current characteristics.

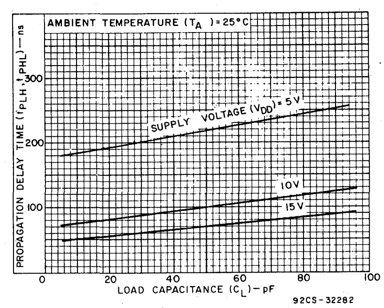


Fig. 5—Typical propagation delay time as a function of load capacitance, (CLOCK to Q).

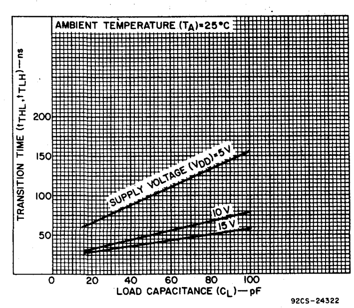


Fig. 6—Typical transition time as a function of load capacitance.

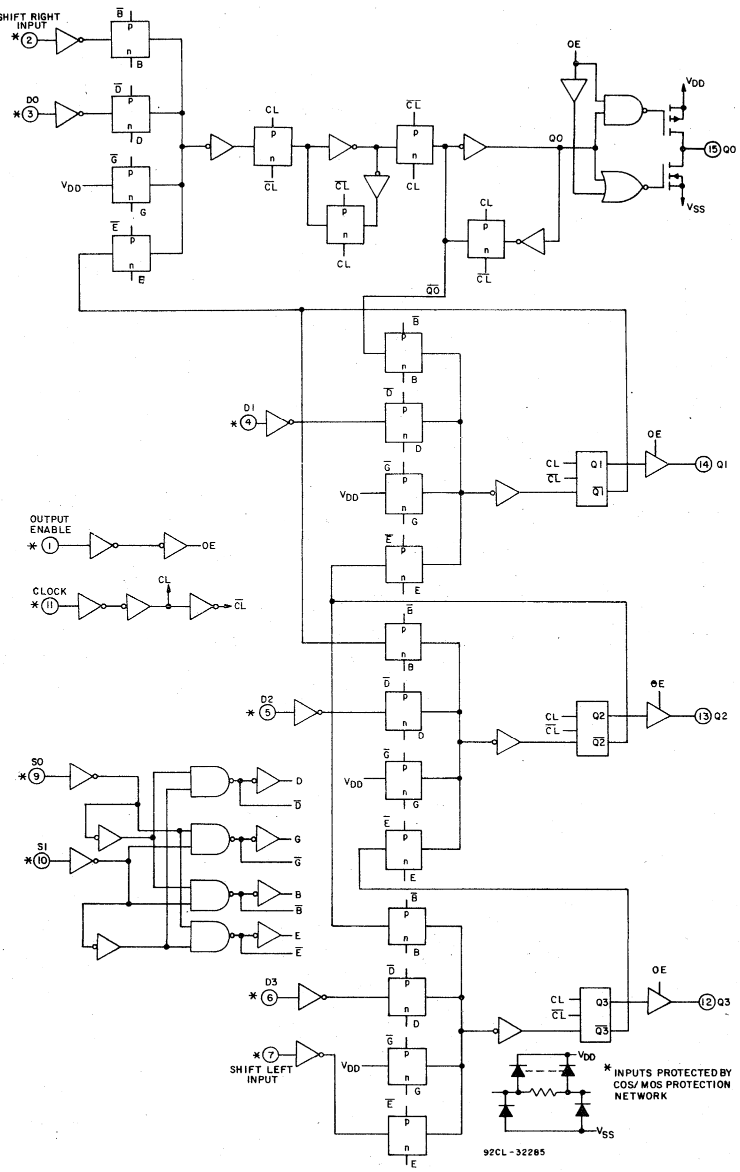


Fig. 7—CD40104B logic diagram.

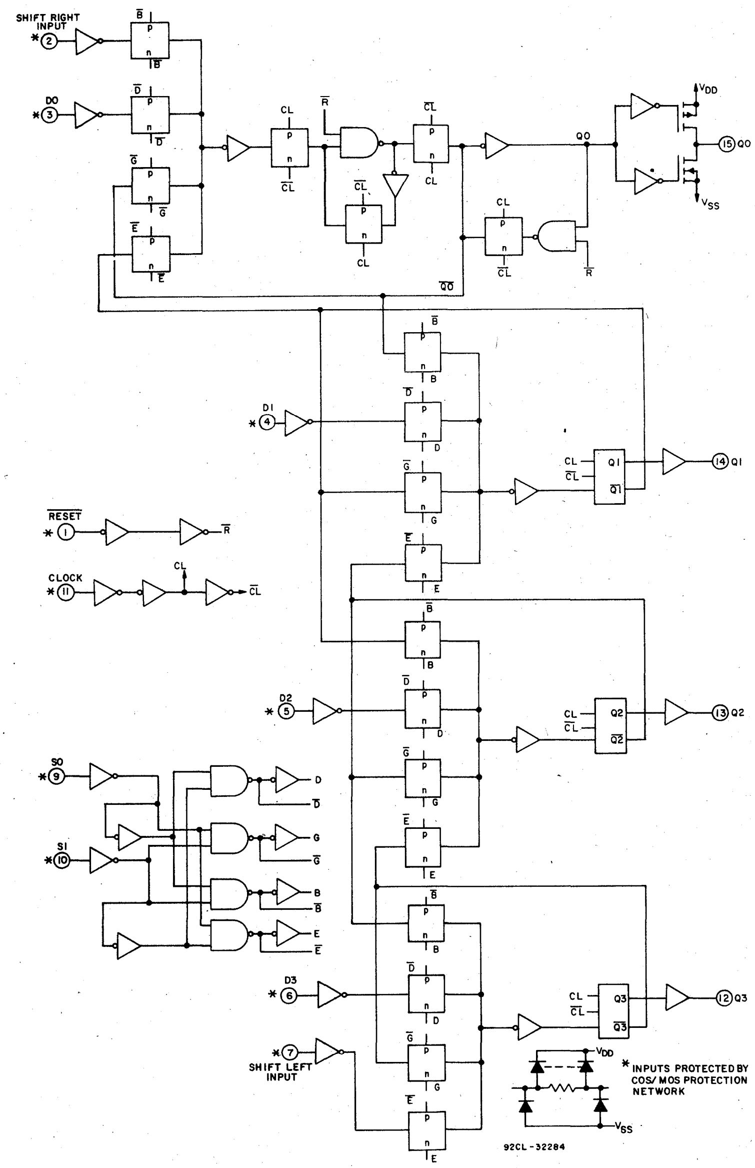


Fig. 8—CD40194B logic diagram.

CD40104B, CD40194B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARAC-TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	—	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	—	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	—	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	—	
Output Voltage: Low-Level, V_{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	—	0,5	5	4.95				4.95	5	—	
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V_{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I_{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	$\pm10^{-5}$	±0.1	μA
3-State Output Leakage Current, I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	—	$\pm10^{-4}$	±0.4	μA

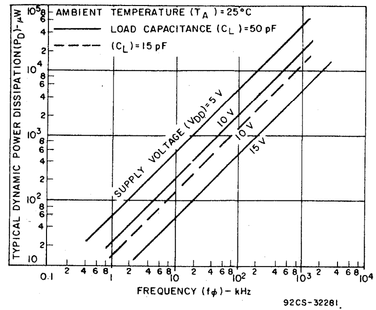


Fig. 9—Typical power dissipation as a function of frequency.

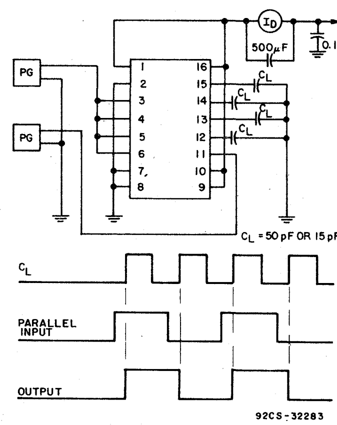


Fig. 10—Dynamic power dissipation test circuit.

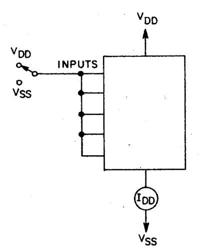


Fig. 11—Quiescent-device-current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} V	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time: Clock to Q t_{PHL}, t_{PLH}	5	—	220	440	ns
	10	—	100	200	
	15	—	70	140	
3-State Outputs:■ High Impedance t_{PZH}, t_{PZL}, t_{PLZ}	5	—	80	160	
	10	—	35	70	
	15	—	25	50	
t_{PHZ}	5	—	45	90	
	10	—	25	50	
	15	—	20	40	
Output Transition Time t_{THL}, t_{TLH}	5	—	100	200	
	10	—	50	100	
	15	—	40	80	
Minimum Setup Time: t_S D0, D3, SR_{IN}, SL_{IN} to Clock	5	—	80	100	
	10	—	35	70	
	15	—	20	50	
SELECT 0, SELECT 1 to Clock	5	—	200	400	
	10	—	110	220	
	15	—	65	130	
Minimum Hold Time: t_H D0, D3, SR_{IN}, SL_{IN} to Clock	5	—	−65	0	
	10	—	−25	0	
	15	—	−15	0	
SELECT 0, SELECT 1 to Clock	5	—	−170	0	
	10	—	−95	0	
	15	—	−55	0	
Minimum Clock Pulse Width t_W	5	—	90	180	
	10	—	40	180	
	15	—	25	50	
Maximum Clock Input Frequency f_{CL}	5	3	6	—	MHz
	10	6	12	—	
	15	8	15	—	
Maximum Clock Rise or Fall Time t_rCL, t_fCL	5	—	—	1000	µs
	10	—	—	100	
	15	—	—	100	
Mininum Reset Pulse Width* t_{WR}	5	—	150	300	ns
	10	—	100	200	
	15	—	70	140	
Reset Propagation Delay* t_{PRHL}	5	—	230	460	
	10	—	90	180	
	15	—	65	130	
Input Capacitance C_{IN}	Any Input	—	5	7.5	pF

■ For CD40104B series only. * For CD40194B series only.

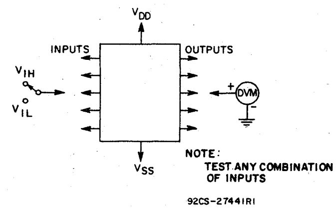


Fig. 12—Input-voltage test circuit.

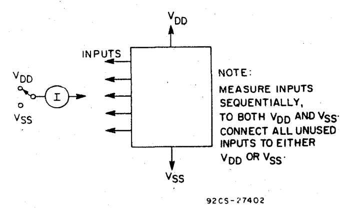
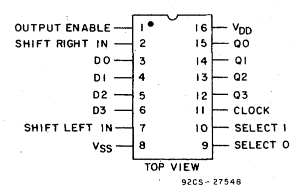


Fig. 13—Input current test circuit.

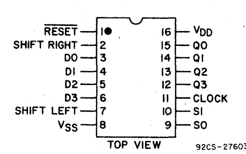
TERMINAL DIAGRAMS

Top View

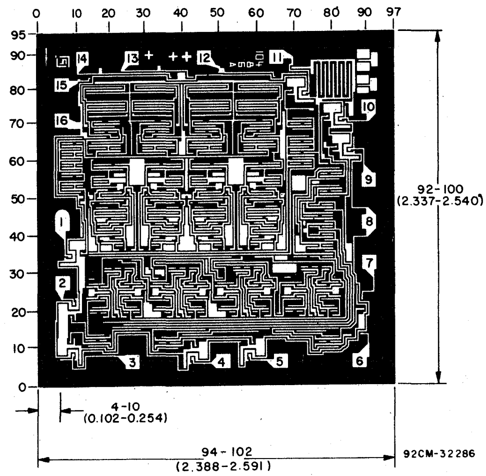


CD40104B

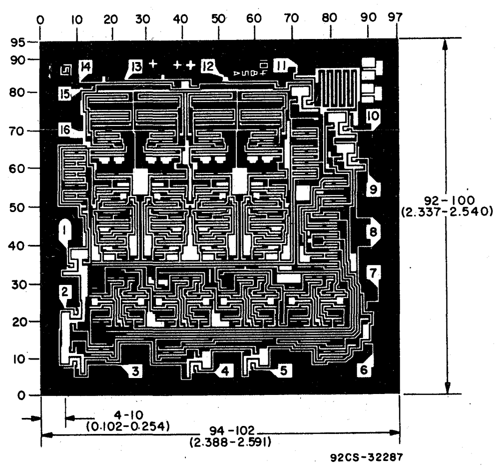
Top View



CD40194B



Dimensions and pad layout for CD40104BH



Dimensions and pad layout for CD40194BH

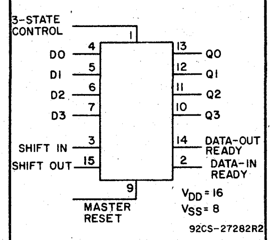
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS FIFO Register

4 Bits X 16 Words

High-Voltage Types (20-Volt Rating)



FUNCTIONAL DIAGRAM

The RCA-CD40105B is a low-power first-in-first-out (FIFO) "elastic" storage register that can store 16 4-bit words. It is capable of handling input and output data at different shifting rates. This feature makes it particularly useful as a buffer between asynchronous systems.

Each word position in the register is clocked by a control flip-flop, which stores a marker bit. A "1" signifies that the position's data is filled and a "0" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse that transfers data from the preceding four data latches into its own four data latches and resets the preceding flip-flop to "0". The first and last control flip-flops have buffered outputs. Since all empty locations "bubble" automatically to the input end, and all valid data ripple through to the output end, the status of the first control flip-flop (DATA-IN READY) indicates if the FIFO is full, and the status of the last flip-flop (DATA-OUT READY) indicates if the FIFO contains data. As the earliest data are removed from the bottom of the data stack (the output end), all data entered later will automatically propagate (ripple) toward the output.

Loading Data – Data can be entered whenever the DATA-IN READY (DIR) flag is high, by a low to high transition on the SHIFT-IN (SI) input. This input must go low momentarily before the next word is accepted by the FIFO. The DIR flag will go low momentarily, until the data have been transferred to the second location. The flag will remain low when all 16-word locations are filled with valid data, and further pulses on the SI input will be ignored until DIR goes high.

Unloading Data – As soon as the first word has rippled to the output, DATA-OUT READY (DOR) goes high, and data can be removed by a falling edge on the SO input. This falling edge causes the DOR signal to go low while the word on the output is dumped and the next word moves to the output. As long as valid data are available in the FIFO, the DOR signal will go high again signifying that the next word is ready at the output. When the FIFO is empty, DOR will remain low, and any further commands will be ignored until a "1" marker ripples down to the last control register, when DOR goes high. Unloading of data is inhibited while the 3-state control input is high. The 3-state control signal should not be shifted from high to low (data outputs turned on) while the SHIFT-OUT is at logic 0. This level change would cause the first word to be shifted out (unloaded) immediately and the data to be lost.

Cascading – The CD40105B can be cascaded to form longer registers simply by connecting the DIR to SO and DOR to SI. In the cascaded mode, a MASTER RESET pulse must be applied after the supply voltage is turned on. For words wider than 4 bits, the DIR and the DOR outputs must be gated together with AND gates. Their outputs drive the SI and SO inputs in parallel, if expanding is done in both directions (see Figs. 4 and 5).

3-State Outputs – In order to facilitate data busing, 3-state outputs are provided on the data output lines, while the load condition of the register can be detected by the state of the DOR output.

Master Reset – A high on the MASTER RESET (MR) sets all the control logic marker bits to "0". DOR goes low and DIR goes high. The contents of the data register are not changed, only declared invalid, and will be superseded when the first word is loaded. The shift-in must be low during Master Reset.

The CD40105B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Independent asynchronous inputs and outputs**
- **3-state outputs**
- **Expandable in either direction**
- **Status indicators on input and output**
- **Reset capability**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD} = 15 V**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Bit rate smoothing**
- **CPU/terminal buffering**
- **Data communications**
- **Peripheral buffering**
- **Line printer input buffers**
- **Auto dialers**
- **CRT buffer memories**
- **Radar data acquisition**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	–0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	–55 to +125°C
PACKAGE TYPE E	–40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	–65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

CD40105B Types

RECOMMENDED OPERATING CONDITIONS at 25°C, Except as Noted

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	–	3	18	V
Shift-In or Shift-Out Rate	5	–	1.5	MHz
	10	–	3	
	15	–	4	
Shift-In Pulse Width	5	200	–	ns
	10	80	–	
	15	60	–	
Shift-Out Pulse Width	5	360	–	ns
	10	160	–	
	15	100	–	
Shift-In or Shift-Out Rise Time	5	–	15	µs
	10	–	15	
	15	–	15	
Shift-In Fall Time	5	–	15	µs
	10	–	15	
	15	–	15	
Shift-Out Fall Time	5	–	15	µs
	10	–	5	
	15	–	5	
Data Hold Time	5	350	–	ns
	10	150	–	
	15	120	–	
Master Reset Pulse Width	5	220	–	ns
	10	90	–	
	15	60	–	

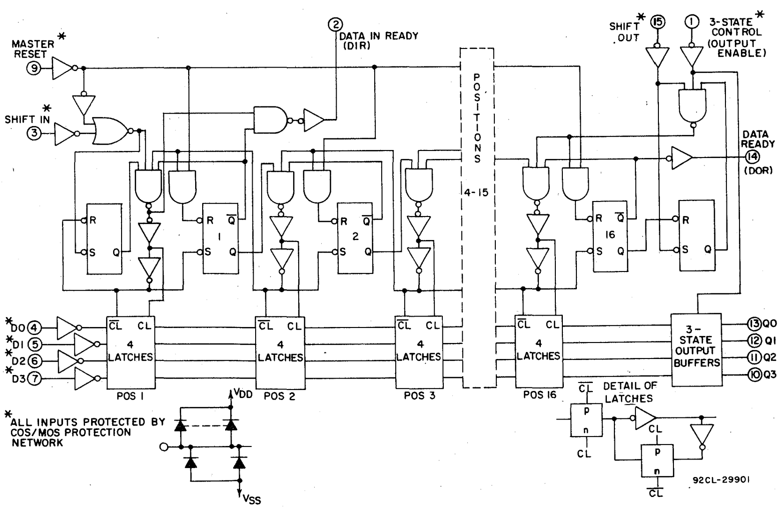


Fig. 1 – Logic diagram for the CD40105B.

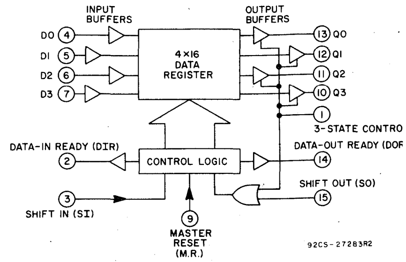
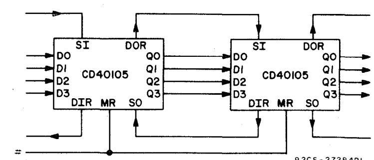


Fig. 2 – CD40105B functional block diagram.



=MASTER RESET pulse must be applied when cascading by 16 N bits.

Fig. 3 – Expansion, 4-bits wide-by-16 N-bits long.

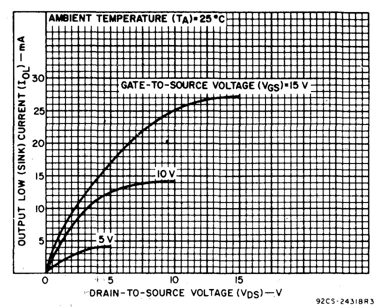


Fig. 4 – Typical output low (sink) current characteristics.

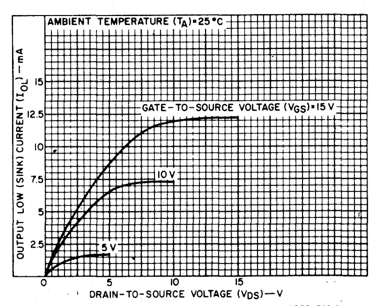


Fig. 5 – Minimum output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages; Values at −40, +25, +85 Apply to E Package: −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm10^{-4}$	±0.4	μA

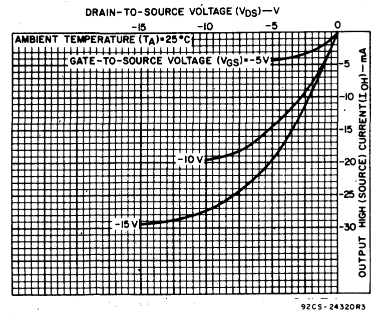


Fig. 6 – Typical output high (source) current characteristics.

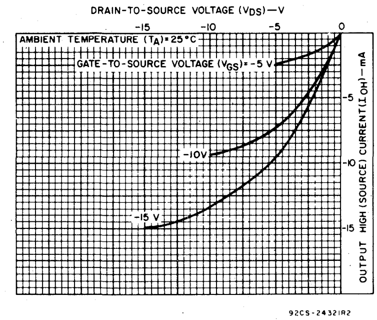


Fig. 7 – Minimum output high (source) current characteristics.

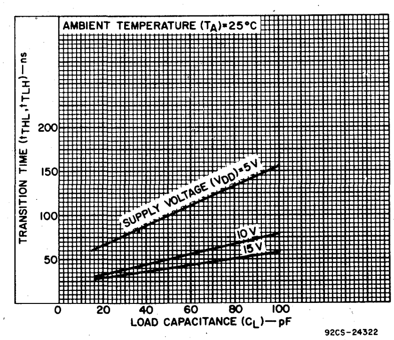


Fig. 8 – Typical transition time as a function of load capacitance.

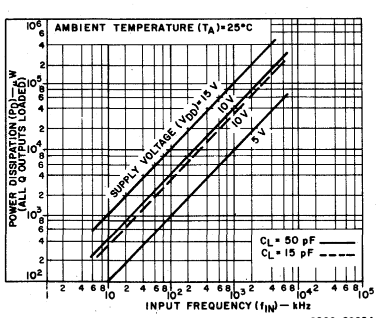


Fig. 9 – Typical dynamic power dissipation as a function of frequency.

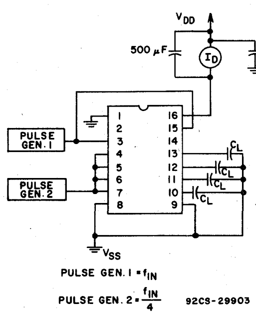


Fig. 10 – Dynamic power dissipation test circuit.

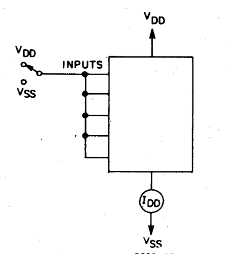


Fig. 11 – Quiescent-device-current test circuit.

CD40105B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C;
Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
		V_{DD} (V)	Min.	Typ.	Max.	
Propagation Delay Time: Shift-Out or Reset to Data-Out Ready, t_{PHL}		5 10 15	– – –	185 90 65	370 180 130	ns
Shift-In to Data-In Ready, t_{PHL}		5 10 15	– – –	160 65 45	320 130 90	ns
3-State Control to Data Out t_{PZH}, t_{PZL}		5 10 15	– – –	140 60 40	280 120 80	ns
t_{PHZ}, t_{PLZ}		5 10 15	– – –	100 50 40	200 100 80	ns
Ripple-Through Delay Input to Output, t_{PLH}		5 10 15	– – –	2 1 0.7	4 2 1.4	μs
Transition Time, t_{THL}, t_{TLH}		5 10 15	– – –	100 50 40	200 100 80	ns
Maximum Shift-In or Shift-Out Rate, f_I		5 10 15	1.5 3 4	3 6 8	– – –	MHz
Minimum Shift-In Pulse Width, t_{WH}		5 10 15	– – –	100 40 30	200 80 60	ns
Minimum Shift-Out Pulse Width, t_{WL}		5 10 15	– – –	180 80 50	360 160 100	ns
Maximum Shift-In or Shift-Out Rise Time, t_r		5 10 15	– – –	– – –	15 15 15	μs
Maximum Shift-In Fall Time, t_f		5 10 15	– – –	– – –	15 15 15	μs
Maximum Shift-Out Fall Time, t_f		5 10 15	– – –	– – –	15 5 5	μs
Minimum Data Setup Time, t_{SU}		5 10 15	– – –	– – –	0 0 0	ns
Minimum Data Hold Time, t_H		5 10 15	– – –	175 75 60	350 150 120	ns
Data-In Ready Pulse Width, t_{WL}		5 10 15	– – –	260 100 70	520 200 140	ns
Data-Out Ready Pulse Width, t_{WL}		5 10 15	– – –	220 90 65	440 180 130	ns
Minimum Master Reset Pulse Width, t_{WH}		5 10 15	– – –	100 45 30	200 90 60	ns
Input Capacitance C_{IN}	(Any Input)	–	–	5	7.5	pF

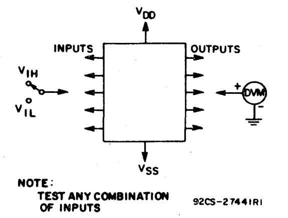


Fig. 12 – Input-voltage test circuit.

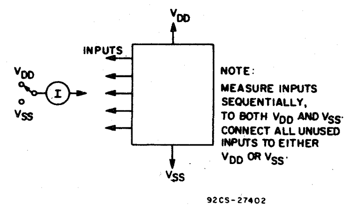
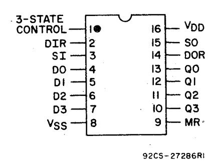


Fig. 13 – Input current test circuit.



TERMINAL ASSIGNMENT

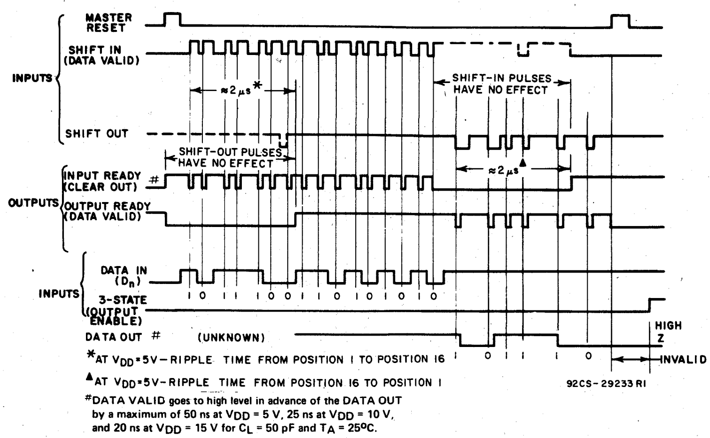


Fig. 14 – Timing diagram for the CD40105B.

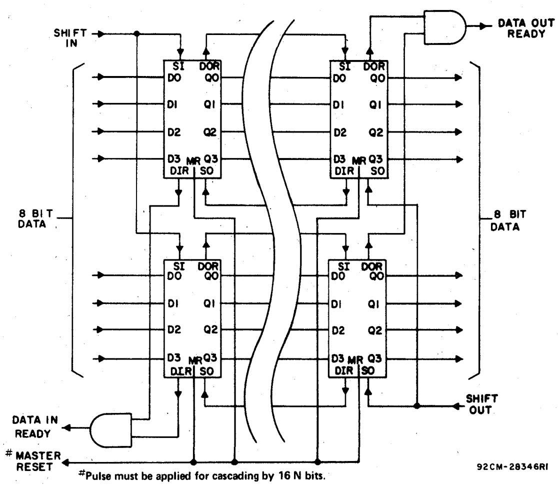
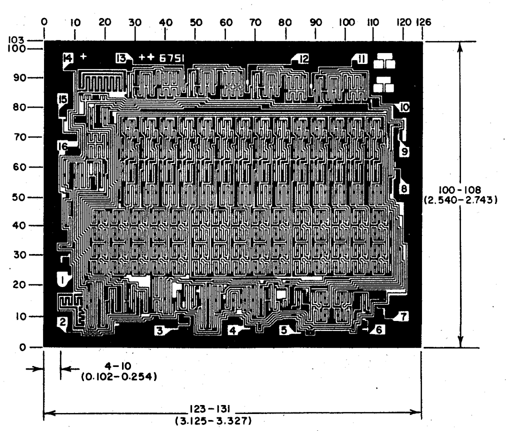


Fig. 15 – Expansion, 8-bits-wide-by-16 N-bits long using CD40105.



Dimension and pad layout for CD40105B.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CD40106B Types

COS/MOS Hex Schmitt Triggers

High-Voltage Types (20-Volt Rating)

The RCA-CD40106B consists of six Schmitt-trigger circuits. Each circuit functions as an inverter with Schmitt-trigger action on the input. The trigger switches at different points for positive- and negative-going signals. The difference between the positive-going voltage (V_P) and the negative-going voltage (V_N) is defined as hysteresis voltage (V_H) (see Fig.6).

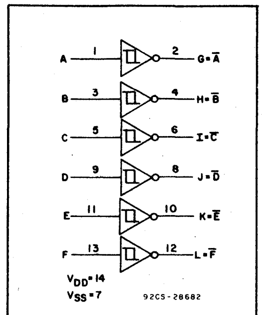
The CD40106B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- Schmitt-trigger action with no external components
- Hysteresis voltage (typ.) 0.9 V at V_{DD} = 5 V, 2.3 V at V_{DD} = 10 V, and 3.5 V at V_{DD} = 15 V
- Noise immunity greater than 50%
- No limit on input rise and fall times
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Low V_{DD} to V_{SS} current during slow input ramp
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators



FUNCTIONAL DIAGRAM

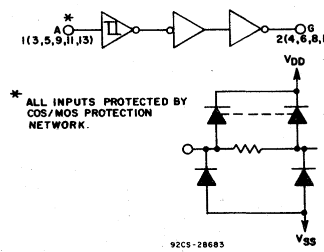


Fig.1 – Logic diagram (1 of 6 Schmitt triggers).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	–0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F,)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F,)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	–55 to +125°C
PACKAGE TYPE E	–40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	–65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

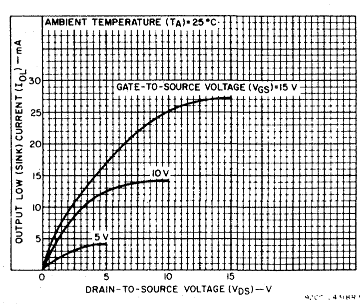


Fig.2 – Typical output low (sink) current characteristics.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS TYP.	LIMITS MAX.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH}		5	140	280	ns
		10	70	140	
		15	60	120	
Transition Time: t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

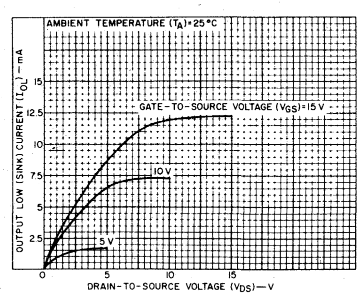


Fig.3 – Minimum output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55,+25,+125 Apply to D, F,H Packages Values at −40,+25,+85 Apply to E Packages							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Positive Trigger Threshold Voltage V_P Min.	–	–	5	2.2	2.2	2.2	2.2	2.2	2.9	–	V
	–	–	10	4.6	4.6	4.6	4.6	4.6	5.9	–	
	–	–	15	6.8	6.8	6.8	6.8	6.8	8.8		
V_P Max.	–	–	5	3.6	3.6	3.6	3.6	–	2.9	3.6	
	–	–	10	7.1	7.1	7.1	7.1	–	5.9	7.1	
	–	–	15	10.8	10.8	10.8	10.8	–	8.8	10.8	
Negative Trigger Threshold Voltage V_N Min.	–	–	5	0.9	0.9	0.9	0.9	0.9	1.9	–	V
	–	–	10	2.5	2.5	2.5	2.5	2.5	3.9	–	
	–	–	15	4	4	4	4	4	5.8	–	
V_N Max.	–	–	5	2.8	2.8	2.8	2.8	–	1.9	2.8	
	–	–	10	5.2	5.2	5.2	5.2	–	3.9	5.2	
	–	–	15	7.4	7.4	7.4	7.4	–	5.8	7.4	
Hysteresis Voltage V_H Min.	–	–	5	0.3	0.3	0.3	0.3	0.3	0.9	–	V
	–	–	10	1.2	1.2	1.2	1.2	1.2	2.3	–	
	–	–	15	1.6	1.6	1.6	1.6	1.6	3.5	–	
V_H Max.	–	–	5	1.6	1.6	1.6	1.6	–	0.9	1.6	
	–	–	10	3.4	3.4	3.4	3.4	–	2.3	3.4	
	–	–	15	5	5	5	5	–	3.5	5	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0.5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage Low-Level, V_{OL} Max.	–	5	5	0.05				–	0	0.05	V
	–	10	10	0.05				–	0	0.05	
	–	15	15	0.05				–	0	0.05	
Output Voltage High Level, V_{OH} Min.	–	0	5	4.95				4.95	5	–	
	–	0	10	9.95				9.95	10	–	
	–	0	15	14.95				14.95	15	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	±10⁻⁵	±0.1	μA

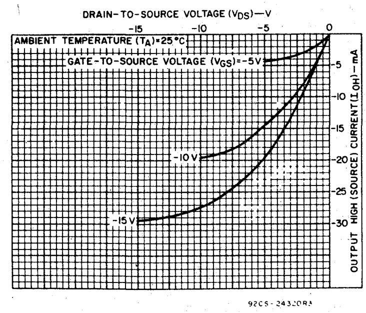


Fig.4 – Typical output high (source) current characteristics.

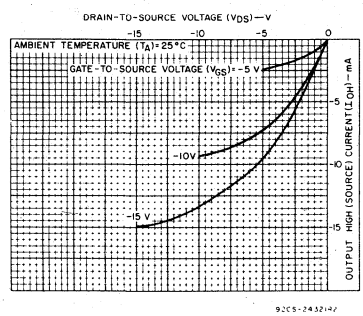


Fig.5 – Minimum output high (source) current characteristics.

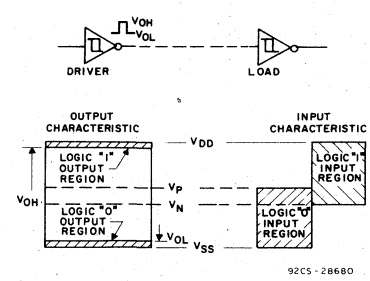


Fig.7 – Input and output characteristics.

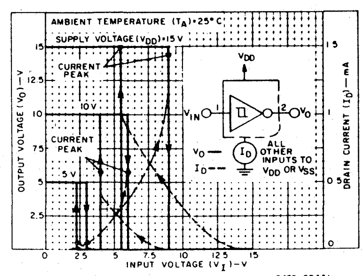
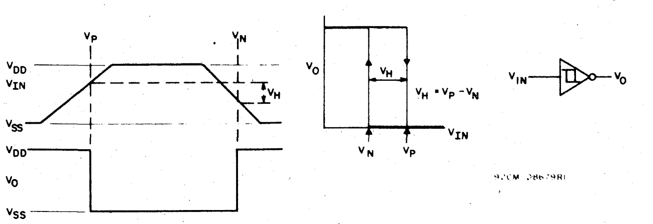


Fig.8 – Typical current and voltage transfer characteristics.



a) Definition of V_P, V_N, V_H *b) Transfer characteristics of 1 of 6 gates*

Fig.6 – Hysteresis definition, characteristics, and test set-up.

CD40106B Types

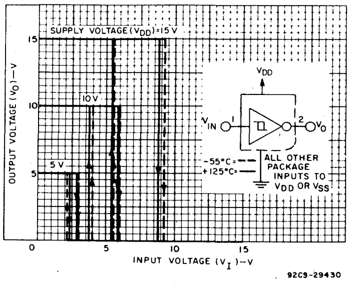


Fig.9 — Typical voltage transfer characteristics as a function of temperature.

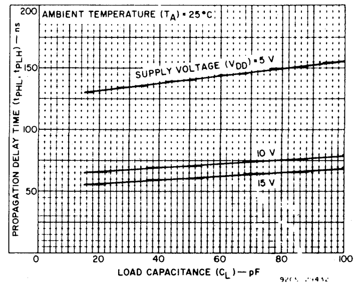


Fig.10 — Typical propagation delay time as a function of load capacitance.

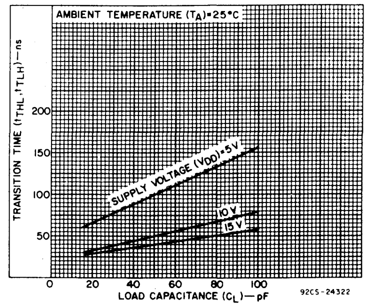


Fig.11 — Typical transition time as a function of load capacitance.

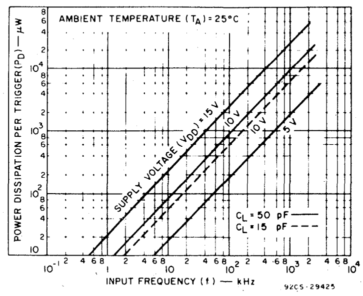


Fig.12 — Typical power dissipation per trigger as a function of input frequency.

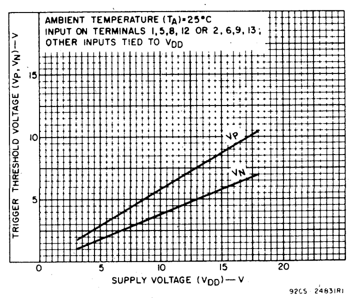


Fig.13 — Typical trigger threshold voltage as a function of supply voltage.

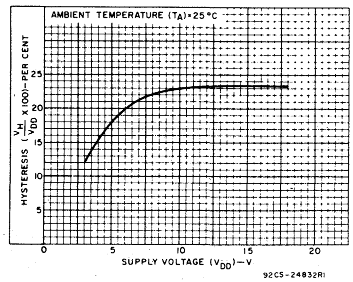


Fig.14 — Typical per cent hysteresis as a function of supply voltage.

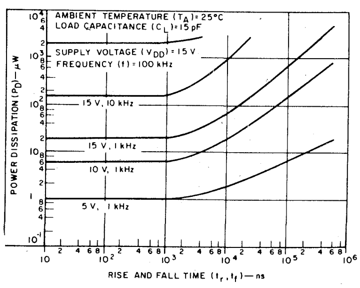


Fig.15 — Typical power dissipation as a function of rise and fall times.

APPLICATIONS

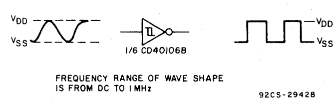


Fig.16 — Wave shaper.

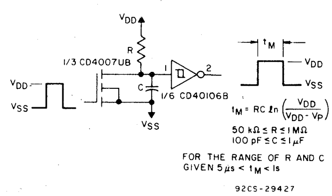


Fig.17 — Monostable multivibrator.

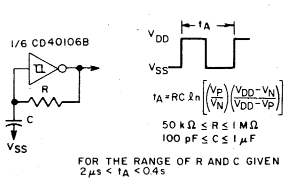


Fig.18 — Astable multivibrator.

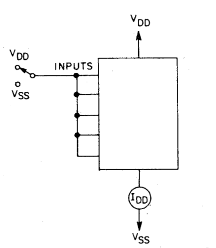


Fig.19 — Quiescent device current test circuit.

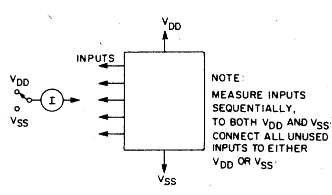


Fig.20 — Input current test circuit.

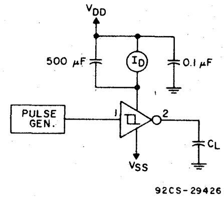
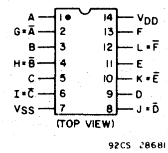
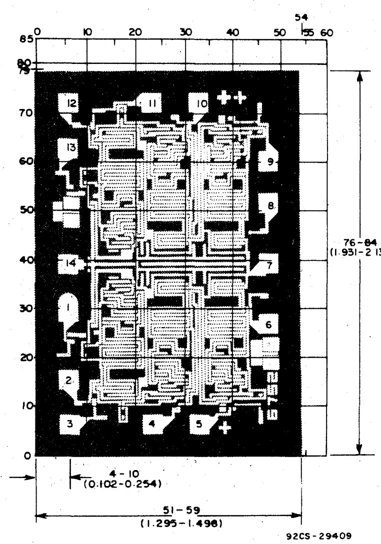


Fig.21 — Dynamic power dissipation test circuit.



TERMINAL ASSIGNMENT



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and Pad Layout for CD40106BH

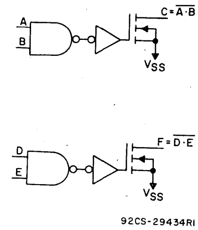
COS/MOS Dual 2-Input NAND Buffer/Driver

High-Voltage Type (20-Volt Rating)

The RCA-CD40107B is a dual 2-input NAND buffer/driver containing two independent 2-input NAND buffers with open-drain single n-channel transistor outputs. This device features a wired-OR capability and high output sink current capability (136 mA typ. at V_{DD} = 10 V, V_{DS} = 1 V). The CD40107B is supplied in the 8-lead dual-in-line plastic (Mini-DIP) package (E suffix), 14-lead hermetic frit-seal ceramic package (F suffix), and in chip form (H suffix).

Features:

- **32 times standard B-Series output current drive sinking capability — 136 mA typ. @ V_{DD} = 10 V, V_{DS} = 1 V**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **5-V, 10-V, and 15-V parametric ratings**
- **Noise margin, full package temperature range, R_L to V_{DD} = 10 kΩ:**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM

Applications

- **Driving relays, lamps, LEDs**
- **Line driver**
- **Level shifter (up or down)**

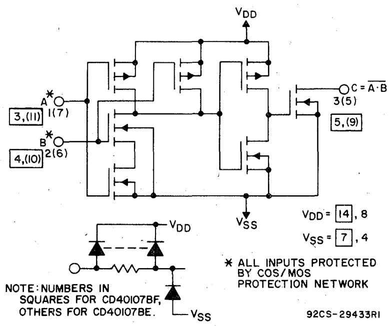


Fig. 1 — Schematic diagram of CD40107B (one of 2 gates)

TRUTH TABLE

A	B	C	
0	0	1*	Z#
1	0	1*	Z#
0	1	1*	Z#
1	1	0	

*Requires external pull-up resistor (R_L) to V_{DD}.

#Without pull-up resistor (3-state).

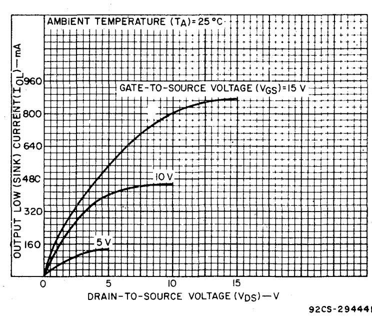


Fig.2 — Typical output low (sink) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPE F) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES F, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

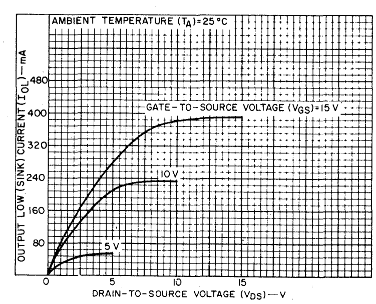


Fig.3 — Minimum output low (sink) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, $C_L = 50$ pF, Input $t_r, t_f = 20$ ns

CHARACTERISTIC	TEST CONDITIONS	V_{DD} Volts	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay: High-to-Low, t_{PHL}	R_L* = 120 Ω	5	100	200	ns
		10	45	90	
		15	30	60	
Low-to-High, t_{PLH}	R_L* = 120 Ω	5	100	200	ns
		10	60	120	
		15	50	100	
Transition Time: High-to-Low, t_{THL}	R_L* = 120 Ω	5	50	100	ns
		10	20	40	
		15	10	20	
Low-to-High, t_{TLH}	R_L* = 120 Ω	5	50	100	ns
		10	35	70	
		15	25	50	
Average Input Capacitance, C_{IN}	Any Input		5	7.5	pF
Average Output Capacitance, C_{OUT}	Any Output		30	–	pF

* R_L is external pull-up resistor to V_{DD}.

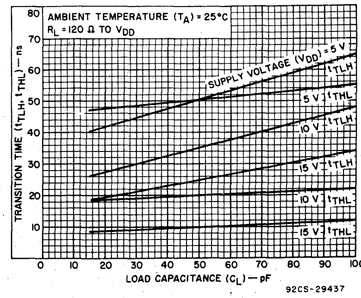


Fig.4 – Typical transition time as a function of load capacitance.

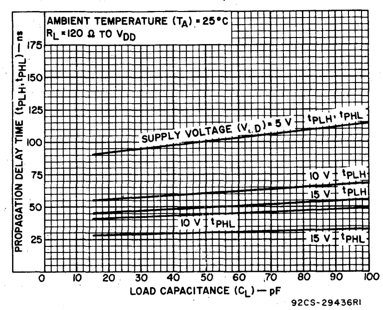


Fig.5 – Typical propagation delay time as a function of load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to F,H Packages Values at –40, +25, +85 Apply to E Package –55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	21	20	14	12	16	32	–	mA
	1	0,5	5	44	42	30	25	34	68	–	
	0.5	0,10	10	49	46	32	28	37	74	–	
	1	0,10	10	89	85	60	51	68	136	–	
	0.5	0,15	15	66	63	44	38	50	100	–	
Output High (Source) Current I_{OH} Min.	No Internal Pull-Up Device										
Input Low Voltage V_{IL} Max.*	4.5	–	5	1.5				–	–	1.5	V
	9	–	10	3				–	–	3	
	13.5	–	15	4				–	–	4	
Input High Voltage V_{IH} Min.*	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA
Output Leakage Current I_{OZ} Max.	18	0,18	18	2	2	20	20	–	10^{-4}	2	μA

* Measured with external pull-up resistor, R_L = 10 kΩ to V_{DD}.

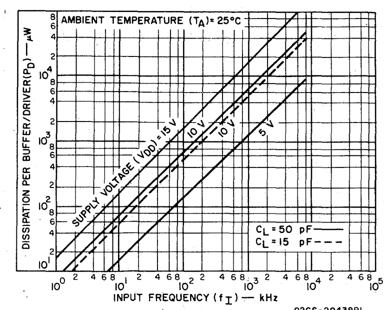


Fig.6 – Typical power dissipation as a function of input frequency.

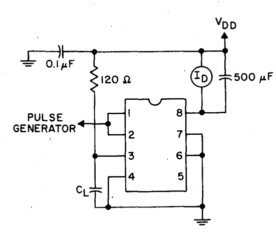
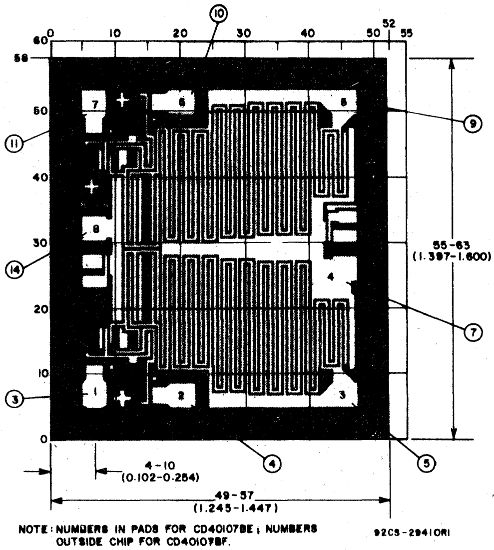


Fig. 7 – Power-dissipation test circuit for CD40107BE.



Dimensions and Pad Layout for CD40107BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

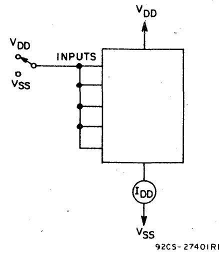


Fig.8 – Quiescent-device current test circuit.

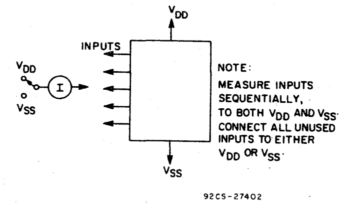


Fig. 9 – Input-current test circuit.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

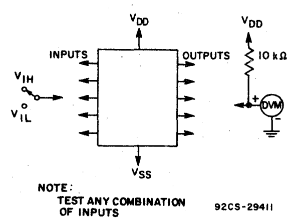
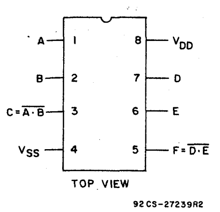
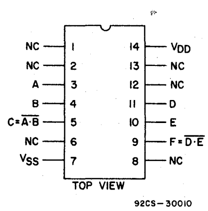


Fig. 10 – Input-voltage test circuit.



CD40107BE



CD40107BF

TERMINAL ASSIGNMENTS

Special Considerations for CD40107B

1. **Limiting Capacitive Currents for CL > 500 pF, V_{DD} > 15 V.**
   For $V_{DD} > 15$ V, and load capacitance (C_L) from output to ground > 500 pF, an external 25 Ω series limiting resistor should be inserted between the output terminal and C_L. No external resistor is necessary if $C_L < 500$ pF or $V_{DD} < 15$ V.
2. **Driving Inductive Loads**
   When using the CD40107B to drive inductive loads, the load should be shunted with a diode to prevent high voltages from developing across the CD40107B output.

COS/MOS 4 x 4 Multiport Register

High-Voltage Types (20-Volt Rating)

The RCA-CD40108B is a 4 x 4 multiport register containing four 4-bit registers, write address decoder, two separate read address decoders, and two 3-state output buses.

When the ENABLE input is low, the corresponding output bus is switched, independently of the clock, to a high-impedance state. The high-impedance third state provides the outputs with the capability of being connected to the bus lines in a bus-organized system without the need for interface or pull-up components.

When the WRITE ENABLE input is high, all data input lines are latched on the positive transition of the CLOCK and the data is entered into the word selected by the write address lines. When WRITE ENABLE is low, the CLOCK is inhibited and no new data is entered. In either case, the contents of any word may be accessed via the read address lines independent of the state of the CLOCK input.

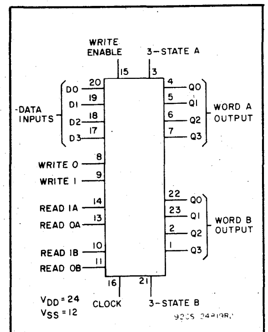
The CD40108B types are supplied in hermetic 24-lead dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Four 4-bit registers**
- **One input and two output buses**
- **Unlimited expansion in bit and word directions**
- **Data lines have latched inputs**
- **3-state outputs**
- **Separate control of each bus, allowing simultaneous independent reading of any of four registers on Bus A and Bus B and independent writing into any of the four registers**
- **CD40108B is pin-compatible with industry type MC14580**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package-temperature range):**
  - **1 V at V_{DD} = 5 V**
  - **2 V at V_{DD} = 10 V**
  - **2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **Scratch-pad memories**
- **Arithmetic units**
- **Data storage**



FUNCTIONAL DIAGRAM

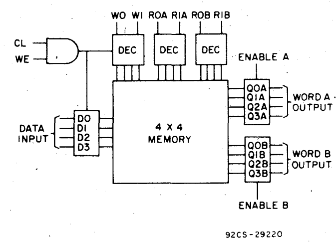


Fig. 1 — Block diagram.

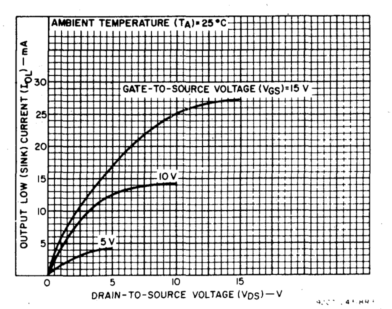


Fig. 2— Typical output low (sink) current characteristics.

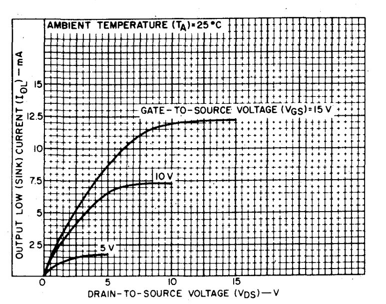


Fig. 3— Minimum output low (sink) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . . +265°C

TRUTH TABLE

CLOCK	WRITE ENABLE	WRITE 1	WRITE 0	READ 1A	READ 0A	READ 1B	READ 0B	ENABLE A	ENABLE B	D_n	Q_{nA}	Q_{nB}
↑	1	S1	S2	S1	S2	S1	S2	1	1	1	1	1
↑	1	S1	S2	S1	S2	S1	S2	1	1	0	0	0
X	X	X	X	X	X	X	X	0	0	X	Z	Z
↑	1	0	0	0	1	1	0	1	1	D_n to word 0	Word 1 out	Word 2 out
↑	0	0	0	0	1	1	0	1	1	Word 0 not altered	Word 1 out	Word 2 out
X	X	X	X	1	0	0	1	1	1	X	Word 2 out	Word 1 out
↓	X	X	X	X	X	X	X	1	1	X	NC	NC

1 - HIGH LEVEL, 0 LOW LEVEL, X DON'T CARE, Z= HIGH IMPEDANCE
S1 and S2 refer to input states of either 1 or 0

RECOMMENDED OPERATING CONDITIONS *at $T_A = 25^oC$, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:*

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply Voltage Range (For T_A = Full Package Temperature Range)	–	3	18	V
Set-Up Time: Data to Clock, $t_{S(D)}$	5	0	–	ns
	10	0	–	
	15	0	–	
Write Enable to $\overline{Clock}$, $t_{S(WE)}$	5	250	–	ns
	10	100	–	
	15	70	–	
Write Address to $\overline{Clock}$, $t_{S(WA)}$	5	250	–	ns
	10	100	–	
	15	70	–	
Hold Time: Data to Clock, $t_{H(D)}$	5	220	–	ns
	10	100	–	
	15	80	–	
Write Enable to Clock, $t_{H(WE)}$	5	270	–	ns
	10	130	–	
	15	80	–	
Write Address to Clock, $t_{H(WA)}$	5	330	–	ns
	10	140	–	
	15	90	–	
Clock Input Frequency, f_{CL}	5	–	1.5	MHz
	10	–	3.5	
	15	–	4.5	
Clock Pulse Width, CL or WE t_W	5	350	–	ns
	10	130	–	
	15	90	–	
Clock Rise or Fall Time, t_rCL or t_fCL	5	–	15	µs
	10	–	5	
	15	–	5	

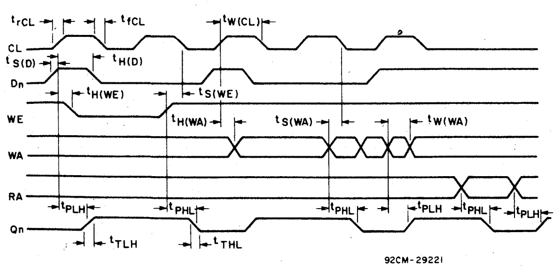


Fig. 4— Timing diagram.

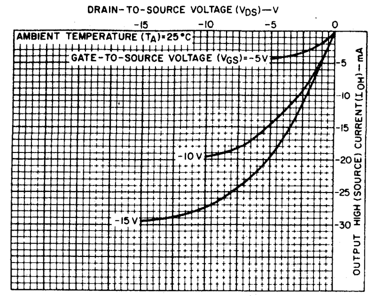


Fig. 5— Typical output high (source) current characteristics.

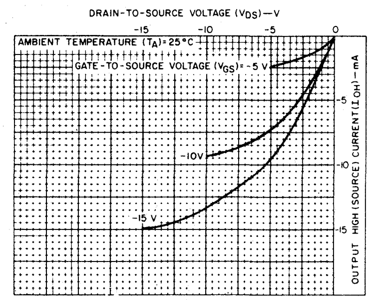


Fig. 6— Minimum output high (source) current characteristics.

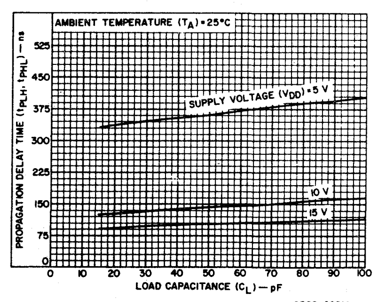


Fig. 7— Typical propagation delay time as a function of load capacitance (CL or WE to Q).

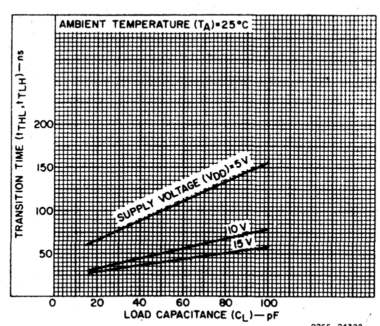


Fig. 8— Typical transition time as a function of load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} Clock or Write Enable to Q	5	–	360	720	ns
	10	–	140	280	
	15	–	100	200	
Read or Write Address to Q	5	–	300	600	ns
	10	–	120	240	
	15	–	85	170	
3-State Disable Delay Time: t_{PZH}, t_{PHZ}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
t_{PZL}, t_{PLZ}	5	–	130	260	ns
	10	–	60	120	
	15	–	50	100	
Output Transition Time: t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Minimum Setup Time: Data to Clock $t_{S(D)}$	5	–	–95	0	ns
	10	–	–35	0	
	15	–	–20	0	
Write Enable to $\overline{Clock}$ $t_{S(WE)}$	5	–	125	250	ns
	10	–	50	100	
	15	–	35	70	
Write Address to $\overline{Clock}$ $t_{S(WA)}$	5	–	125	250	ns
	10	–	50	100	
	15	–	35	70	
Clock Rise and Fall Time: t_rCL, t_fCL	5	–	–	15	µs
	10	–	–	5	
	15	–	–	5	
Minimum Hold Time: Data to Clock $t_{H(D)}$	5	–	110	220	ns
	10	–	50	100	
	15	–	40	80	
Write Enable to Clock $t_{H(WE)}$	5	–	135	270	ns
	10	–	65	130	
	15	–	40	80	
Write Address to $\overline{Clock}$ $t_{H(WA)}$	5	–	165	330	ns
	10	–	70	140	
	15	–	45	90	
Maximum Clock Input Frequency, f_{CL}	5	1.5	3	–	MHz
	10	3.5	7	–	
	15	4.5	9	–	
Minimum Clock Pulse Width, Clock or Write Enable $t_{W(CL)}$	5	–	175	350	ns
	10	–	65	130	
	15	–	45	90	
Write Address $t_{W(WA)}$	5	–	150	300	ns
	10	–	75	150	
	15	–	45	90	
Average Input Capacitance, (Any Input) C_I	–	–	5	7.5	pF

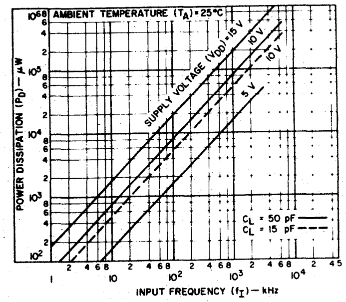


Fig. 9— Typical power dissipation as a function of input frequency.

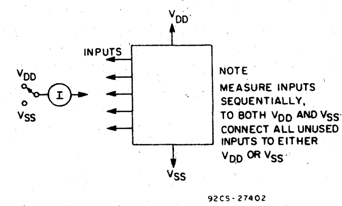


Fig. 10— Input leakage current test circuit.

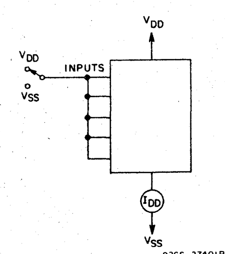


Fig. 11— Quiescent-device-current test circuit.

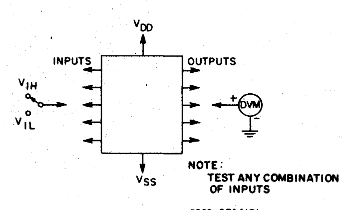
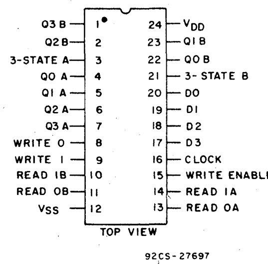


Fig. 12— Input-voltage test circuit.

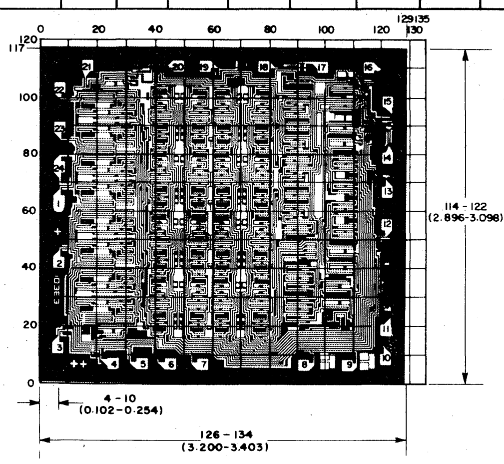
CD40108B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages Values at –40, +25, +85 Apply to E Package –55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5, 13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm10^{-4}$	±0.4	μA



TERMINAL ASSIGNMENT



Dimensions and Pad Layout for CD40108BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

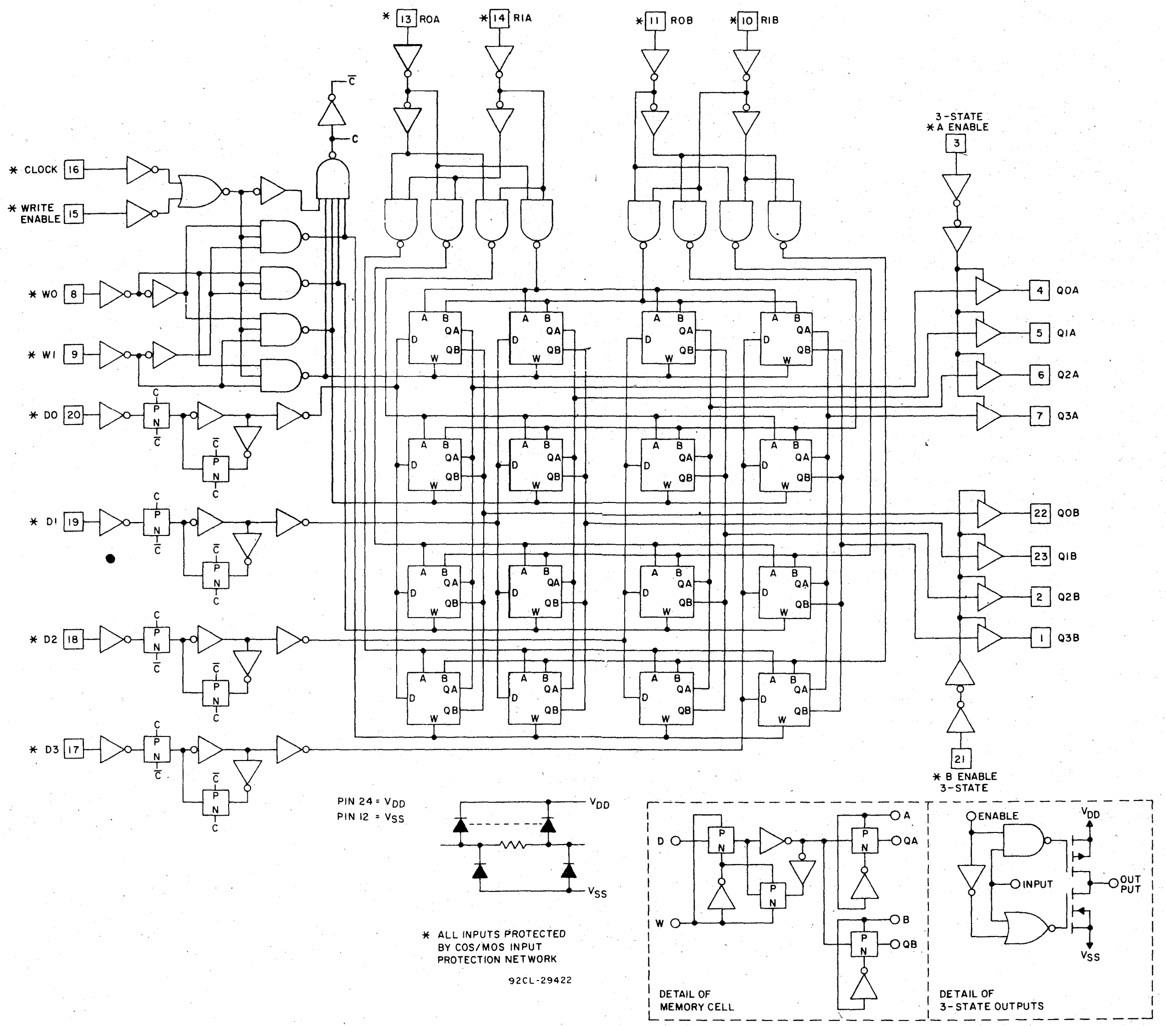
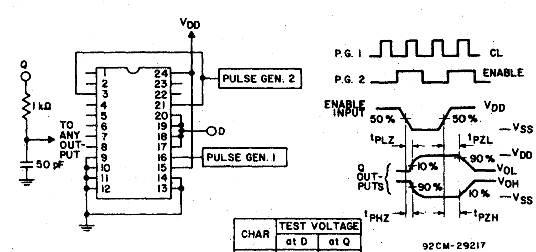


Fig. 13— Schematic diagram

92CL-29422



CHAR	TEST VOLTAGE at D	TEST VOLTAGE at Q
t_{PHZ}	V_{DD}	V_{SS}
t_{PZH}	V_{DD}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}
t_{PZL}	V_{SS}	V_{DD}

Fig. 14— Output-enable-delay-times test circuit and waveforms.

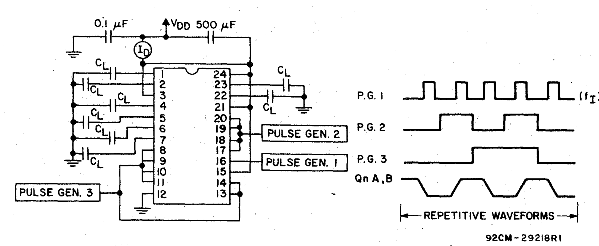


Fig. 15— Power-dissipation test circuit and waveforms.

CD40109B Types

COS/MOS Quad Low-to-High Voltage Level Shifter

High-Voltage Types (20-Volt Rating)

The RCA-CD40109B contains four low-to-high-voltage level-shifting circuits. Each circuit will shift a low-voltage digital-logic input signal (A, B, C, D) with logical 1 = V_{CC} and logical 0 = V_{SS} to a higher-voltage output signal (E, F, G, H) with logical 1 = V_{DD} and logical 0 = V_{SS}.

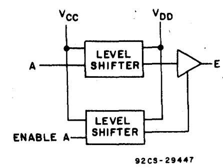
The RCA-CD40109, unlike other low-to-high level-shifting circuits, does not require the presence of the high-voltage supply (V_{DD}) before the application of either the low-voltage supply (V_{CC}) or the input signals. There are no restrictions on the sequence of application of V_{DD}, V_{CC}, or the input signals. In addition, there are no restrictions on the relative magnitudes of the supply voltages or input signals within the device maximum ratings; V_{CC} may exceed V_{DD}, and input signals may exceed V_{CC} and V_{DD}. When operated in the mode $V_{CC} > V_{DD}$, the CD40109 will operate as a high-to-low level-shifter.

The CD40109 also features individual three-state output capability. A low level on any of the separately enabled three-state output controls produces a high-impedance state in the corresponding output.

The CD40109B-Series types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Independence of power supply sequence considerations—V_{CC} can exceed V_{DD}, input signals can exceed both V_{CC} and V_{DD}**
- **Up and down level-shifting capability**
- **Three-state outputs with separate enable controls**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range)**
  = 1 V at V_{CC} = 5 V, V_{DD} = 10 V
  = 2 V at V_{CC} = 10 V, V_{DD} = 15 V
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM
(1 of 4 units)

Applications:

- **High-or-low level-shifting with three-state outputs for unidirectional or bidirectional bussing**
- **Isolation of logic subsystems using separate power supplies from supply sequencing, supply loss and supply regulation considerations**

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}, V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to +20 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

TRUTH TABLE

MODE	INPUTS		OUTPUTS
	A, B, C, D	ENABLE A, B, C, D	E, F, G, H
Low-to-high level shift	0	1	0
	1	1	1
	X	0	Z

LOGIC 0 = LOW(V_{SS}) X = DON'T CARE Z = HIGH IMPEDANCE
LOGIC 1 = V_{CC} at INPUTS and V_{DD} at OUTPUTS

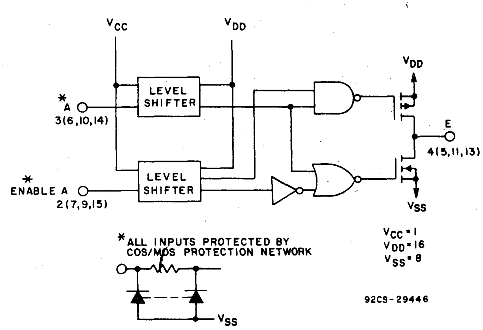


Fig. 1 — CD40109B logic diagram (1 of 4 units).

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.		0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	μA
	V_O (V)	V_{CC} (V)	V_{DD} (V)								
Input Low Voltage, V_{IL} Max.	1,9	5	10	1.5				–	–	1.5	V
	1.5, 13.5	10	15	3				–	–	3	
Input High Voltage, V_{IH} Min.	1,9	5	10	3.5				3.5	–	–	
	1.5,13.5	10	15	7				7	–	–	

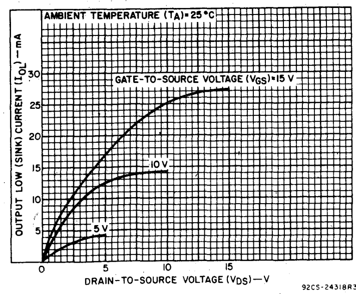


Fig.2 – Typical output low (sink) current characteristics.

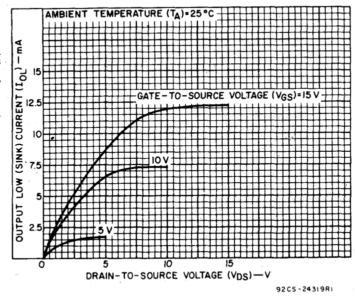


Fig.3 – Minimum output low (sink) current characteristics.

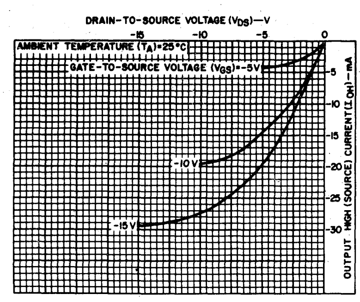


Fig.4 – Typical output high (source).

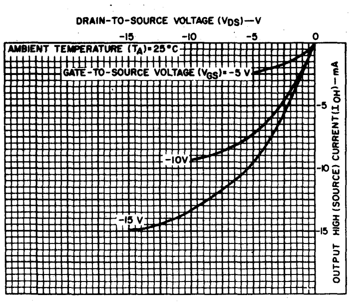


Fig.5 – Minimum output high (source) current characteristics.

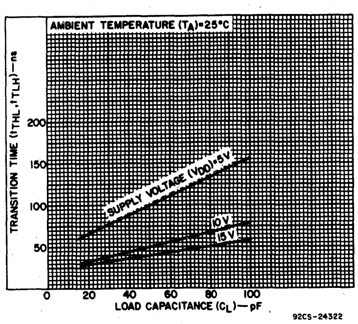


Fig.6 – Typical transition time as a function of load capacitance.

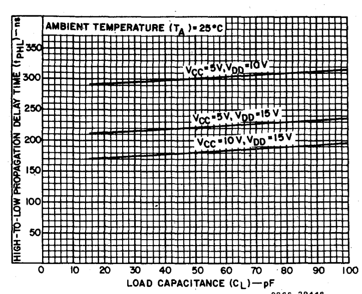


Fig.7 – Typical high-to-low propagation delay time as a function of load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	SHIFTING MODE	V_{CC} (V)	V_{DD} (V)	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay — Data Input to Output: High-to-Low Level, t_{PHL}	L–H	5	10	300	600	ns
		5	15	220	440	
		10	15	180	360	
	H–L	10	5	850	1600	
		15	5	850	1600	
		15	10	290	580	
Low-to-High Level, t_{PLH}	L–H	5	10	130	260	ns
		5	15	120	240	
		10	15	70	140	
	H–L	10	5	230	460	
		15	5	230	460	
		15	10	80	160	
3-State Disable Delay: Output High to High Impedance, t_{PHZ}	L–H	5	10	60	120	ns
		5	15	50	100	
		10	15	35	70	
	H–L	10	5	120	240	
		15	5	120	240	
		15	10	40	80	
Output Low to High Impedance, t_{PLZ}	L–H	5	10	370	740	ns
		5	15	300	600	
		10	15	250	500	
	H–L	10	5	850	1600	
		15	5	850	1600	
		15	10	350	700	
High Impedance to Output High, t_{PZH}	L–H	5	10	320	640	ns
		5	15	230	460	
		10	15	180	360	
	H–L	10	5	800	1500	
		15	5	800	1500	
		15	10	280	560	
High Impedance to Output Low, t_{PZL}	L–H	5	10	100	200	ns
		5	15	80	160	
		10	15	40	80	
	H–L	10	5	120	240	
		15	5	120	240	
		15	10	40	80	
Transition Time, t_{THL}, t_{TLH}	L–H	5	10	50	100	ns
		5	15	40	80	
		10	15	40	80	
	H–L	10	5	100	200	
		15	5	100	200	
		15	10	50	100	
Input Capacitance, C_I		Any Input		5	7.5	pF

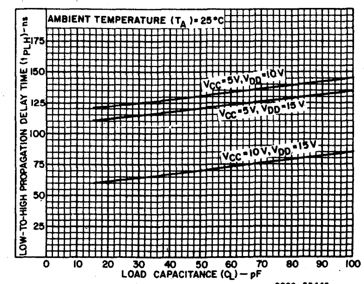


Fig.8 — Typical low-to-high propagation delay time as a function of load capacitance.

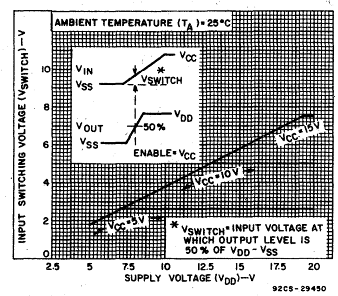


Fig.9 — Typical input switching as a function of high-level supply voltage.

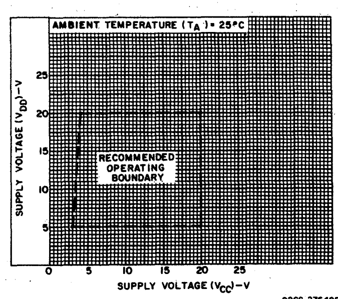


Fig. 10 — High-level supply voltage vs. low-level supply voltage.

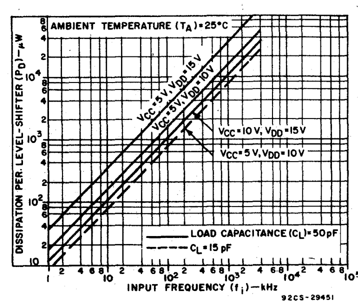
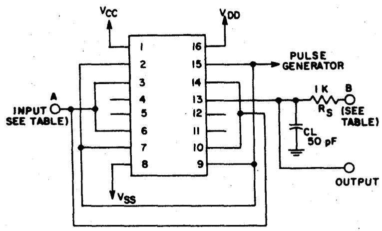


Fig.11 — Typical dynamic power dissipation as a function of input frequency.

TEST CIRCUITS



CHAR.	TEST VOLTAGE AT A	TEST VOLTAGE AT B
t_{PHZ}	V_{CC}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}
t_{PZL}	V_{SS}	V_{DD}
t_{PZH}	V_{CC}	V_{SS}

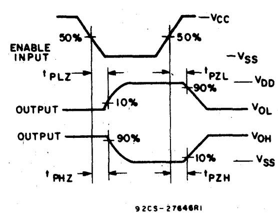


Fig. 12 – Output enable delay times test circuit and waveforms.

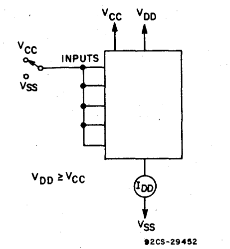


Fig. 13 – Quiescent device current.

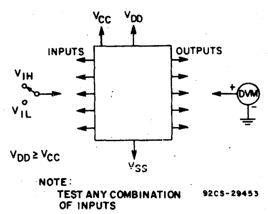


Fig. 14 – Input voltage.

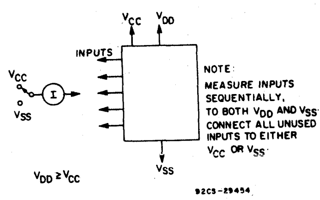


Fig. 15 – input current.

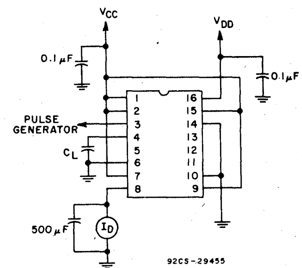
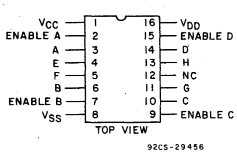


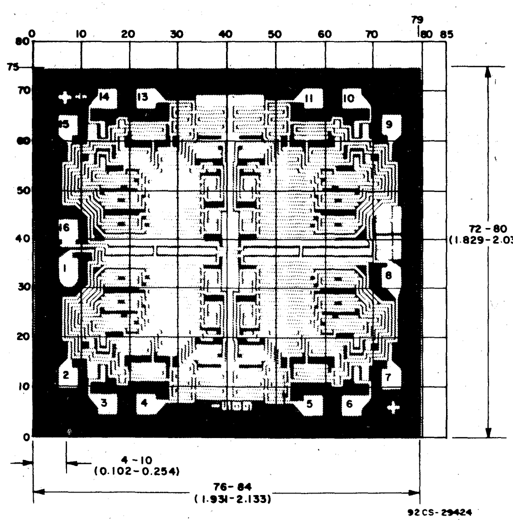
Fig. 16 – Dynamic power dissipation test circuit.



CD40109B TERMINAL ASSIGNMENT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



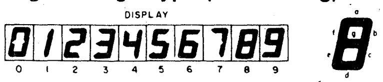
Dimensions and pad layout for CD40109BH.

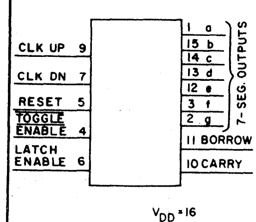
CD40110B Types

Preliminary Data

COS/MOS Decade Up-Down Counter/Decoder/Latch/Driver

High-Voltage Type (20-V Rating)





FUNCTIONAL DIAGRAM

92CS-31375

The RCA-CD40110B is a dual-clocked up/down counter with a special preconditioning circuit that allows the counter to be clocked, via positive going inputs, up or down regardless of that state or timing (within 100 ns typ.) of the other clock line.

The clock signal is fed into the control logic and Johnson counter after it is preconditioned. The outputs of the Johnson counter (which include anti-lock gating to avoid being locked at an illegal state) are fed into a latch. This data can be fed directly to the decoder through the latch or can be strobed to hold a particular count while the Johnson counter continues to be clocked. The decoder feeds a seven-segment bipolar output driver which can source up to 25 mA to drive LEDs and other displays such as low-voltage fluorescent and incandescent lamps.

A short duration negative-going pulse appears on the BORROW output when the count changes from 0 to 9 or the CARRY output when the count changes from 9 to 0. At the other times the BORROW and CARRY output are a logic 1.

The CARRY and BORROW outputs can be tied directly to the clock-up and clock-down lines respectively of another CD40110B for easy cascading of several counters.

The CD40110B types are supplied in 16-lead dual-in-line ceramic packages (D and F suffixes), and 16-lead dual-in-line plastic package (E suffix).

Applications:

- **Rate comparators**
- **General counting applications where display is desired**
- **Up/down counting applications where input pulses are random in nature**

Features:

- **Separate clock-up and clock-down lines**
- **Capable of driving common cathode LEDs and other displays directly**
- **Allows cascading without any external circuitry**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) =**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **5-V, 10-V and 15-V parametric ratings**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) .... −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT .... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C
(PACKAGE TYPE E) .... Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) .... 500 mW
For T_A = +100 to +125°C
(PACKAGE TYPES D,F) .... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE
(All Package Types) .... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D,F,H .... −55 to +125°C
PACKAGE TYPE E .... −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)
from case for 10 s max. .... +265°C

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:*

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL TYPES		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions				Limits at Indicated Temperatures (°C) Values at –55, +25, +125 for D,F,H Packages; Values at –40, +25, +85 for E Packages							UNITS
	I_{OH} (mA)	V_o (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quescent Device Current: I_{DD} Max.	–	–	–	5	5	5	150	150	–	0.04	5	μA
	–	–	–	10	10	10	300	300	–	0.04	10	
	–	–	–	15	20	20	600	600	–	0.04	20	
	–	–	–	20	100	100	3000	3000	–	0.08	100	
Output Voltage: Low-Level V_{OL} Max.	–	–	0,5	5	0.05				–	0	0.05	V
	–	–	0,10	10	0.05				–	0	0.05	
	–	–	0,15	15	0.05				–	0	0.05	
High-Level V_{OH} Min.	–	–	0,5	5	–	–	–	–	–	4.55	–	V
	–	–	0,10	10	–	–	–	–	–	9.55	–	
	–	–	0,15	15	–	–	–	–	–	14.55	–	
Input Low Voltage, V_{IL} Max.	–	0.5,3.8	–	5	1.5				–	–	1.5	V
	–	1,8.8	–	10	3				–	–	3	
	–	1.5,13.8	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	–	0.5,3.8	–	5	3.5				3.5	–	–	V
	–	1,8.8	–	10	7				7	–	–	
	–	1.5,13.8	–	15	11				11	–	–	
Output Drive Voltage V_{OH} Min.	0	–	–	5	–	–	–	–	–	4.55	–	V
	10	–	–	5	–	–	–	–	–	4.13	–	
	25	–	–	5	–	–	–	–	–	3.64	–	
	0	–	–	10	–	–	–	–	–	9.55	–	
	10	–	–	10	–	–	–	–	–	9.25	–	
	25	–	–	10	–	–	–	–	–	8.85	–	
	0	–	–	15	–	–	–	–	–	14.55	–	
	10	–	–	15	–	–	–	–	–	14.21	–	
	25	–	–	15	–	–	–	–	–	13.9	–	
Output Low (Sink) Current, I_{OL} Min.	–	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	–	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	–	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Input Current, I_{IN} Max.	–	0,18	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

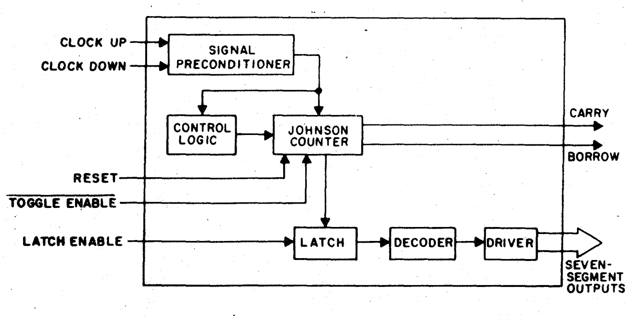


Fig. 1—Functional diagram.

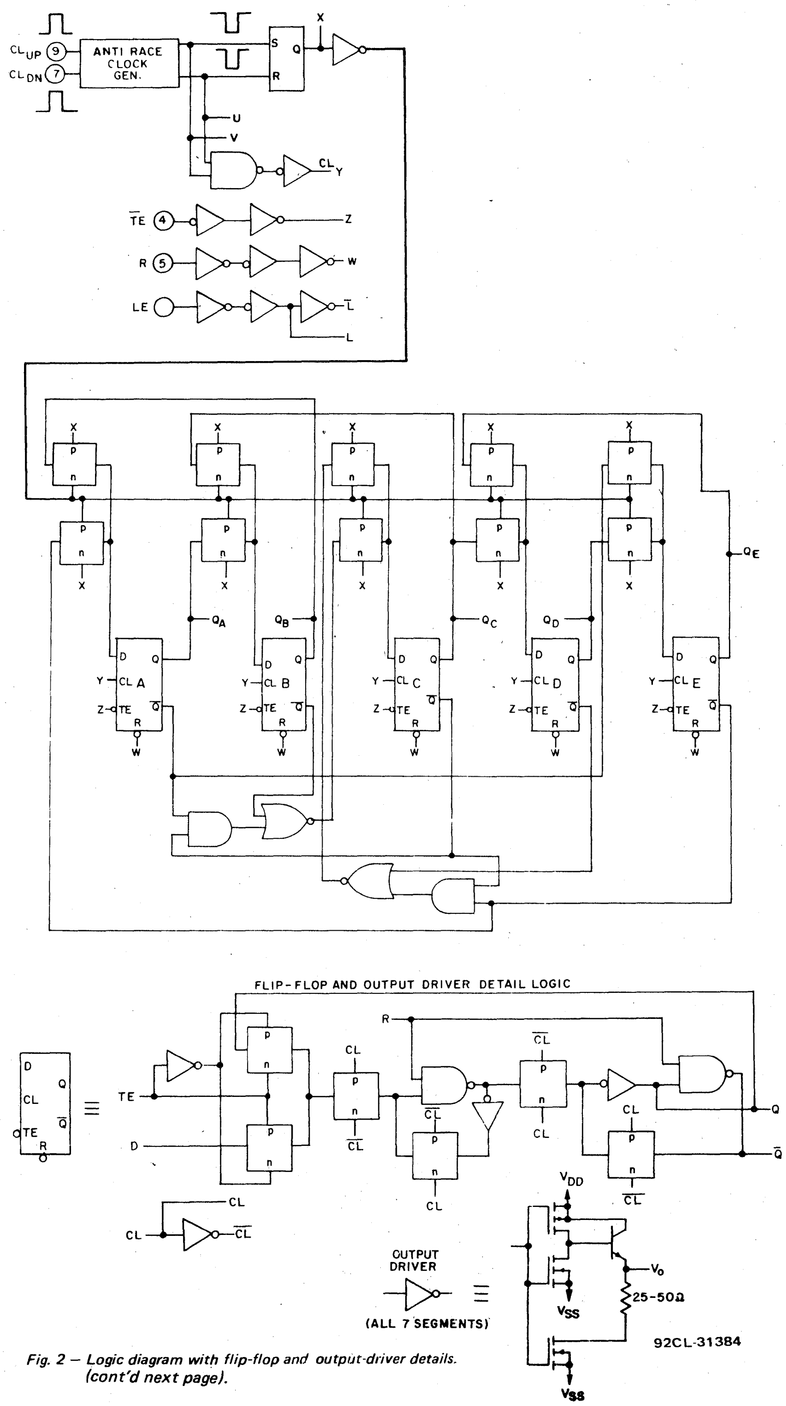
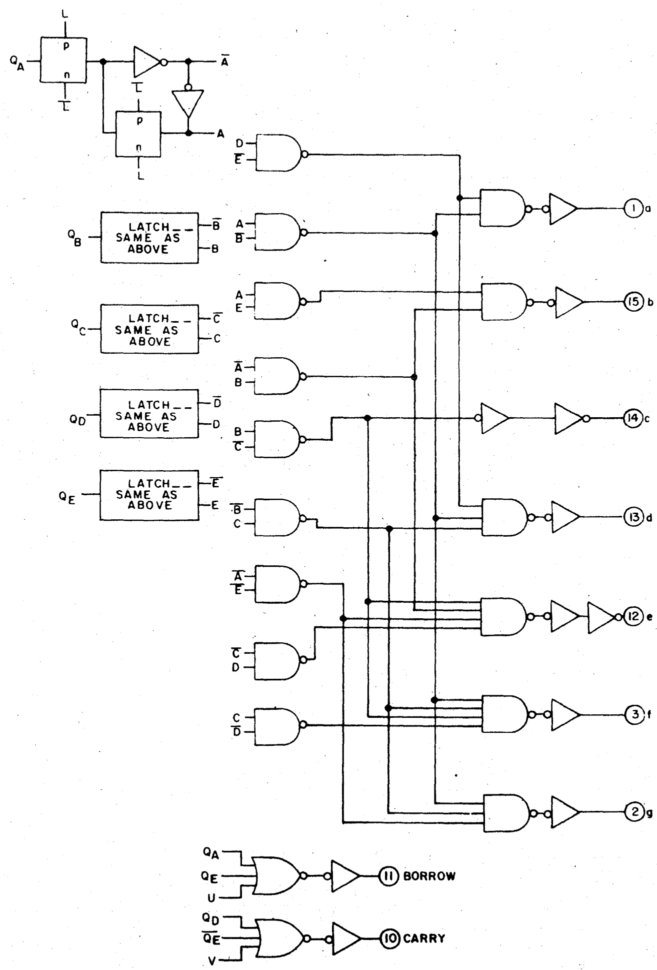


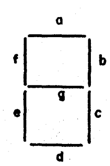
Fig. 2 – Logic diagram with flip-flop and output-driver details.
(cont'd next page).



92CL-31384

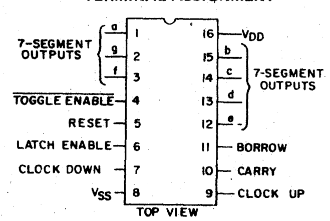
Fig.2 – Logic diagram with flip-flop and output-driver details (cont'd from previous page).

DISPLAY SEGMENTS



92CS-31376

TERMINAL ASSIGNMENT

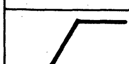


92CS-31377

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	Test Conditions V_{DD} Volts	LIMITS All Packages Typ.	UNITS
Clock Up/Clock Down			
Minimum Pulse Width	5 10 15	85 35 15	ns
Maximum Frequency	5 10 15	2.5 5 8	MHz
Minimum CARRY Pulse Width	5 10 15	225 100 70	ns
Minimum BORROW Pulse Width	5 10 15	260 110 80	ns
Reset			
Propagation Delay Time Reset to Clock t_{PHL}, t_{PLH}	5 10 15	750 285 200	ns
Delay from Reset to first allowable Clock	5 10 15	300 125 75	ns
Minimum Pulse Width	5 10 15	150 60 40	ns

TRUTH TABLE

CLOCK UP*	CLOCK DOWN*	LATCH ENABLE	$\overline{\text{TOGGLE ENABLE}}$	RESET	COUNTER	DISPLAY
	X	0	0	0	Increments by 1	Follows Counter
X		0	0	0	Decrements by 1	Follows Counter
		X	X	0	No Change	No Change
X	X	X	X	1	Goes to 00000	Follows Counter (Display = [illegible])
X	X	X	1	0	Inhibited	Remains Fixed
	X	1	0	0	Increments by 1	Remains Fixed
X		1	0	0	Decrements by 1	Remains Fixed

X = Don't care 1 ≡ High State 0 ≡ Low State

* Typically 100 ns between clock-up and clock-down positive transitions are required to ensure proper counting.

10-Line to 4-Line BCD Priority Encoder

High-Voltage Types (20-Volt Rating)

The RCA-CD40147B COS/MOS encoder features priority encoding of the inputs to ensure that only the highest-order data line is encoded. Ten data input lines (0-9) are encoded to four-line (8,4,2,1) BCD. The highest priority line is line 9. All four output lines are logic 1 (V_{SS}) when all input lines are logic 0. All inputs and outputs are buffered, and each output can drive one TTL low-power Schottky load. The CD40147B is functionally similar to the TTL 54/74147 if pin 15 is tied low.

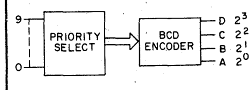
The CD40147B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

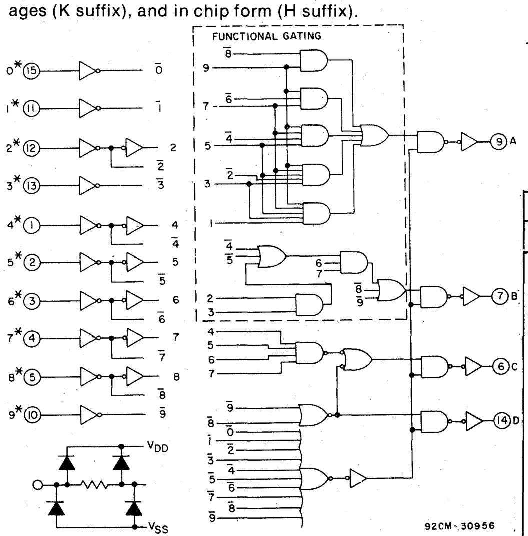
- Encodes 10-line to 4-line BCD
- Active low inputs and outputs
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V

Applications:

- Keyboard encoding
- 10-line to BCD encoding
- Range selection



FUNCTIONAL DIAGRAM



* INPUTS PROTECTED BY COS/MOS PROTECTION NETWORK

Fig. 1 – CD40147B logic diagram.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS Min.	LIMITS Max.	UNITS
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

TRUTH TABLE (Negative Logic)

INPUTS 0	1	2	3	4	5	6	7	8	9	OUTPUTS D	C	B	A
0	0	0	0	0	0	0	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0
X	1	0	0	0	0	0	0	0	0	0	0	0	1
X	X	1	0	0	0	0	0	0	0	0	0	1	0
X	X	X	1	0	0	0	0	0	0	0	0	1	1
X	X	X	X	1	0	0	0	0	0	0	1	0	0
X	X	X	X	X	1	0	0	0	0	0	1	0	1
X	X	X	X	X	X	1	0	0	0	0	1	1	0
X	X	X	X	X	X	X	1	0	0	0	1	1	1
X	X	X	X	X	X	X	X	1	0	1	0	0	0
X	X	X	X	X	X	X	X	X	1	1	0	0	1

0 = High Level 1 = Low Level X = Don't Care

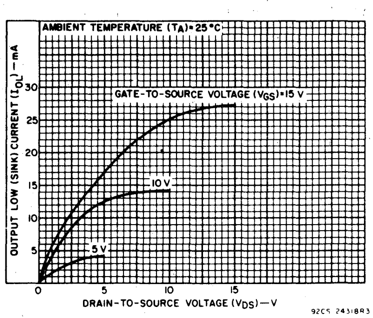


Fig. 2 – Typical output low (sink) current characteristics.

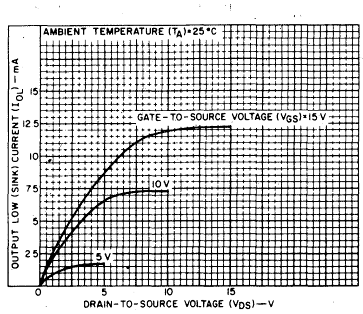


Fig. 3 – Minimum output low (sink) current characteristics.

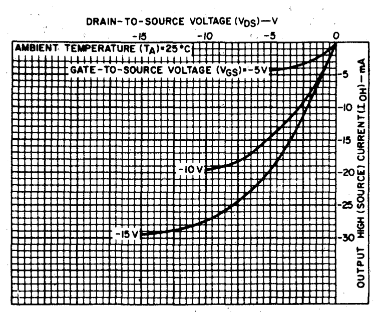


Fig. 4 – Typical output high (source) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . . . +265°C

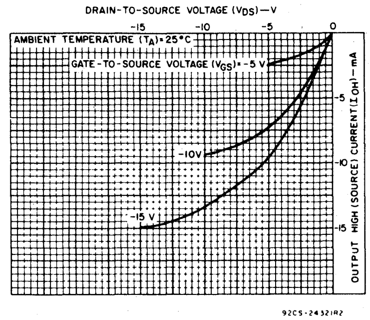


Fig. 5 — Minimum output high (source) current characteristics.

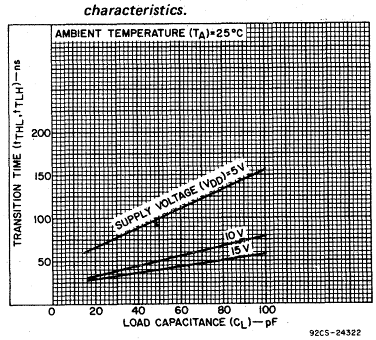


Fig. 6 — Typical transition time as a function of load capacitance.

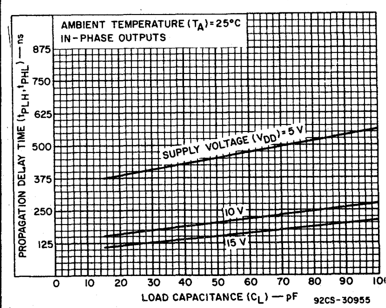


Fig. 7 — Propagation delay time as a function of load capacitance.

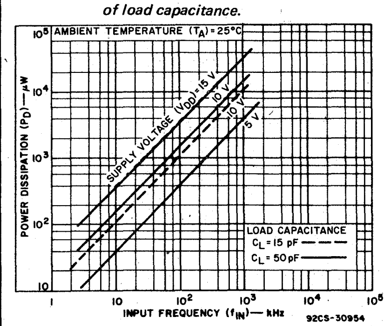


Fig. 8 — Typical dynamic power dissipation as a function of input frequency.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	µA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6		
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8		
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	µA

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS ALL TYPES		UNITS
		V_{DD} (V)	Typ.	Max.	
Propagation Delay Time, t_{PLH}, t_{PHL} In-Phase Output	Any input to any output	5	450	900	ns
		10	200	400	
		15	150	300	
Out-of-Phase Output		5	425	850	ns
		10	175	350	
		15	125	250	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_1	Any Input		5	7.5	pF

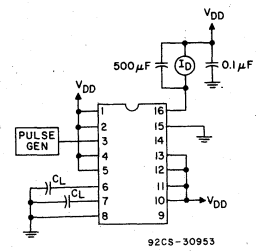


Fig. 9 – Dynamic power dissipation test circuit.

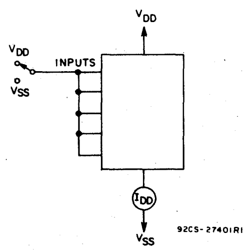


Fig. 10 – Quiescent device current test circuit.

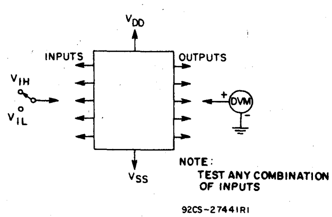


Fig. 11 – Input voltage test circuit.

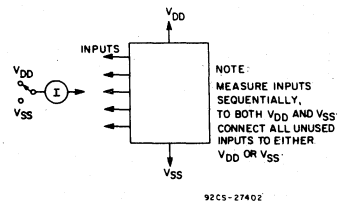
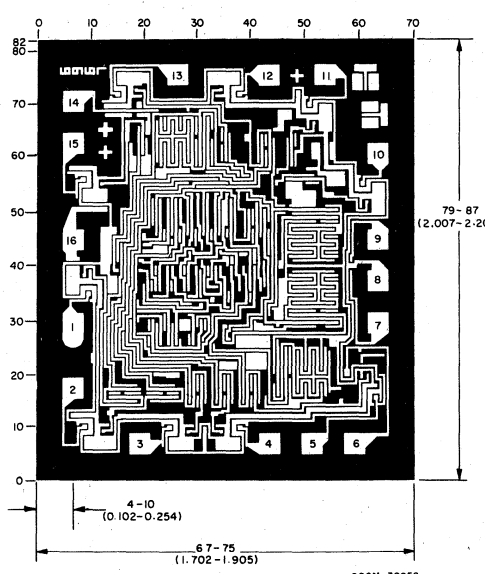
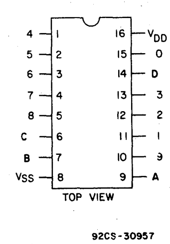


Fig. 12 – Input current test circuit.





CD40147B TERMINAL ASSIGNMENT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for CD40147BH

CD40160B, CD40161B, CD40162B, CD40163B Types

COS/MOS Synchronous Programmable 4-Bit Counters

High-Voltage Types (20-Volt Rating)

CD40160B – Decade with Asynchronous Clear
CD40161B – Binary with Asynchronous Clear
CD40162B – Decade with Synchronous Clear
CD40163B – Binary with Synchronous Clear

RCA-CD40160B, CD40161B, CD40162B, and CD40163B are 4-bit synchronous programmable counters. The CLEAR function of the CD40162B and CD40163B is synchronous and a low level at the $\overline{CLEAR}$ input sets all four outputs low on the next positive CLOCK edge. The CLEAR function of the CD40160B and CD40161B is asynchronous and a low level at the $\overline{CLEAR}$ input sets all four outputs low regardless of the state of the CLOCK, $\overline{LOAD}$, or ENABLE inputs. A low level at the $\overline{LOAD}$ input disables the counter and causes the output to agree with the setup data after the next CLOCK pulse regardless of the conditions of the ENABLE inputs.

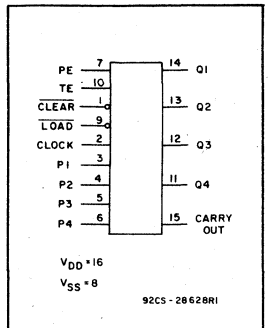
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output (C_{OUT}). Counting is enabled when both PE and TE inputs are high. The TE input is fed forward to enable C_{OUT}. This enabled output produces a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages. Logic transitions at the PE or TE inputs may occur when the clock is either high or low.

The CD40160B, CD40161B, CD40162B, and CD40163B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

The CD40160B through CD40163B types are functionally equivalent to and pin-compatible with the TTL counter series 74160 through 74163 respectively.

Features:

- **Internal look-ahead for fast counting**
- **Carry output for cascading**
- **Synchronously programmable**
- **Clear asynchronous input (CD40160B, CD40161B)**
- **Clear synchronous input (CD40162B, CD40163B)**
- **Synchronous load control input**
- **Low-power TTL compatibility**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



Functional Diagram

Applications:

- **Programmable binary and decade counting**
- **Counter control/timers**
- **Frequency dividing**

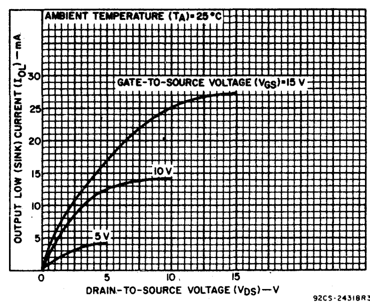


Fig. 1— Typical output low (sink) current characteristics.

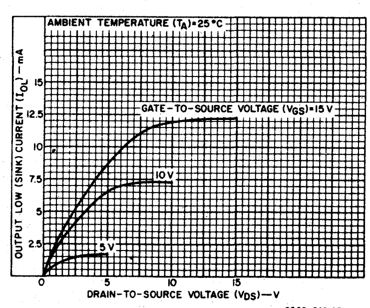


Fig. 2— Minimum output low (sink) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

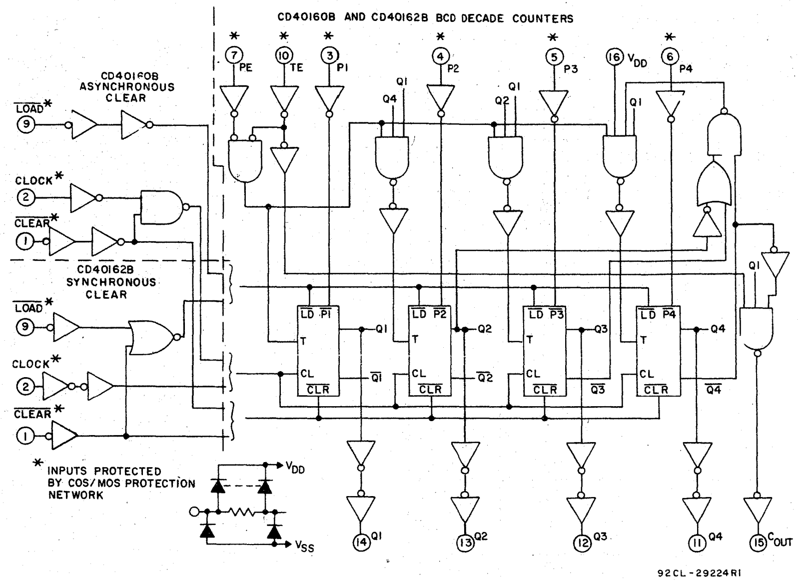


Fig. 3— Logic diagrams for CD40160B and CD40162B BCD decade counters.

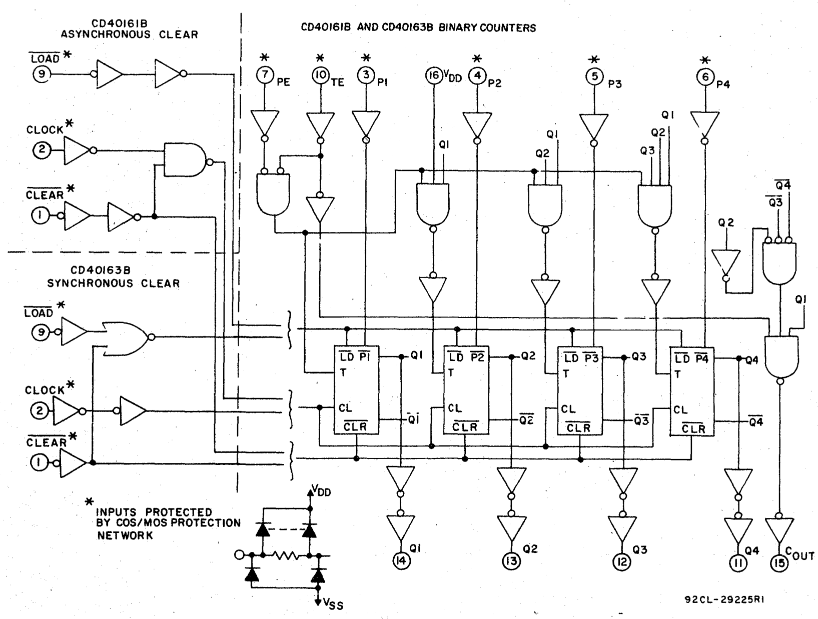


Fig. 4— Logic diagrams for CD40161B and CD40163B binary counters.

CD40160B, CD40161B, CD40162B, CD40163B Types

RECOMMENDED OPERATING CONDITIONS *at $T_A = 25^oC$, Except as Noted*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply Voltage Range (Full T_A = Full Package-Temperature Range)	–	3	18	V
Setup Time: t_{SU} Data to Clock	5 10 15	240 90 60	– – –	ns
$\overline{Load}$ to Clock	5 10 15	240 90 60	– – –	ns
PE or TE to Clock	5 10 15	340 140 100	– – –	ns
$\overline{Clear}$ to Clock (CD40162B, CD40163B)	5 10 15	340 140 100	– –	ns
All Hold Times, t_H	5 10 15	0 0 0	– – –	ns
$\overline{Clear}$ Removal Time, t_{rem} (CD40160B, CD40161B)	5 10 15	200 100 70	– – –	ns
$\overline{Clear}$ Pulse Width, t_{WL} (CD40160B, CD40161B)	5 10 15	170 70 50	– – –	ns
Clock Input Frequency, f_{CL}	5 10 15	– – –	2 5.5 8	MHz
Clock Pulse Width, t_W	5 10 15	170 70 50	– – –	ns
Clock Rise or Fall Time, t_rCL or t_fCL	5 10 15	– – –	200 70 15	μs

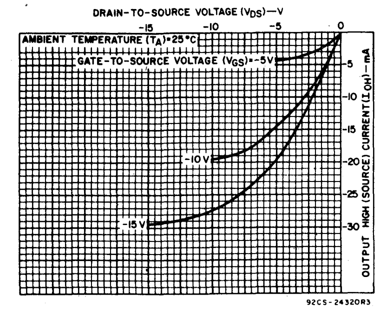


Fig. 5— Typical output high (source) current characteristics.

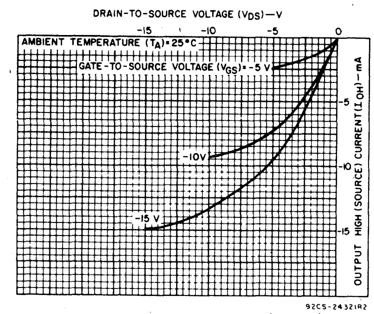


Fig. 6— Minimum output high (source) current characteristics.

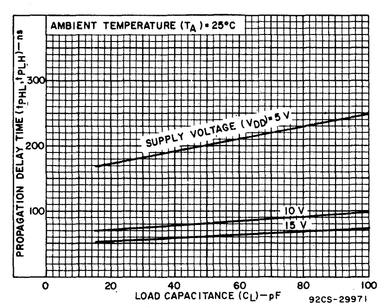


Fig. 7— Typical propagation delay time as a function of load capacitance (CLOCK to Q).

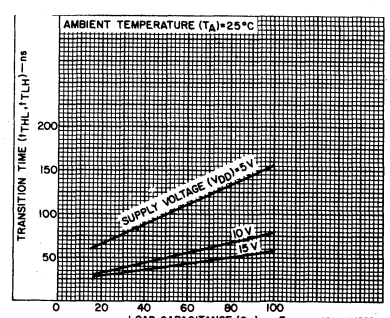


Fig. 8— Typical transition time as a function of load capacitance.

TRUTH TABLE

CLOCK	$\overline{CLR}$	$\overline{LOAD}$	PE	TE	OPERATION
↑	1	0	X	X	PRESET
↑	1	1	0	X	NC
↑	1	1	X	0	NC
↑	1	1	1	1	COUNT
X	0	X	X	X	RESET (CD40160B, CD40161B)
↑	0	X	X	X	RESET (CD40162B, CD40163B)
↓	1	X	X	X	NC (CD40162B, CD40163B)

1 = HIGH LEVEL 0 = LOW LEVEL X = DON'T CARE NC = NO CHANGE

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages; Values at –40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

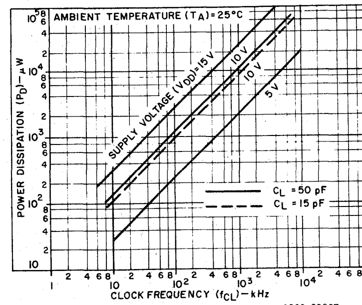


Fig. 9– Typical power dissipation as a function of CLOCK frequency.

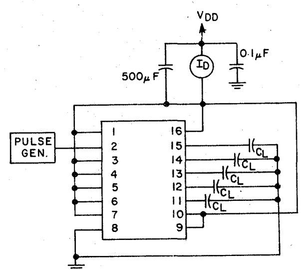


Fig. 10– Dynamic power dissipation test circuit.

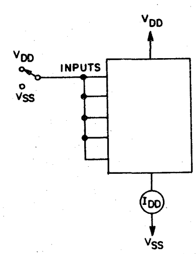


Fig. 11– Quiescent-device-current test circuit.

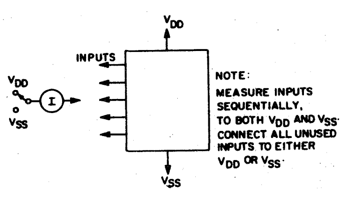


Fig. 12– Input-current test circuit.

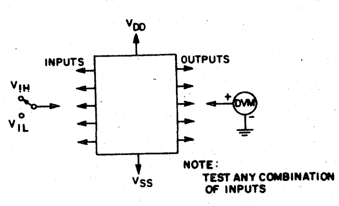
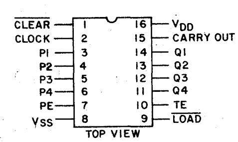


Fig. 13– Input-voltage test circuit.

TERMINAL ASSIGNMENT



DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C;
Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS ALL TYPES* Min.	Typ.	Max.	UNITS
CLOCK OPERATION					
Propagation Delay Time, t_{PHL},t_{PLH} Clock to Q	5	–	200	400	ns
	10	–	80	160	
	15	–	60	120	
Clock to C_{OUT}	5	–	225	450	ns
	10	–	95	190	
	15	–	70	140	
TE to C_{OUT}	5	–	125	250	ns
	10	–	55	110	
	15	–	40	80	
Minimum Setup Time, t_{SU} Data to Clock	5	–	120	240	ns
	10	–	45	90	
	15	–	30	60	
$\overline{Load}$ to Clock	5	–	120	240	ns
	10	–	45	90	
	15	–	30	60	
PE to TE to Clock	5	–	170	340	ns
	10	–	70	140	
	15	–	50	100	
Minimum Hold Time, t_H	5	–	–	0	ns
	10	–	–	0	
	15	–	–	0	
Transition Time, t_{THL},t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Minimum Clock Pulse Width, t_W	5	–	85	170	ns
	10	–	35	70	
	15	–	25	50	
Maximum Clock Frequency, f_{CL}	5	2	3	–	MHz
	10	5.5	8.5	–	
	15	8	12	–	
Maximum Clock Rise or Fall Time,† t_rCL, t_fCL	5	200	–	–	µs
	10	70	–	–	
	15	15	–	–	
CLEAR OPERATION					
Propagation Delay Time, t_{PHL} (CD40160B, CD40161B) $\overline{Clear}$ to Q	5	–	250	500	ns
	10	–	110	220	
	15	–	80	160	
Minimum Setup Time, t_{SU} (CD40162B, CD40163B) $\overline{Clear}$ to Clock	5	–	170	340	ns
	10	–	70	140	
	15	–	50	100	
Minimum Hold Time, t_H (CD40162B, CD40163B) $\overline{Clear}$ to Clock	5	–	–	0	ns
	10	–	–	0	
	15	–	–	0	
Minimum $\overline{Clear}$ Removal Time, t_{rem} (CD40160B, CD40161B)	5	–	100	200	ns
	10	–	50	100	
	15	–	35	70	
Minimum $\overline{Clear}$ Pulse Width, t_{WL} (CD40160B, CD40161B)	5	–	85	170	ns
	10	–	35	70	
	15	–	25	50	

* Except as noted.
† If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the carry output driving stage for the estimated capacitive load.

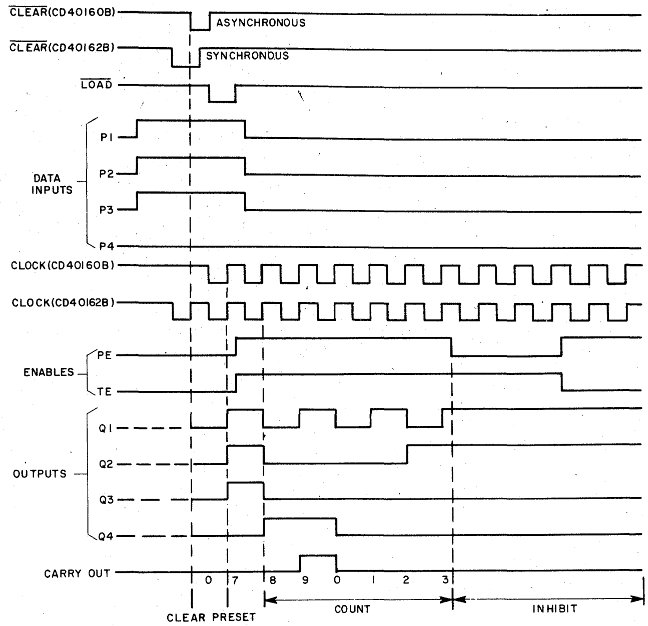


Fig. 14— Timing diagram for CD40160B, CD40162B.

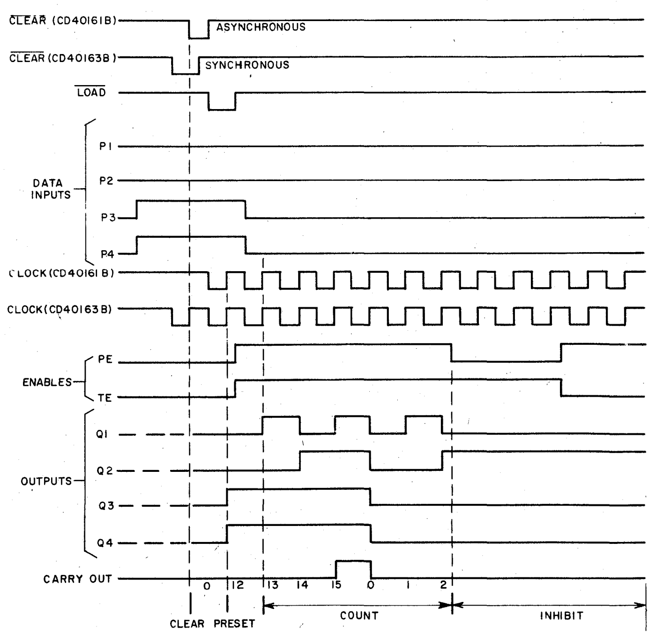


Fig. 15— Timing diagram for CD40161B, CD40163B.

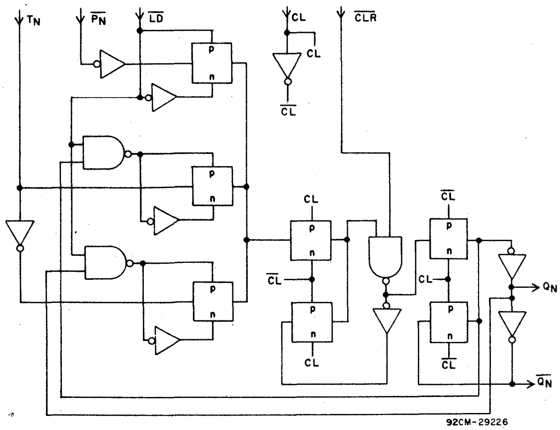


Fig. 16— Detail of flip-flops of CD40160B and CD40161B (asynchronous clear).

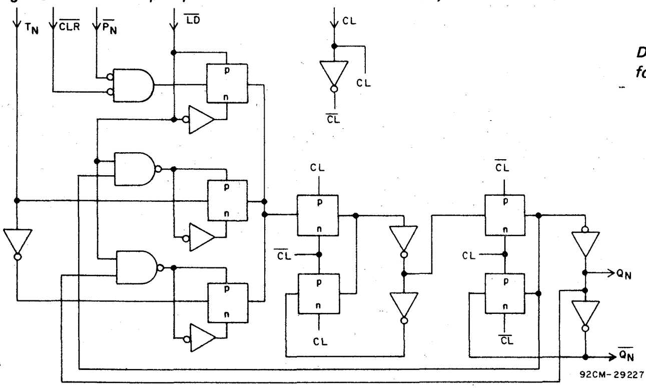
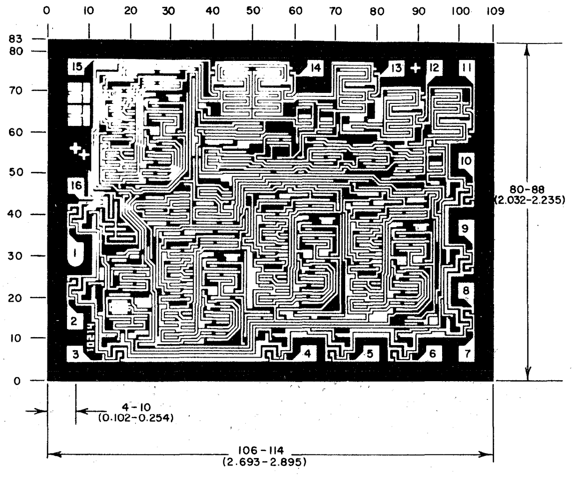


Fig. 17— Detail of flip-flops for CD40162B and CD40163B (synchronous clear).



Dimensions and pad layout for CD40160BH. Dimensions and pad layout for CD40161BH, CD40162BH, and CD40163BH are identical.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

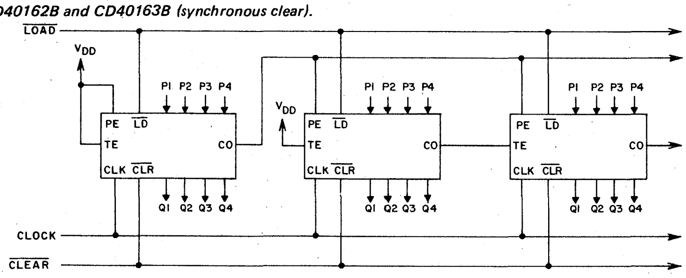


Fig. 18 – Cascaded counter packages in the parallel-clocked mode.

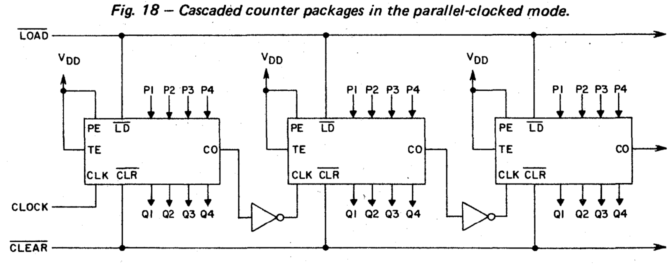


Fig. 19 – Cascaded counter packages in the ripple-clocked mode.

COS/MOS Hex 'D'-Type Flip-Flop

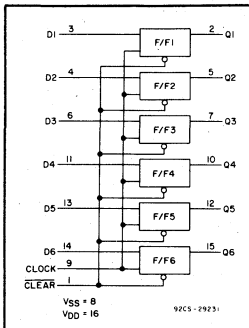
High-Voltage Types (20-Volt Rating)

The RCA-CD40174B consists of six identical 'D'-type flip-flops having independent DATA inputs. The CLOCK and $\overline{\text{CLEAR}}$ inputs are common to all six units. Data is transferred to the Q outputs on the positive-going transition of the clock pulse. All six flip-flops are simultaneously reset by a low level on the $\overline{\text{CLEAR}}$ input.

The CD40174B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- 5-V, 10-V, and 15-V parametric rating
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



FUNCTIONAL DIAGRAM

Applications:

- Shift Registers
- Buffer/Storage Registers
- Pattern Generators

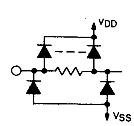
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . −55 to +125°C
PACKAGE TYPE E . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . +265°C

TRUTH TABLE FOR 1 OF 6 FLIP-FLOPS

INPUTS			OUTPUT
CLOCK	DATA	$\overline{\text{CLEAR}}$	Q
↑	0	1	0
↑	1	1	1
↓	X	1	NC
X	X	0	0

1 = High Level X = Don't Care
0 = Low Level NC = No Change



*ALL INPUTS (TERMS 1,3,4,6,9, 11, 13, 14) PROTECTED BY COS/MOS PROTECTION NETWORK

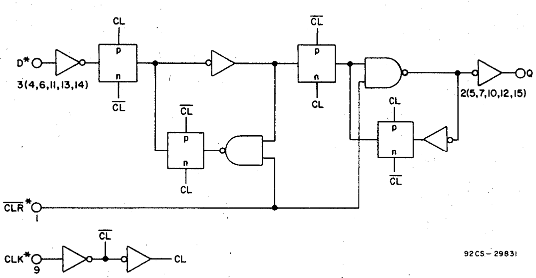


Fig. 1 – Logic diagram (1 of 6 flip-flops).

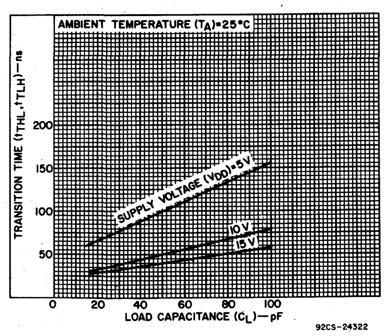
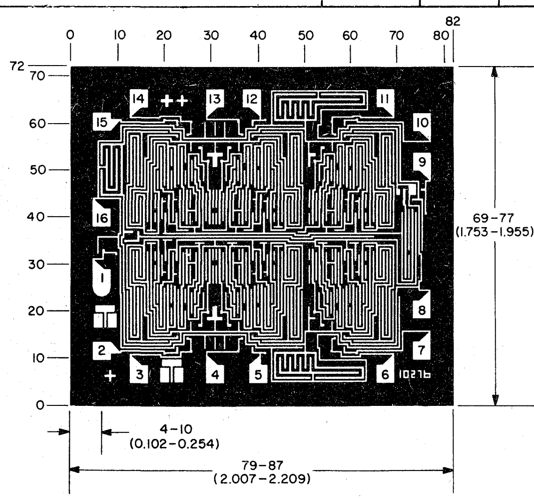


Fig. 2– Typical transition time as a function of load capacitance.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	–	3	18	V
Data Setup Time, t_{SU}	5 10 15	40 20 10	– – –	ns
Data Hold Time, t_H	5 10 15	80 40 30	– – –	ns
Clock Input Frequency, f_{CL}	5 10 15	– dc 	3.5 6 8	MHz
Clock Input Rise or Fall Time, t_rCL, t_fCL	5 10 15	– – –	15 15 15	μs
Clock Input Pulse Width, t_{WL}, t_{WH}	5 10 15	130 60 40	– – –	ns
$\overline{\text{Clear}}$ Pulse Width, t_{WL}	5 10 15	100 50 40	– – –	ns
$\overline{\text{Clear}}$ Removal Time, t_{REM}	5 10 15	0 0 0	– – –	ns



Dimensions and pad layout for CD40174BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

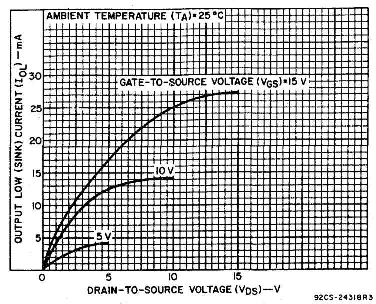


Fig. 3— Typical output low (sink) current characteristics.

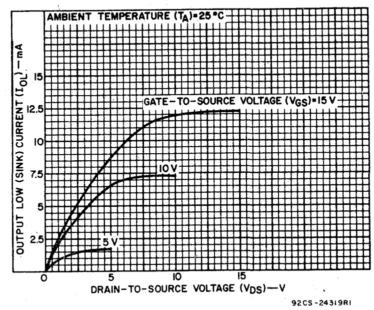


Fig. 4— Minimum output low (sink) current characteristics.

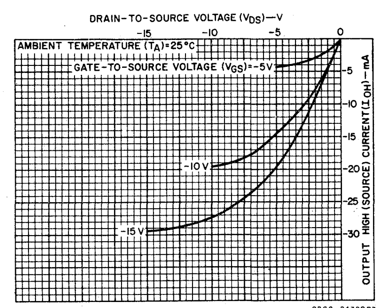


Fig. 5— Typical output high (source) current characteristics.

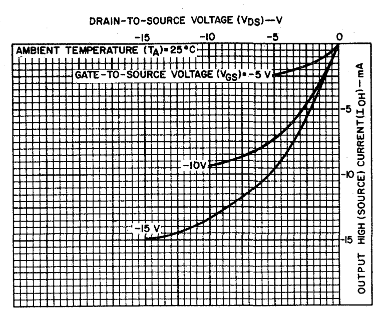


Fig. 6— Minimum output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D, F, H Packages; Values at –40, +25, +85 Apply to E Package: –55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	µA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6		
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8		
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–		0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	µA

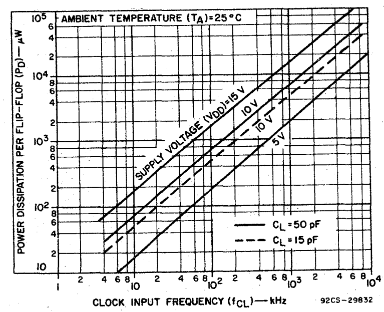


Fig. 7— Typical dynamic power dissipation as a function of CLOCK frequency.

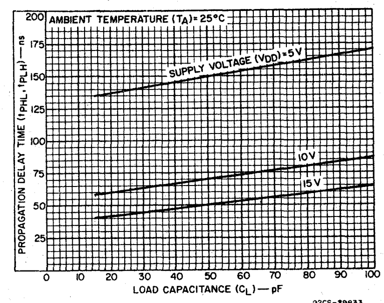


Fig. 8— Typical propagation delay time (CLOCK to OUTPUT) as a function of load capacitance.

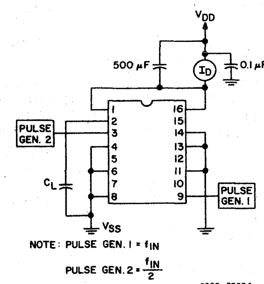


Fig. 9— Dynamic power dissipation test circuit.

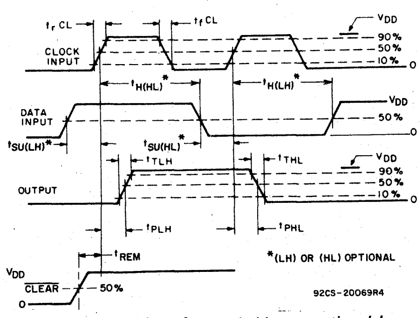


Fig. 10— Definition of setup, hold, propagation delay, and removal times.

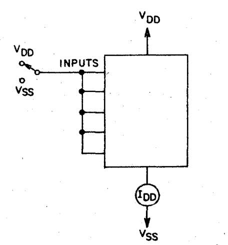


Fig. 11 — Quiescent device current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C;
Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time Clock to Output, t_{PHL}, t_{PLH}	5 10 15	– – –	150 70 50	300 140 100	ns
$\overline{Clear}$ to Output, t_{PHL}	5 10 15	– – –	100 50 40	200 100 80	ns
Transition Time, t_{THL}, t_{TLH}	5 10 15	– – –	100 50 40	200 100 80	ns
Minimum Pulse Width, Clock, t_{WL}, t_{WH}	5 10 15	– – –	65 30 20	130 60 40	ns
$\overline{Clear}$, t_{WL}	5 10 15	– – –	50 25 20	100 50 40	ns
Minimum Data Setup Time, t_{SU}	5 10 15	– – –	20 10 0	40 20 10	ns
Minimum Data Hold Time, t_H	5 10 15	– – –	40 20 15	80 40 30	ns
Maximum Clock Frequency, f_{CL}	5 10 15	3.5 6 8	7 12 16	– – –	MHz
Maximum Clock Rise or Fall Time, t_rCL, t_fCL	5 10 15	15 15 15	– – –	– – –	μs
Input Capacitance, C_{IN} $\overline{Clear}$	–	–	25	40	pF
All other	–	–	5	7.5	pF
Minimum $\overline{Clear}$ Removal Time, t_{REM}	5 10 15	– – –	–40 –15 –10	0 0 0	ns

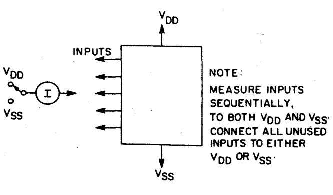


Fig. 12 – Input current test circuit.

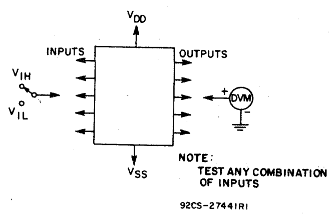
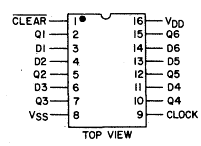


Fig. 13 – Input voltage test circuit.

TERMINAL ASSIGNMENT



COS/MOS 4-Bit Arithmetic Logic Unit

High-Voltage Types (20-Volt Rating)

The RCA-CD40181B is a low-power four-bit parallel arithmetic logic unit (ALU) capable of providing 16 binary arithmetic operations on two four-bit words and 16 logical functions of two Boolean variables. The mode control input M selects logical (M = High) or arithmetic (M = Low) operation. The four select inputs (S0, S1, S2, and S3) select the desired logical or arithmetic functions, which include AND, OR, NAND, NOR, and exclusive—OR and—NOR in the logic mode, and addition, subtraction, decrement, left-shift and straight transfer in the arithmetic mode, according to the truth table. The CD40181B operation may be interpreted with either active-low or active-high data at the A and B word inputs and the function outputs F, by using the appropriate truth table.

The CD40181B contains logic for full look-ahead carry operation for fast carry generation using the carry-generate and carry-propagate outputs $\overline{G}$ and $\overline{P}$ for the four bits of the CD40181B. Use of the CD40182B look-ahead carry generator in conjunction with multiple CD40181B'S permits high-speed arithmetic operations on long words. A ripple carry output C_{n+4} is available for use in systems where speed is not of primary importance.

Also included in the CD40181B is a comparator output A = B, which assumes a high level whenever the two four-bit input words A and B are equal and the device is in the subtract mode. In addition, relative magnitude information may be derived from the carry-in input C_n and ripple carry-out output C_{n+4} by placing the unit in the subtract mode and externally decoding using the information in Table III.

The CD40181B types are supplied in 24-lead hermetic ceramic dual-in-line packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

The CD40181 is similar to industry types MC14581 and 74181.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

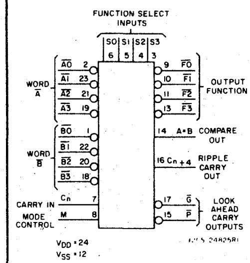
CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

Features:

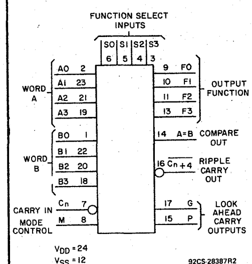
- Full look-ahead carry for speed operations on long words
- Generates 16 logic functions of two Boolean variables
- Generates 16 arithmetic functions of two 4-bit binary words
- A = B comparator output available
- Ripple-carry input and output available
- Typical addition time 200 ns @ V_{DD} = 10 V
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package temperature range)
  = 1 V at V_{DD} = 5 V
  = 2 V at V_{DD} = 10 V
  = 2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Parallel arithmetic units
- Process controllers
- Low-power minicomputers



(Active-low data)
FUNCTIONAL DIAGRAM



(Active-high data)
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	–0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	–55 to +125°C
PACKAGE TYPE E	–40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	–65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

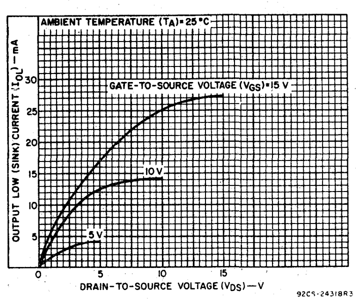


Fig. 1 — Typical output low (sink) current characteristics.

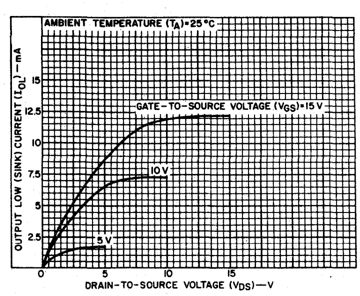


Fig. 2 — Minimum output low (sink) current characteristics.

CD40181B Types

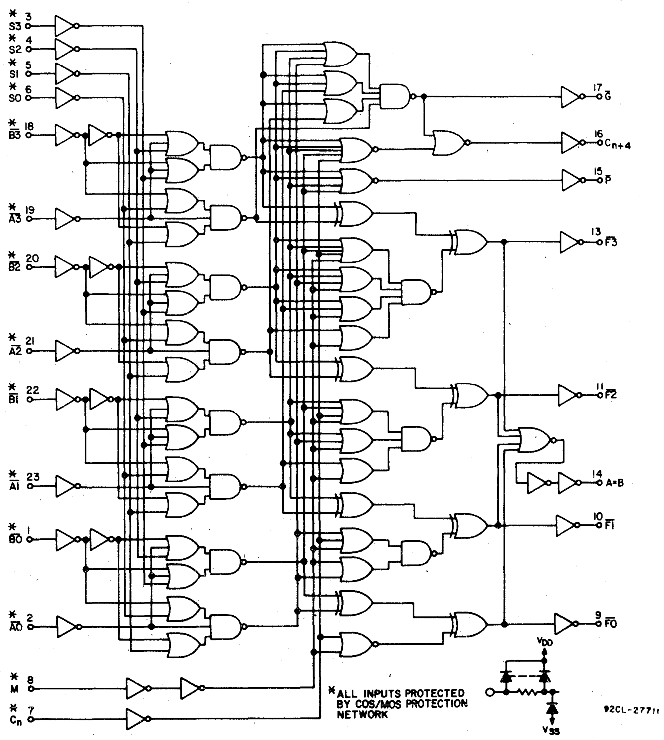


Fig. 3 — CD40181B logic diagram (active-low data).

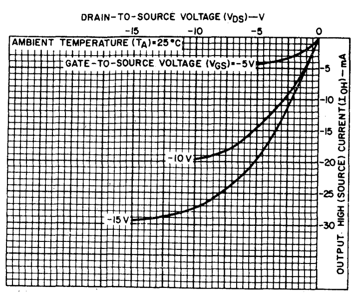


Fig. 4 — Typical output high (source) current characteristics.

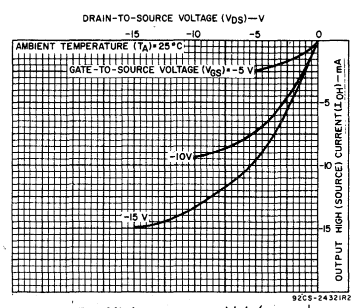


Fig. 5 — Minimum output high (source) current characteristics.

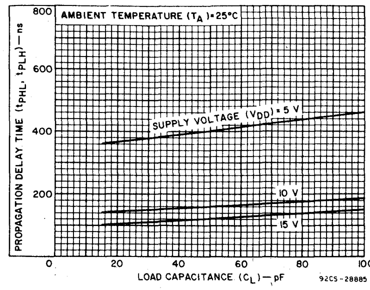


Fig. 6 — Typical propagation delay time as a function of load capacitance (for A or B to F, logic mode).

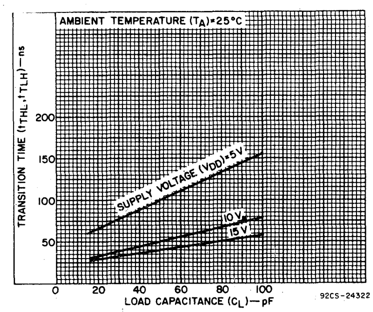


Fig. 7 — Typical transition time as a function of load capacitance.

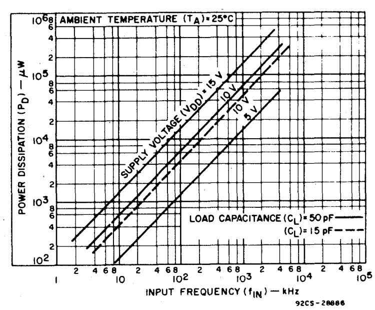


Fig. 8 — Typical dynamic dissipation as a function of input frequency (see Fig. 11 — dynamic power dissipation test circuit).

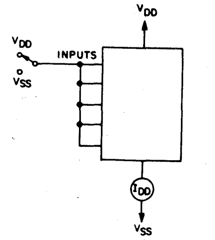


Fig. 9 — Quiescent-device-current test circuit.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages; Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

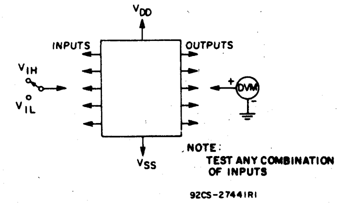
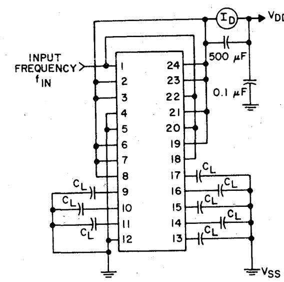


Fig. 10 – Input-voltage test circuit.



TEST CONDITIONS:
A0, A1, A2, A3, S0, S3, M, Cn = V_{DD}
B0, B1, B2, B3 = f_{IN}
S1, S2 = V_{SS}
(ALL OUTPUTS SWITCHING EXCEPT G)

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Fig. 11 – Dynamic power dissipation test circuit.

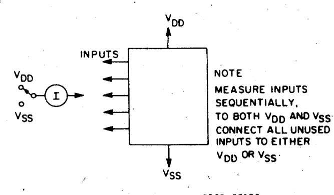
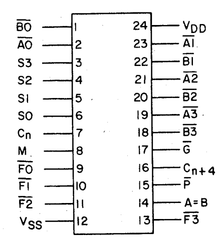


Fig. 12 – Input current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} A or B to F (logic mode), A or B to G or P,	5	400	800	ns
	10	160	320	
	15	120	240	
A or B to F, C_{n+4}, or A = B,	5	500	1000	ns
	10	200	400	
	15	140	280	
C_n to F	5	320	640	ns
	10	135	270	
	15	100	200	
C_n to C_{n+4}	5	200	400	ns
	10	100	200	
	15	70	140	
Transition Time: t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN} (Any Input)	–	5	7.5	pF

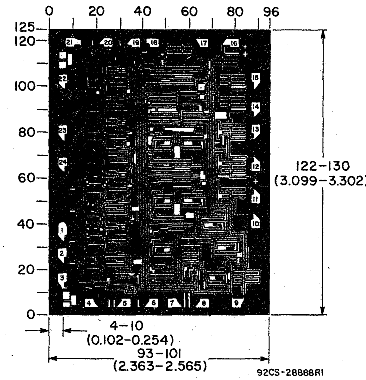


Top View

Terminal Assignment (Active-low Data)

TABLE I
TRUTH TABLE

FUNCTION SELECT				INPUTS/OUTPUT ACTIVE LOW		
				LOGIC FUNCTION	ARITHMETIC* FUNCTION M = L	
S3	S2	S1	S0	M = H	C_n = L	C_n = H
0	0	0	0	$\overline{A}$	A minus 1	A
0	0	0	1	$\overline{AB}$	AB minus 1	AB
0	0	1	0	$\overline{A}$ + B	$A\overline{B}$ minus 1	$A\overline{B}$
0	0	1	1	Logic 1	minus 1	Zero
0	1	0	0	$\overline{A + B}$	A plus (A + $\overline{B}$)	A plus (A + $\overline{B}$) plus 1
0	1	0	1	$\overline{B}$	AB plus (A + $\overline{B}$)	AB plus (A + $\overline{B}$) plus 1
0	1	1	0	$\overline{A \oplus B}$	A minus B minus 1	A minus B
0	1	1	1	A + $\overline{B}$	A + $\overline{B}$	(A + $\overline{B}$) plus 1
1	0	0	0	$\overline{A}B$	A plus (A + B)	A plus (A + B) plus 1
1	0	0	1	$A \oplus B$	A plus B	A plus B plus 1
1	0	1	0	B	$A\overline{B}$ plus (A + B)	$A\overline{B}$ plus (A + B) plus 1
1	0	1	1	A + B	A + B	A + B plus 1
1	1	0	0	Logic 0	A plus A	A plus A plus 1
1	1	0	1	$A\overline{B}$	AB plus A	AB plus A plus 1
1	1	1	0	AB	$A\overline{B}$ plus A	$A\overline{B}$ plus A plus 1
1	1	1	1	A	A	A plus 1



Dimensions and pad layout for CD40181BH.

FUNCTION SELECT				INPUTS/OUTPUTS ACTIVE HIGH		
				LOGIC FUNCTION	ARITHMETIC* FUNCTION M = L	
S3	S2	S1	S0	M = H	C_n = H	C_n = L
0	0	0	0	$\overline{A}$	A	A plus 1
0	0	0	1	$\overline{A + B}$	A + B	(A + B) plus 1
0	0	1	0	$\overline{A}B$	A + $\overline{B}$	(A + $\overline{B}$) plus 1
0	0	1	1	Logic 0	minus 1	Zero
0	1	0	0	$\overline{AB}$	A plus $A\overline{B}$	A plus $A\overline{B}$ plus 1
0	1	0	1	$\overline{B}$	(A + B) plus $A\overline{B}$	(A + B) plus $A\overline{B}$ plus 1
0	1	1	0	$A \oplus B$	A minus B minus 1	A minus B
0	1	1	1	$A\overline{B}$	$A\overline{B}$ minus 1	$A\overline{B}$
1	0	0	0	$\overline{A}$ + B	A plus AB	A plus AB plus 1
1	0	0	1	$\overline{A \oplus B}$	A plus B	A plus B plus 1
1	0	1	0	B	(A + $\overline{B}$) plus AB	(A + $\overline{B}$) plus AB plus 1
1	0	1	1	AB	AB minus 1	AB
1	1	0	0	Logic 1	A plus A	A plus A plus 1
1	1	0	1	A + $\overline{B}$	(A + B) plus A	(A + B) plus A plus 1
1	1	1	0	A + B	(A + $\overline{B}$) plus A	(A + $\overline{B}$) plus A plus 1
1	1	1	1	A	A minus 1	A

* Expressed as two's complement. 1 = HIGH LEVEL 0 = LOW LEVEL

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

TABLE II
AC TEST SETUP REFERENCE (ACTIVE-LOW DATA)

TEST DELAY TIMES	AC PATHS		DC DATA INPUTS		MODE*
	INPUTS	OUTPUTS	TO V_{SS}	TO V_{DD}	
SUM_{IN} to SUM_{OUT}	$\overline{BO}$	Any $\overline{F}$	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$, M, C_n	All $\overline{A}$'s	ADD
SUM_{IN} to $\overline{P}$	$\overline{AO}$	$\overline{P}$	$\overline{A1}$, $\overline{A2}$, $\overline{A3}$, M, C_n	All $\overline{B}$'s	ADD
SUM_{IN} to $\overline{G}$	$\overline{BO}$	$\overline{G}$	All $\overline{A}$'s M, C_n	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$	ADD
SUM_{IN} to C_{n+4}	$\overline{BO}$	C_{n+4}	All $\overline{A}$'s, M, C_n	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$	ADD
C_n to SUM_{OUT}	C_n	Any $\overline{F}$	All $\overline{A}$'s, M	All $\overline{B}$'s	ADD
C_n to C_{n+4}	C_n	C_{n+4}	All $\overline{A}$'s, M	All $\overline{B}$'s	ADD
SUM_{IN} to A = B	$\overline{BO}$	A = B	All A's, B1, B2, B3, M	C_n	SUBTRACT
SUM_{IN} to SUM_{OUT} (Logic Mode)	All $\overline{B}$'s	Any $\overline{F}$	All $\overline{A}$'s, C_n	M	EXCLUSIVE OR

* ADD Mode: SO, S3 = V_{DD}; S1, S2 = V_{SS}. SUBTRACT Mode: SO, S3 = V_{SS}; S1, S2 = V_{DD}.

TABLE III
MAGNITUDE COMPARISON

ACTIVE – HIGH DATA				ACTIVE – LOW DATA		
INPUT C_n	OUTPUT C_{n+4}	MAGNITUDE		INPUT C_n	OUTPUT C_{n+4}	MAGNITUDE
1	1	$A \leq B$		0	0	$A \leq B$
0	1	$A < B$		1	0	$A < B$
1	0	$A > B$		0	1	$A > B$
0	0	$A \geq B$		1	1	$A \geq B$

1 = HIGH LEVEL
0 = LOW LEVEL

CD40182B Types

COS/MOS Look-Ahead Carry Generator

High-Voltage Types (20-Volt Rating)

The RCA-CD40182B is a high-speed look-ahead carry generator capable of anticipating a carry across four binary adders or groups of adders. The CD40182B is cascadable to perform full look-ahead across n-bit adders. Carry, propagate-carry, and generate-carry functions are provided as enumerated in the terminal designation below.

The CD40182B, when used in conjunction with the CD40181B arithmetic logic unit (ALU), provides full high-speed look-ahead carry capability for up to n-bit words. Each CD40182B generates the look-ahead (anticipated carry) across a group of four ALU's. In addition, other CD40182B's may be employed to anticipate the carry across sections of four look-ahead blocks up to n-bits. Carry inputs and outputs of the CD40181B are active-high logic, and carry-generate (G) and carry-propagate (P) outputs are active-low. Therefore the inputs and outputs of the CD40182B are compatible.

The CD40182B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

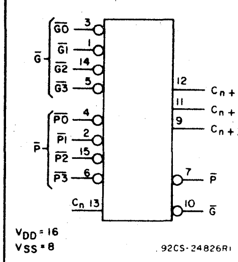
The CD40182B is similar to industry type MC14582.

Features:

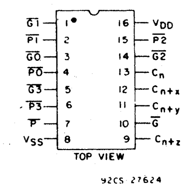
- **Generates high-speed carry across four adders or adder groups**
- **High-speed operations:** $t_{PHL} = t_{PLH} = 100$ **ns (typ.) @** $V_{DD} = 10$ **V**
- **Cascadable for fast carries over N bits**
- **Designed for use with CD40181B ALU**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) = 1 V at** $V_{DD} = 5$ **V, 2 V at** $V_{DD} = 10$ **V, 2.5 V at** $V_{DD} = 15$ **V**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:

- **High-speed parallel arithmetic units**
- **Multi-level look-ahead carry generation for long word lengths**



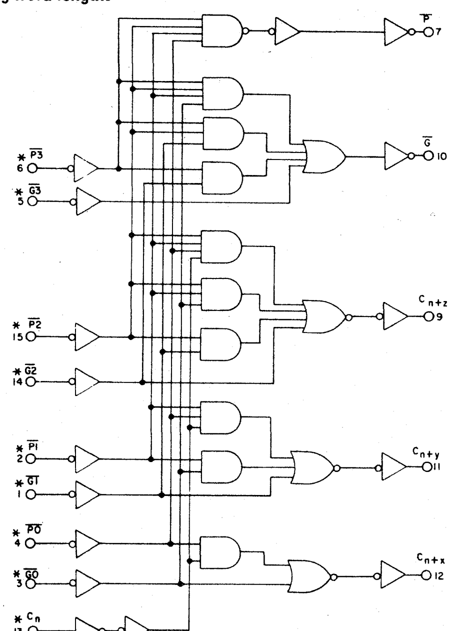
FUNCTIONAL DIAGRAM



TERMINAL ASSIGNMENT

TERMINAL DESIGNATIONS

DESIGNATION	TERM.	FUNCTION
$\overline{G0}, \overline{G1}, \overline{G2}, \overline{G3}$	3, 1, 14, 5	Active-Low Carry-Generate Inputs
$\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$	4, 2, 15, 6	Active-Low Carry-Propagate Inputs
C_n	13	Active-High Carry Input
$C_{n+x}, C_{n+y}, C_{n+z}$	12, 11, 9	Active-High Carry Outputs
$\overline{G}$	10	Active-Low Group Carry-Generate Output
$\overline{P}$	7	Active-Low Group Carry-Propagate Output



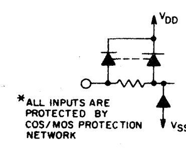


Fig. 1 – CD40182B logic diagram.

CD40182B Logic Equations:

$$C_{n+x} = G0 + P0 \cdot C_n$$

$$C_{n+y} = G1 + P1 \cdot G0 + P1 \cdot P0 \cdot C_n$$

$$C_{n+z} = G2 + P2 \cdot G1 + P2 \cdot P1 \cdot G0 + P2 \cdot P1 \cdot P0 \cdot C_n$$

$$\overline{G} = \overline{G3 + P3 \cdot G2 + P3 \cdot P2 \cdot G1 + P3 \cdot P2 \cdot P1 \cdot G0}$$

$$\overline{P} = \overline{P3 \cdot P2 \cdot P1 \cdot P0}$$

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . 0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . 0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D,F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . 55 to +125°C
PACKAGE TYPE E . . . . 40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . 65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,F,H Packages Values at –40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

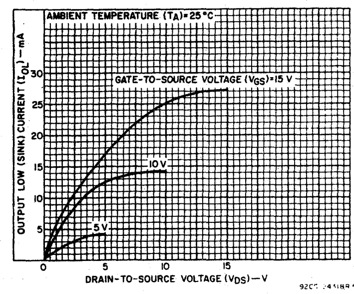


Fig. 2 – Typical output low (sink) current characteristics.

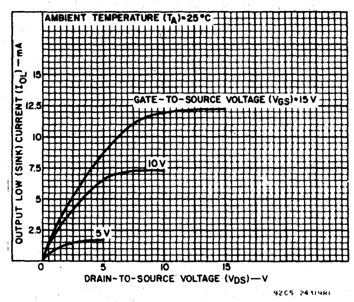


Fig. 3 – Minimum output low (sink) current characteristics.

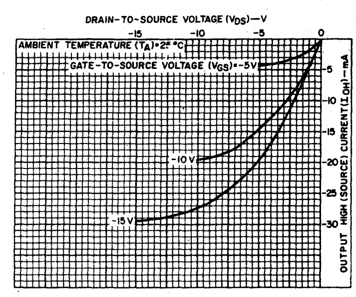


Fig. 4 – Typical output high (source) current characteristics.

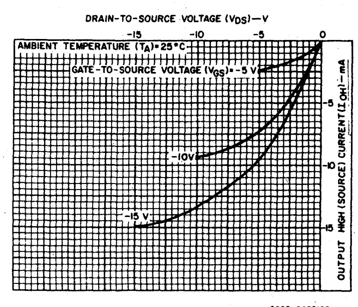


Fig. 5 – Minimum output high (source) current characteristics.

CD40182B Types

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$; Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} P, G In to P, G Out and Carry Outs	5	200	400	ns
	10	100	200	
	15	75	150	
C_n to Carry Outs	5	240	480	ns
	10	120	240	
	15	90	180	
Transition Time: t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance C_{IN} (Any Input)	–	5	7.5	pF

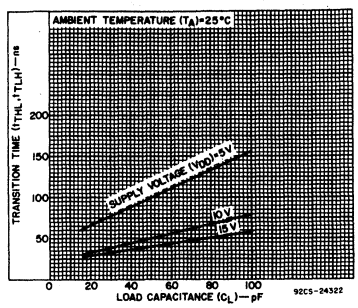


Fig. 6 – Typical transition time as a function of load capacitance.

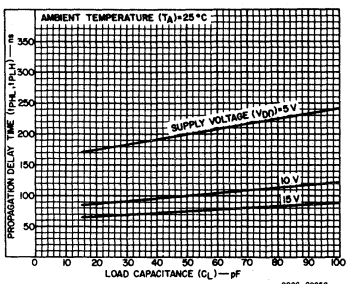


Fig. 7 – Typical propagation delay time as a function of load capacitance (P, G In to P, G Out and Carry-Outs).

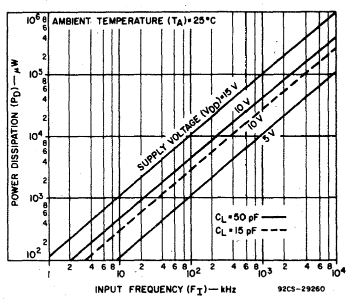


Fig. 8 – Typical power dissipation as a function of input frequency.

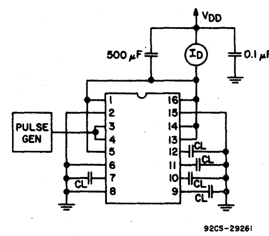


Fig. 9 – Power dissipation test circuit.

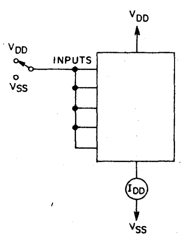


Fig. 10 – Quiescent device current test circuit.

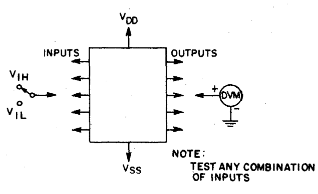


Fig. 11 – Input voltage test circuit.

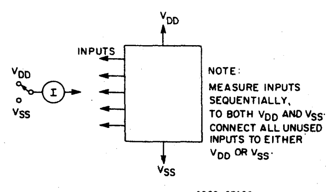


Fig. 12 – Input current test circuit.

Applications

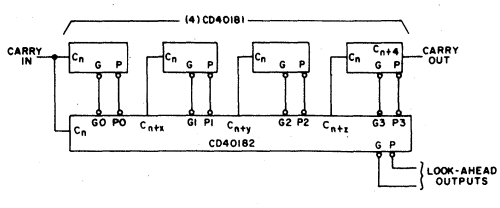


Fig. 13 – 16-Bit two-level look-ahead ALU.

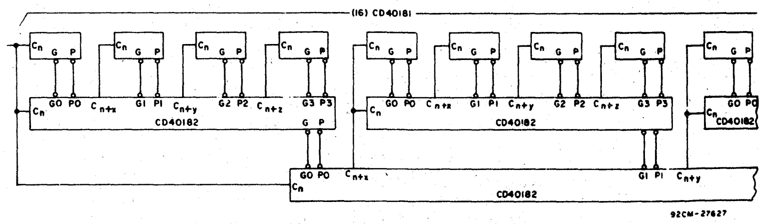


Fig. 14 – 64-Bit full carry look-ahead ALU in 3 levels.

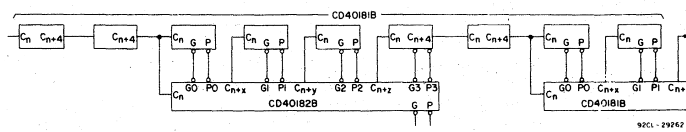
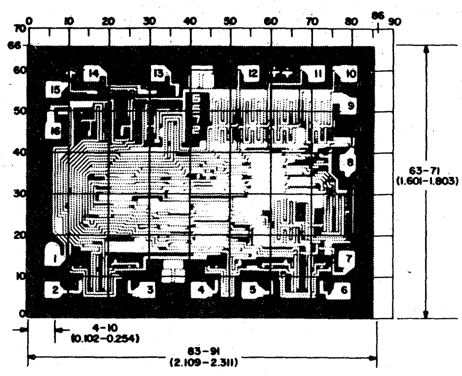


Fig. 15 – Combined two-level look-ahead and ripple-carry ALU.

DIMENSIONS AND PAD LAYOUT FOR CD40182BH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS Presettable Up/Down Counters (Dual Clock With Reset)

High-Voltage Types (20-Volt Rating)
CD40192 – BCD Type
CD40193 – Binary Type

The RCA-CD40192B Presettable BCD Up/Down Counter and the CD40193B Presettable Binary Up/Down Counter each consist of 4 synchronously clocked, gated "D" type flip-flops connected as a counter. The inputs consist of 4 individual jam lines, a $\overline{\text{PRESET ENABLE}}$ control, individual CLOCK UP and CLOCK DOWN signals and a master RESET. Four buffered Q signal outputs as well as $\overline{\text{CARRY}}$ and $\overline{\text{BORROW}}$ outputs for multiple-stage counting schemes are provided.

The counter is cleared so that all outputs are in a low state by a high on the RESET line. A RESET is accomplished asynchronously with the clock. Each output is individually programmable asynchronously with the clock to the level on the corresponding jam input when the $\overline{\text{PRESET ENABLE}}$ control is low.

The counter counts up one count on the positive clock edge of the CLOCK UP signal provided the CLOCK DOWN line is high. The counter counts down one count on the positive clock edge of the CLOCK DOWN signal provided the CLOCK UP line is high.

The $\overline{\text{CARRY}}$ and $\overline{\text{BORROW}}$ signals are high when the counter is counting up or down. The $\overline{\text{CARRY}}$ signal goes low one-half clock cycle after the counter reaches its maximum count in the count-up mode. The $\overline{\text{BORROW}}$ signal goes low one-half clock cycle after the counter reaches its minimum count in the count-down mode. Cascading of multiple packages is easily accomplished without the need for additional external circuitry by tying the $\overline{\text{BORROW}}$ and $\overline{\text{CARRY}}$ outputs to the CLOCK DOWN and CLOCK UP inputs, respectively, of the succeeding counter package.

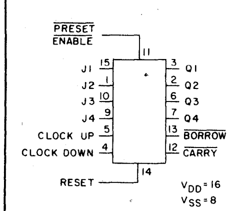
The CD40192B and CD40193B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Individual clock lines for counting up or counting down
- Synchronous high-speed carry and borrow propagation delays for cascading
- Asynchronous reset and preset capability
- Medium-speed operation—f_{CL} = 8 MHz (typ.) @ 10 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin over full package temperature range:
  1 V at V_{DD} = 5 V 2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

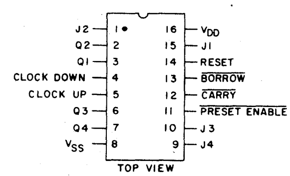
Applications:

- Up/down difference counting
- Multistage ripple counting
- Synchronous frequency dividers
- A/D and D/A conversion
- Programmable binary or BCD counting



CD40192B, CD40193B FUNCTIONAL DIAGRAM

92CS-27561RI



92CS-27564R2

CD40192B, CD40193B TERMINAL ASSIGNMENT

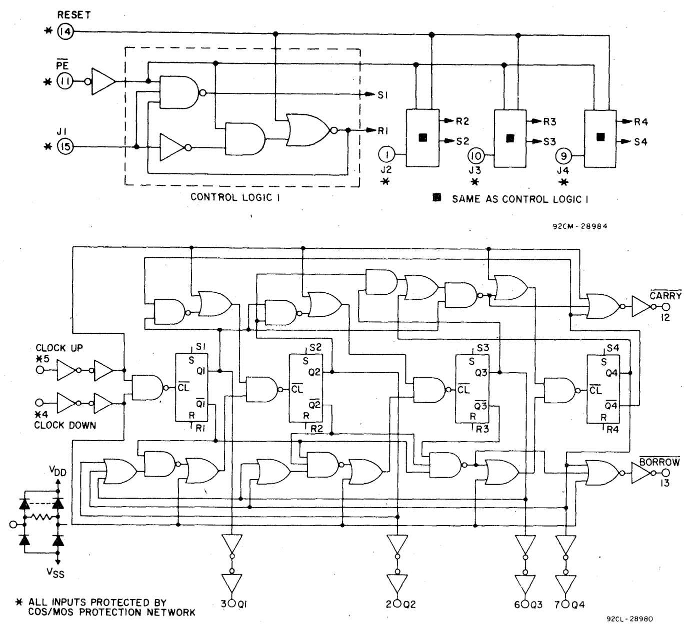


Fig. 1 – CD40192B logic diagram (BCD).

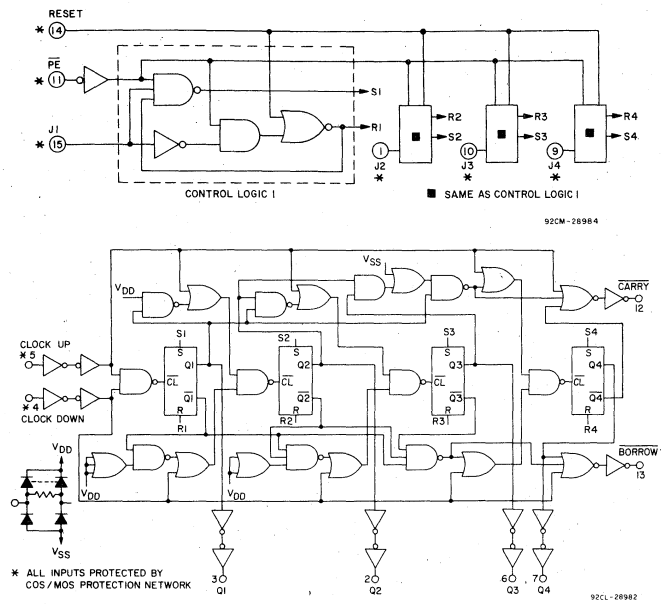


Fig. 2 — CD40193B logic diagram (binary).

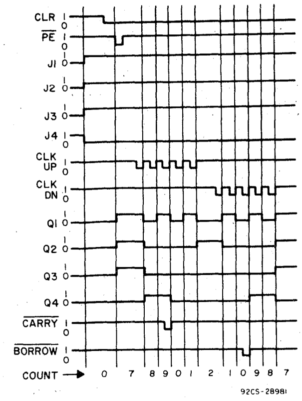


Fig. 3 — CD40192B timing diagram.

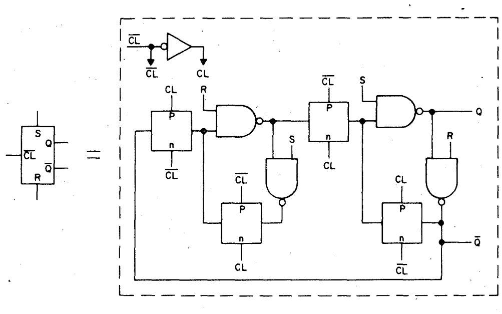


Fig. 4 — Internal logic of Flip-flop.

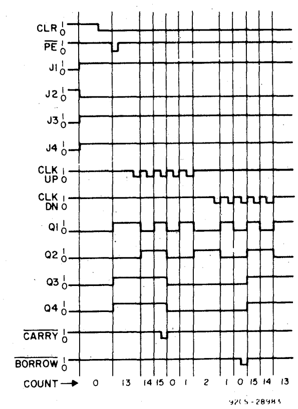


Fig. 5 — CD40193B timing diagram.

TRUTH TABLE

CLOCK UP	CLOCK DOWN	PRESET ENABLE (overbar)	RESET	ACTION
↑ (low-to-high)	1	1	0	COUNT UP
↓ (high-to-low)	1	1	0	NO COUNT
1	↑ (low-to-high)	1	0	COUNT DOWN
1	↓ (high-to-low)	1	0	NO COUNT
X	X	0	0	PRESET
X	X	X	1	RESET

1 = HIGH LEVEL   0 = LOW LEVEL   X = DON'T CARE

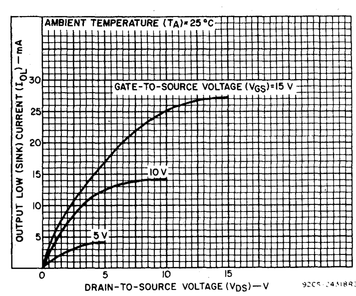


Fig. 6 — Typical output low (sink) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

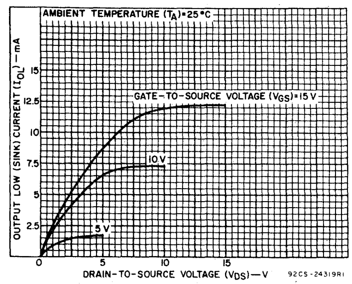


Fig. 7 — Minimum output low (sink) current characteristics.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C (unless otherwise specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply Voltage Range (For T_A = Full Temp. Range)	–	3	18	V
Removal Time: RESET or $\overline{PE}$	5	80	–	ns
	10	40	–	
	15	30	–	
Pulse Width: RESET	5	480	–	ns
	10	300	–	
	15	260	–	
$\overline{PE}$	5	240	–	ns
	10	170	–	
	15	140	–	
CLOCK	5	180	–	ns
	10	90	–	
	15	60	–	
Clock Input Frequency	5	DC	2	MHz
	10		4	
	15		5.5	
Clock Rise & Fall Time	5	–	15	μs
	10	–	15	
	15	–	5	

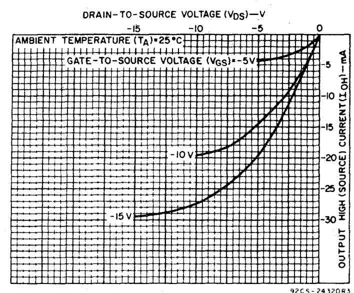


Fig. 8 — Typical output high (source) current characteristics.

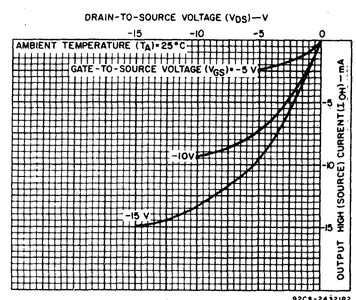


Fig. 9 — Minimum output high (source) current characteristics.

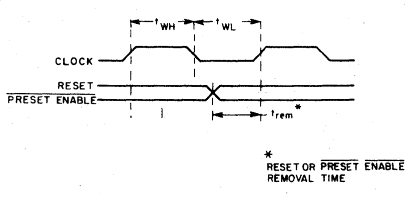


Fig. 10 — Timing diagram defining t_{rem}.

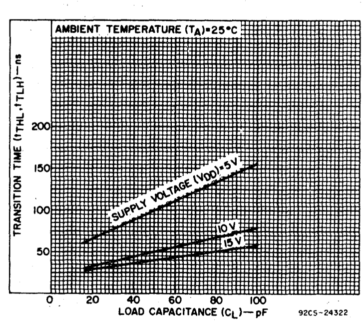


Fig. 11 — Typical transition time as a function of load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D, F, H Packages Values at –40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

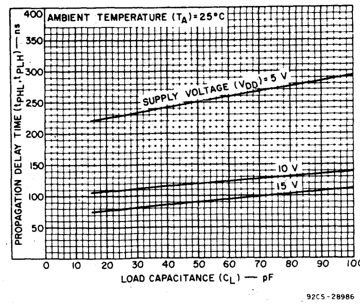


Fig. 12 – Typical propagation delay time as a function of load capacitance.

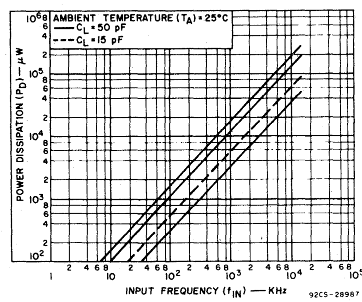
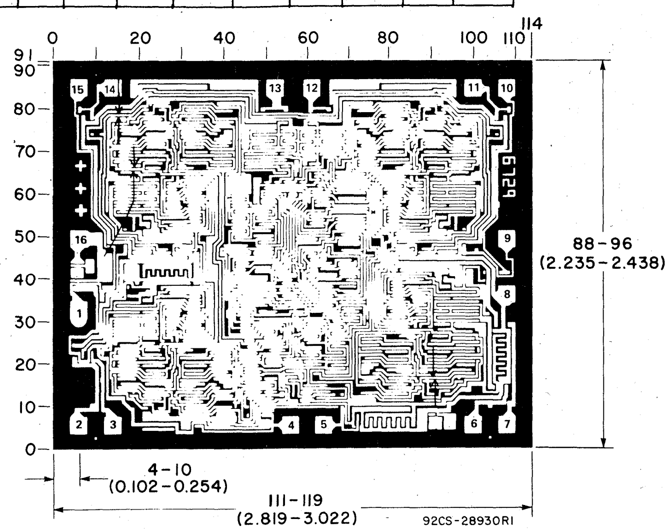


Fig. 13 – Dynamic power dissipation.



Dimensions and pad layout for the CD40192BH (dimensions and pad layout for the CD40193BH are identical).

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C
Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time t_{PHL}, t_{PLH}: CLOCK UP or CLOCK DOWN to Q, RESET to Q	5	–	250	500	ns
	10	–	120	240	
	15	–	90	180	
$\overline{PE}$ to Q	5	–	200	400	ns
	10	–	100	200	
	15	–	70	140	
CLOCK UP to $\overline{CARRY}$, CLOCK DOWN to $\overline{BORROW}$	5	–	160	320	ns
	10	–	80	160	
	15	–	60	120	
$\overline{RESET}$ or $\overline{PE}$ to $\overline{BORROW}$ or $\overline{CARRY}$	5	–	300	600	ns
	10	–	150	300	
	15	–	110	220	
Transition Time, t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Min. Removal Time, t_{rem}* RESET or $\overline{PE}$	5	–	40	80	ns
	10	–	20	40	
	15	–	15	30	
Min. Pulse Width, t_W RESET	5	–	240	480	ns
	10	–	150	300	
	15	–	130	260	
$\overline{PE}$	5	–	120	240	ns
	10	–	85	170	
	15	–	70	140	
CLOCK	5	–	90	180	ns
	10	–	45	90	
	15	–	30	60	
Max. Clock Input Frequency, f_{CL}	5	2	4	–	MHz
	10	4	8	–	
	15	5.5	11	–	
Clock Rise & Fall Time, t_r, t_f	5	–	–	15	μs
	10	–	–	15	
	15	–	–	5	
Input Capacitance, C_{IN}: RESET	–	–	10	15	pF
All Other Inputs	–	–	5	7.5	pF

*The time required for RESET or PRESET ENABLE control to be removed before clocking (see timing diagram, Fig. 10.

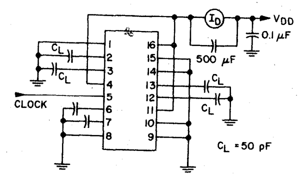


Fig. 14 – Dynamic power dissipation test circuit.

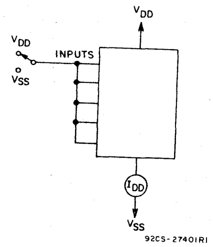


Fig. 15 – Quiescent-device-current test circuit.

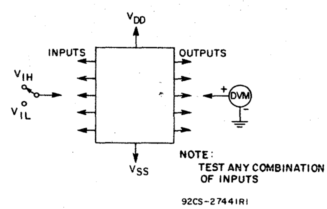


Fig. 16 – Input-voltage test circuit.

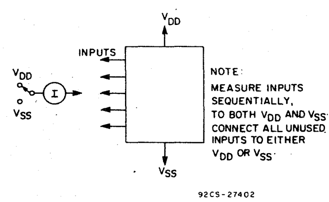


Fig. 17 – Input current test circuit.

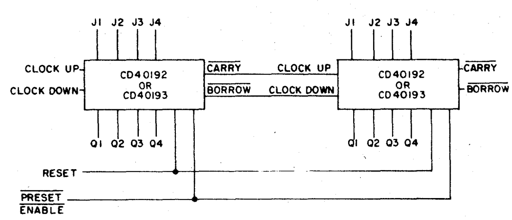


Fig. 18 – Cascaded counter packages.

COS/MOS 4 x 4 Multiport Register

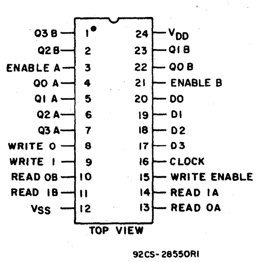
High-Voltage Types (20-Volt Rating)

The RCA-CD40208B is a 4 x 4 multiport register containing four 4-bit registers, write address decoder, two separate read address decoders, and two 3-state output buses.

When the ENABLE input is low, the corresponding output bus is switched, independently of the clock, to a high-impedance state. The high-impedance third state provides the outputs with the capability of being connected to the bus lines in a bus-organized system without the need for interface or pull-up components.

When the WRITE ENABLE input is high, all data input lines are latched on the positive transition of the CLOCK and the data is entered into the word selected by the write address lines. When WRITE ENABLE is low, the CLOCK is inhibited and no new data is entered. In either case, the contents of any word may be accessed via the read address lines independent of the state of the CLOCK input.

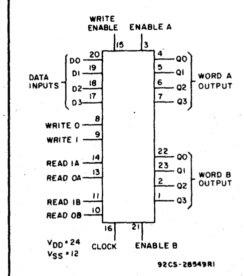
The CD40208B types are supplied in hermetic 24-lead dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).



TERMINAL ASSIGNMENT

Features:
- **Four 4-bit registers**
- **One input and two output buses**
- **Unlimited expansion in bit and word directions**
- **Data lines have latched inputs**
- **3-state outputs**
- **Separate control of each bus, allowing simultaneous independent reading of any of four registers on Bus A and Bus B and independent writing into any of the four registers**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package-temperature range):**
  - **1 V at V_{DD} = 5 V**
  - **2 V at V_{DD} = 10 V**
  - **2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications:
- **Scratch-pad memories**
- **Arithmetic units**
- **Data storage**



FUNCTIONAL DIAGRAM

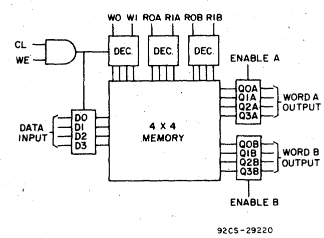


Fig. 1 – Block diagram.

TRUTH TABLE

CLOCK	WRITE ENABLE	WRITE 1	WRITE 0	READ 1A	READ 0A	READ 1B	READ 0B	ENABLE A	ENABLE B	D_n	Q_{nA}	Q_{nB}
↑	1	S1	S2	S1	S2	S1	S2	1	1	1	1	1
↑	1	S1	S2	S1	S2	S1	S2	1	1	0	0	0
X	X	X	X	X	X	X	X	0	0	X	Z	Z
↑	1	0	0	0	1	1	0	1	1	D_n to word 0	Word 1 out	Word 2 out
↑	0	0	0	0	1	1	0	1	1	Word 0 not altered	Word 1 out	Word 2 out
X	X	X	X	1	0	0	1	1	1	X	Word 2 out	Word 1 out
↓	X	X	X	X	X	X	X	1	1	X	NC	NC

1 = HIGH LEVEL; 0 = LOW LEVEL, X = DON'T CARE, Z = HIGH IMPEDANCE
S1 and S2 refer to input states of either 1 or 0

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

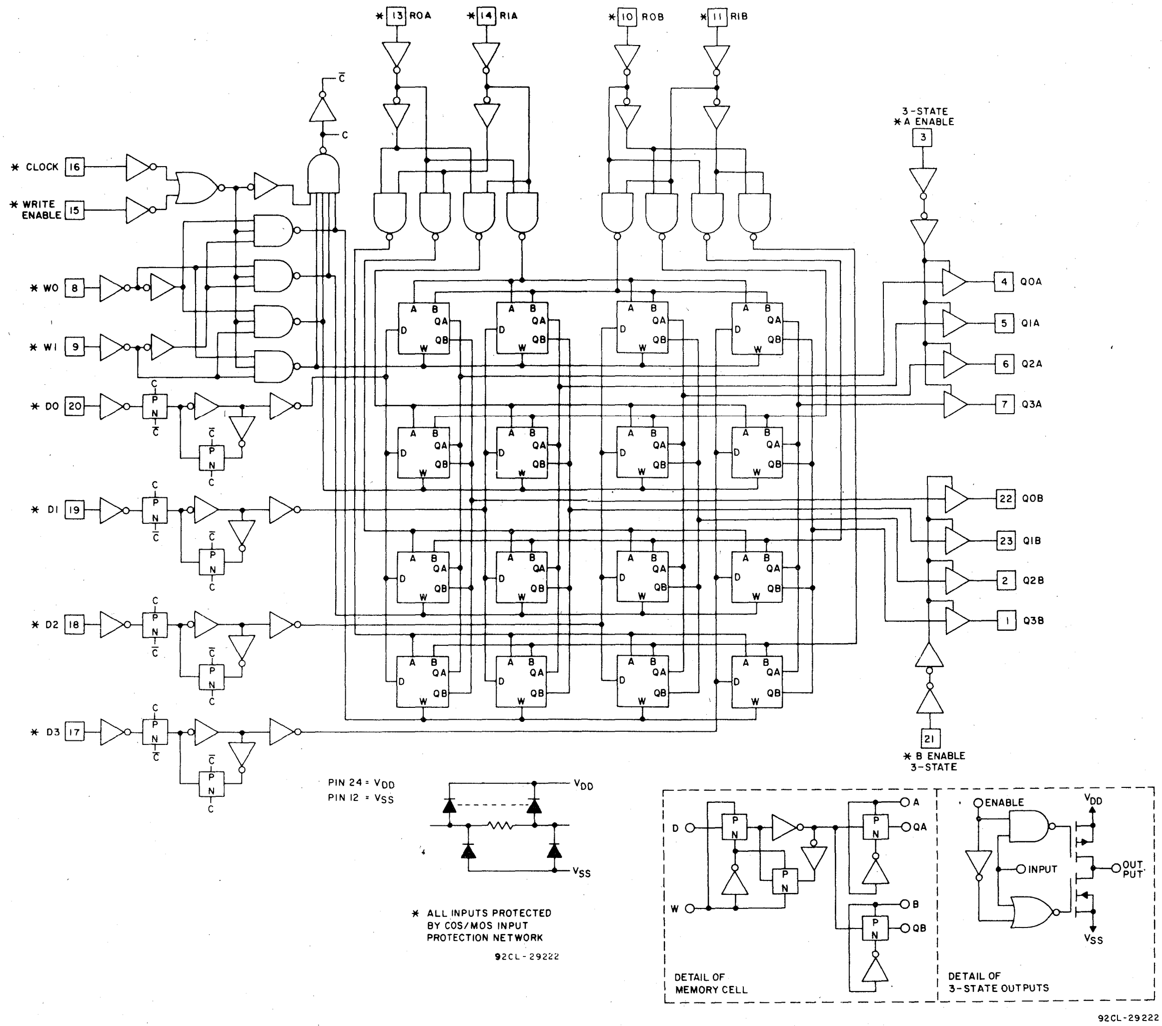


Fig. 2 — Logic diagram.

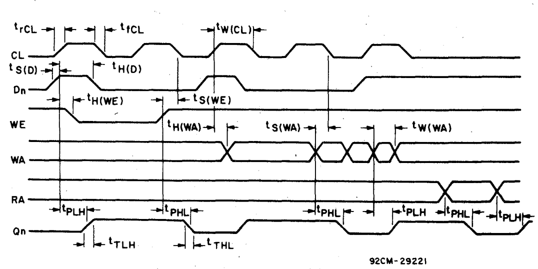


Fig. 3 — Timing diagram.

RECOMMENDED OPERATING CONDITIONS *at $T_A = 25^oC$, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:*

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply Voltage Range (For T_A = Full Package Temperature Range)	–	3	18	V
Set-Up Time: Data to Clock, $t_{S(D)}$	5	0	–	ns
	10	0	–	
	15	0	–	
Write Enable to $\overline{Clock}$, $t_{S(WE)}$	5	250	–	ns
	10	100	–	
	15	70	–	
Write Address to $\overline{Clock}$, $t_{S(WA)}$	5	250	–	ns
	10	100	–	
	15	70	–	
Hold Time: Data to Clock, $t_{H(D)}$	5	220	–	ns
	10	100	–	
	15	80	–	
Write Enable to Clock, $t_{H(WE)}$	5	270	–	ns
	10	130	–	
	15	80	–	
Write Address to Clock, $t_{H(WA)}$	5	330	–	ns
	10	140	–	
	15	90	–	
Clock Input Frequency, f_{CL}	5	–	1.5	MHz
	10	–	3.5	
	15	–	4.5	
Clock Pulse Width, CL or WE t_W	5	350	–	ns
	10	130	–	
	15	90	–	
Clock Rise or Fall Time, t_rCL or t_fCL	5	–	15	µs
	10	–	5	
	15	–	5	

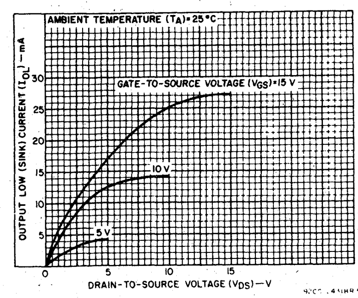


Fig. 4 – Typical output low (sink) current characteristics.

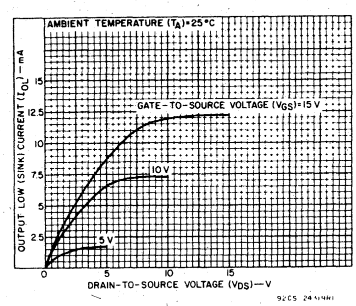


Fig. 5 – Minimum output low (sink) current characteristics.

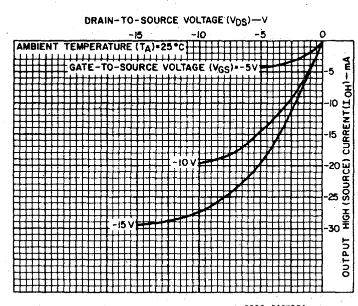


Fig. 6 – Typical output high (source) current characteristics.

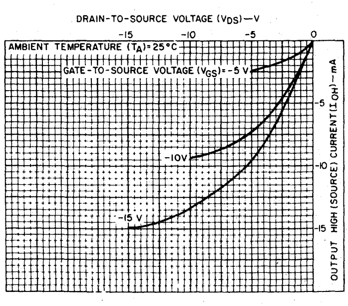


Fig. 7 – Minimum output high (source) current characteristics.

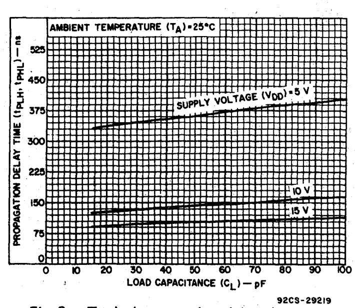


Fig. 8 – Typical propagation delay time as a function of load capacitance (CL or WE to Q).

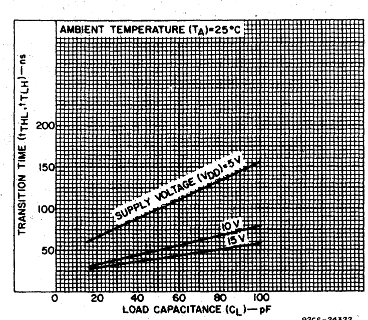


Fig. 9 – Typical transition time as a function of load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55, +25, +125 Apply to D,K,F,H Packages Values at –40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	µA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	15, 13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	µA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	µA

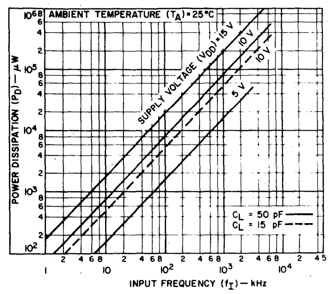


Fig. 10 — Typical power dissipation as a function of input frequency.

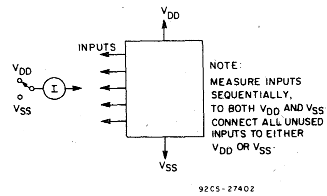


Fig. 11 — Input leakage current test circuit.

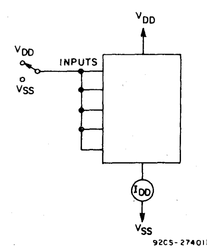
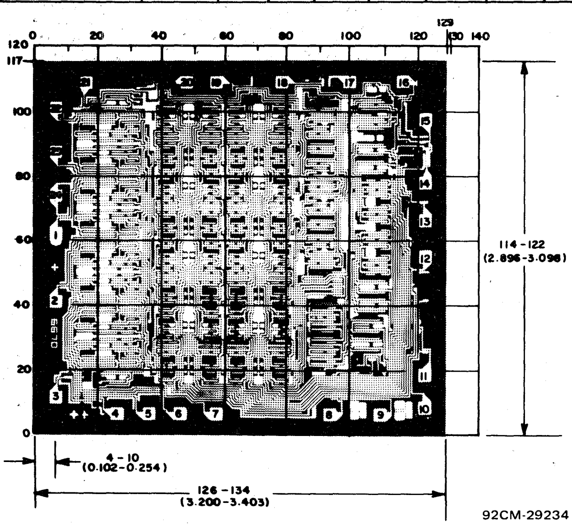


Fig. 12 — Quiescent-device-current test circuit.



Dimensions and Pad Layout for CD40208BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} Clock or Write Enable to Q	5	–	360	720	ns
	10	–	140	280	
	15	–	100	200	
Read or Write Address to Q	5	–	300	600	ns
	10	–	120	240	
	15	–	85	170	
3-State Disable Delay Time: t_{PZH}, t_{PHZ}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
t_{PZL}, t_{PLZ}	5	–	130	260	ns
	10	–	60	120	
	15	–	50	100	
Output Transition Time: t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Minimum Setup Time: Data to Clock $t_{S(D)}$	5	–	–95	0	ns
	10	–	–35	0	
	15	–	–20	0	
Write Enable to $\overline{Clock}$ $t_{S(WE)}$	5	–	125	250	ns
	10	–	50	100	
	15	–	35	70	
Write Address to $\overline{Clock}$ $t_{S(WA)}$	5	–	125	250	ns
	10	–	50	100	
	15	–	35	70	
Clock Rise and Fall Time: t_rCL, t_fCL	5	–	–	15	μs
	10	–	–	5	
	15	–	–	5	
Minimum Hold Time: Data to Clock $t_{H(D)}$	5	–	110	220	ns
	10	–	50	100	
	15	–	40	80	
Write Enable to Clock $t_{H(WE)}$	5	–	135	270	ns
	10	–	65	130	
	15	–	40	80	
Write Address to $\overline{Clock}$ $t_{H(WA)}$	5	–	165	330	ns
	10	–	70	140	
	15	–	45	90	
Maximum Clock Input Frequency, f_{CL}	5	1.5	3	–	MHz
	10	3.5	7	–	
	15	4.5	9	–	
Minimum Clock Pulse Width, Clock or Write Enable $t_{W(CL)}$	5	–	175	350	ns
	10	–	65	130	
	15	–	45	90	
Write Address $t_{W(WA)}$	5	–	150	300	ns
	10	–	75	150	
	15	–	45	90	
Average Input Capacitance, (Any Input) C_I	–	–	5	7.5	pF

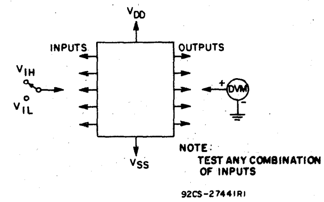


Fig. 13 – Input-voltage test circuit.

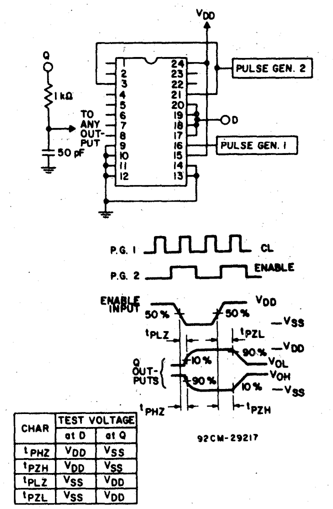


Fig. 14 – Output-enable-delay-times test circuit and waveforms.

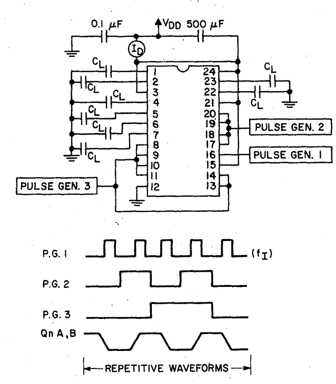


Fig. 15 – Power-dissipation test circuit and waveforms.

CD40257B Types

COS/MOS Quad 2-Line-to-1-Line Data Selector/Multi plexer

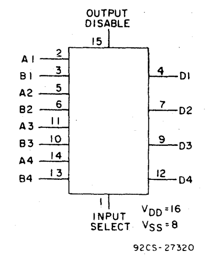
High-Voltage Types (20-Volt Rating)

The RCA-CD40257B is a Data Selector/Multiplexer featuring three-state outputs which can interface directly with and drive data lines of bus-oriented systems.

The CD40257B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **3-state outputs**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package-temperature range):**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM

Applications:

- **Digital Multiplexing**
- **Shift-right/shift-left registers**
- **True/complement selection**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . 0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . 0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A 40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A 55 to +100°C (PACKAGE TYPES D,F) . . . . . 500 mW
For T_A +100 to +125°C (PACKAGE TYPES D, F) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A)
PACKAGE TYPES D, F, H . . . . . 55 to +125°C
PACKAGE TYPE E . . . . . -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . 65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

TRUTH TABLE

INPUTS				OUTPUT
3-STATE OUTPUT DISABLE	SELECT	A	B	D
1	X	X	X	Z
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1

X = DON'T CARE LOGIC 1 = HIGH
LOGIC 0 = LOW Z = HIGH IMPEDANCE

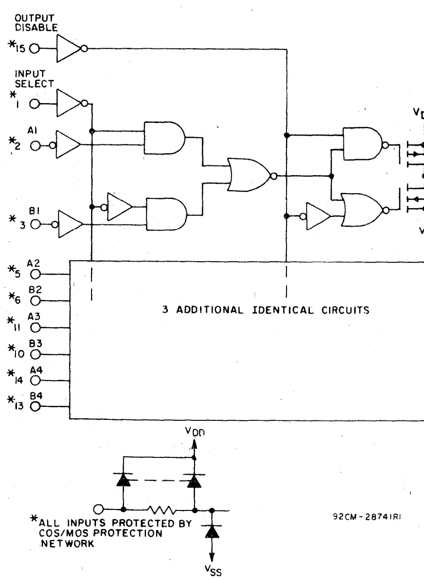


Fig. 1 – Logic diagram for CD40257B.

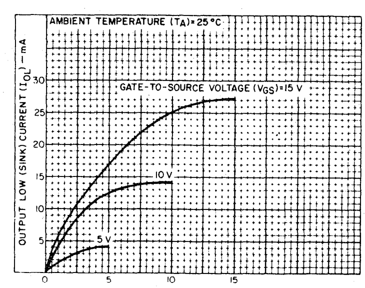


Fig. 2 – Typical output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at –55,+25,+125 Apply to D, F,H Pkgs. Values at –40,+25,+85 Apply to E Pkgs.							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	μA
	–	0,15	15	4	4	120	120	–	0.02	4	μA
	–	0,20	20	20	20	600	600	–	0.04	20	μA
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	mA
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	mA
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	mA
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	mA
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	mA
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	mA
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	V
	–	0,15	15	0.05				–	0	0.05	V
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	V
	–	0,10	10	9.95				9.95	10	–	V
	–	0,15	15	14.95				14.95	15	–	V
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	V
	1.5,13.5	–	15	4				–	–	4	V
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	V
	1,9	–	10	7				7	–	–	V
	1.5,13.5	–	15	11				11	–	–	V
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.		0,18	18	±0.4	±0.4	±12	±12	–	$\pm10^{-4}$	±0.4	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
		V_{DD}(V)	Typ.	Max.	
Propagation Delay Time: Data Input to Output, t_{PHL}, t_{PLH}		5	150	300	ns
		10	70	140	ns
		15	50	100	ns
Select to Output, t_{PHL}, t_{PLH}		5	190	380	ns
		10	85	170	ns
		15	65	130	ns
Output Disable to Output, t_{PHL}, t_{PLH}		5	95	190	ns
		10	50	100	ns
		15	40	80	ns
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	ns
		15	40	80	ns
Input Capacitance, C_{IN}	Any Input	–	5	7.5	pF

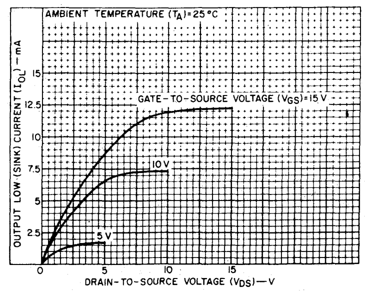


Fig.3 – Minimum output low (sink) current characteristics.

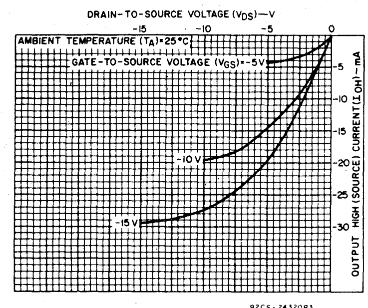


Fig.4 – Typical output high (source) current characteristics.

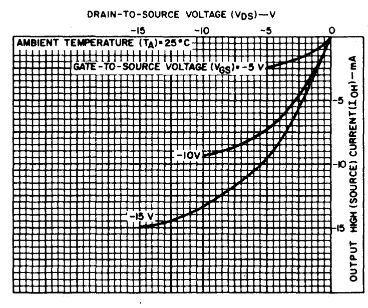


Fig.5 – Minimum output high (source) current characteristics.

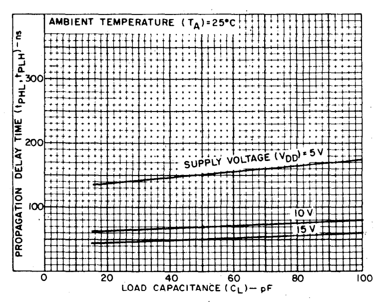


Fig.6 – Typical propagation delay time as a function of load capacitance (DATA INPUT to OUTPUT).

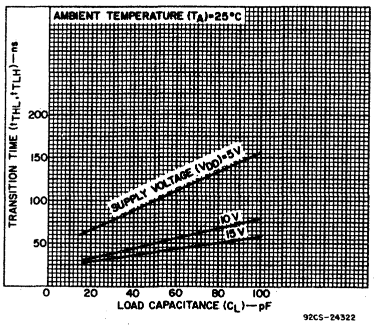


Fig.7 – Typical transition time as a function of load capacitance.

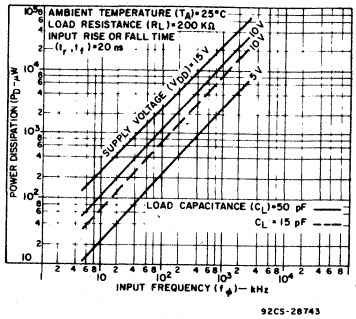


Fig.8 – Typical dynamic power dissipation as a function of input frequency (one INPUT to one OUTPUT).

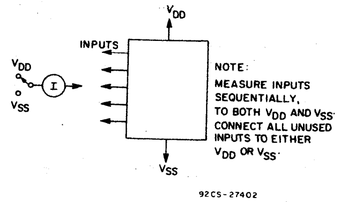


Fig.9 – Input current test circuit.

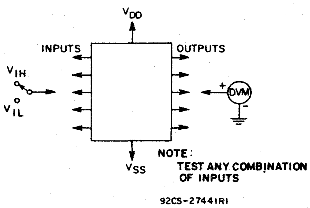


Fig.10 – Input voltage test circuit.

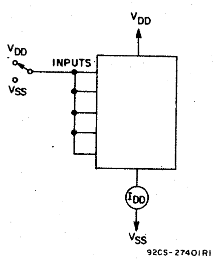
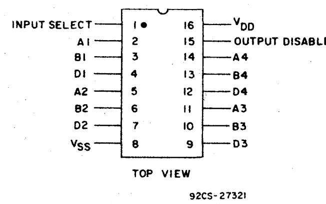
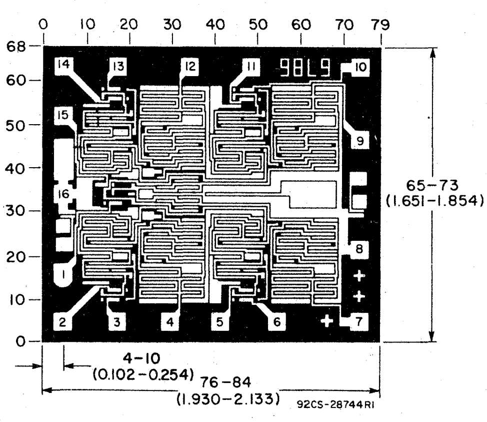


Fig.11 – Quiescent device current test circuit.



TERMINAL ASSIGNMENT

Dimensions and pad layout for CD40257BH.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS A-Series Integrated Circuits

Technical Data

CD4000A, CD4001A, CD4002A, CD4025A Types

COS/MOS NOR Gates

Dual 3 Input plus Inverter—CD4000A
Quad 2 Input—CD4001A
Dual 4 Input—CD4002A
Triple 3 Input—CD4025A

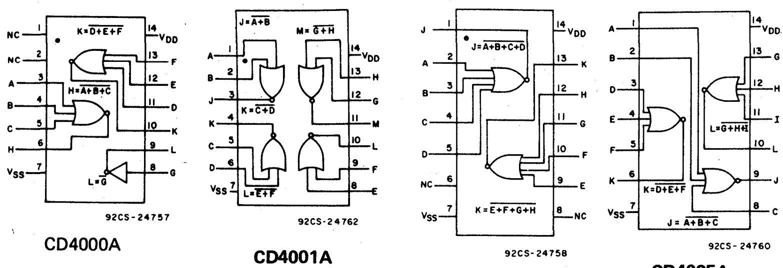
The RCA-CD4000A, CD4001A, CD4002A, and CD4025A NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of COS/MOS gates.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

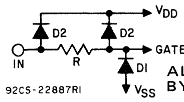
Features:

- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

FUNCTIONAL DIAGRAMS



CD4000A CD4001A CD4002A CD4025A



ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . -65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . -55 to +125°C
PACKAGE TYPE E . . . . -40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . -0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = -40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = -55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . -0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	12	V

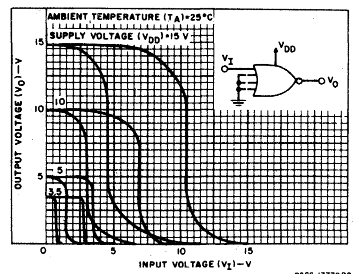


Fig. 1 — Minimum & maximum voltage transfer characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C, C_L = 15 pF, Input t_r, t_f = 20 ns*

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (Volts)	D, F, H PACKAGES TYP.	D, F, H PACKAGES MAX.	E PACKAGE TYP.	E PACKAGE MAX.	UNITS
Propagation Delay Time: High-to-Low Level, t_{PHL}		5	35/60	50/95	35/60	80/95	ns
		10	25/35	40/60	25/35	55/60	
Low-to-High Level, t_{PLH}		5	35/80	95/120	35/80	120/120	ns
		10	25/40	45/65	25/40	65/65	
Transition Time: High-to-Low Level, t_{THL}		5	65	125	65	200	ns
		10	35	70	35	115	
Low-to-High Level, t_{TLH}		5	65	175	65	300	ns
		10	35	75	35	125	
Input Capacitance, C_I	Any Input		5	–	5	–	pF

Note: Numbers to the right of slash mark are for CD4025A; numbers to the left of slash mark are for 4000A, 4001A, and 4002A.

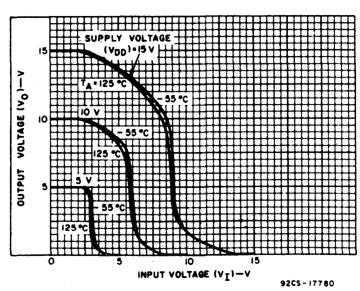
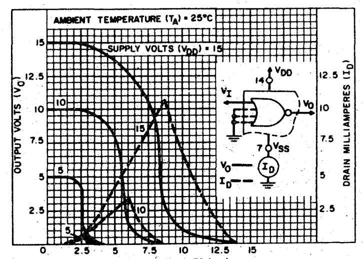


Fig. 2 — Typical voltage transfer characteristics as a function of temperature.

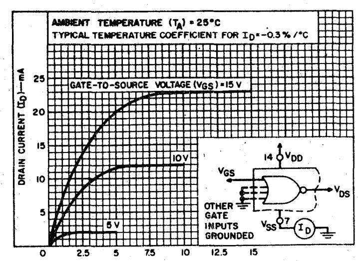
STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, F, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	0.05	0.001	0.05	3	0.5	0.005	0.5	15	μA
	–	–	10	0.1	0.001	0.1	6	5	0.005	5	30	
	–	–	15	2	0.02	2	40	50	0.5	50	500	
Output Voltage: Low Level, V_{OL}	–	0, 5	5	0 Typ.; 0.05 Max								V
	–	0, 10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0, 5	5	4.95 Min.; 5 Typ.								
	–	0, 10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	1	0.4	0.28	0.35	1	0.3	0.24	mA
	0.5	–	10	1.1	2.5	0.9	0.65	0.72	2.5	0.6	0.48	
P-Channel (Source): I_DP Min.	2.5	–	5	-0.62	-2	-0.5	-0.35	-0.35	-2	-0.3	-0.24	
	9.5	–	10	-0.62	-1	-0.5	-0.35	-0.3	-1	-0.25	-0.2	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ., ±1 Max.								μA



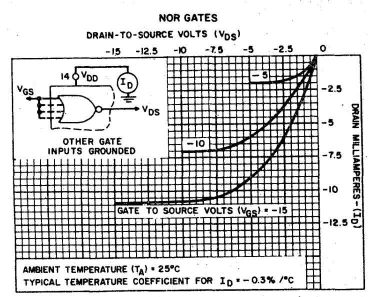
92CS-17778

Fig. 3 — Typical current & voltage transfer characteristics.



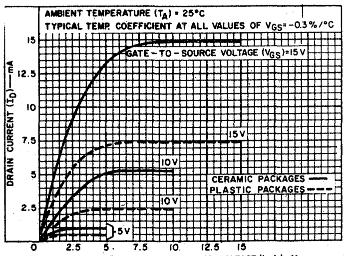
92CS-17777

Fig. 4 — Typical n-channel drain characteristics.



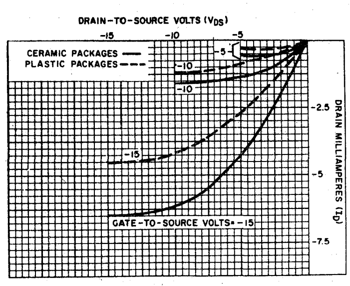
92CS-17776

Fig. 5 — Typical p-channel drain characteristics.



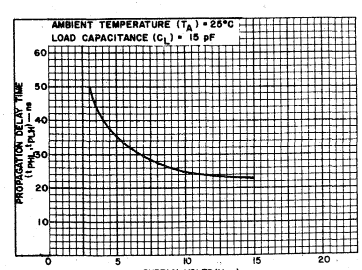
92CS-17853

Fig. 6 — Minimum n-channel drain characteristics.



92CS-17844

Fig. 7 — Minimum p-channel drain characteristics.



92CS-19866

Fig. 8 — Typical propagation delay time vs. V_{DD}.

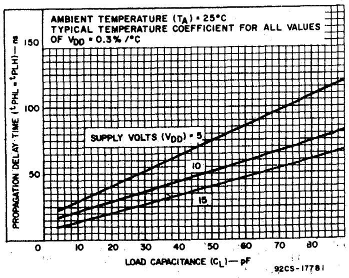


Fig. 9 — Typical propagation delay time vs. C_L.

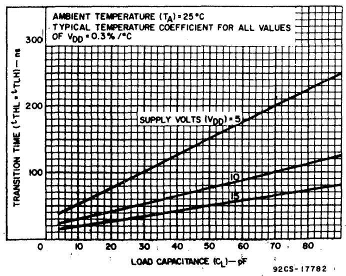


Fig. 10 — Typical transition time vs. C_L.

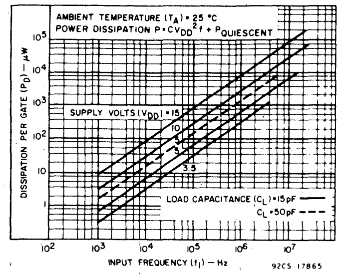


Fig. 11 — Typical dissipation characteristics.

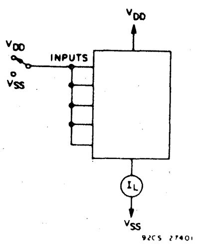
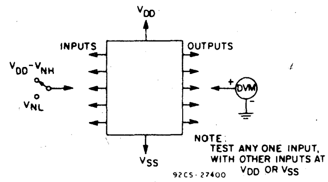


Fig. 12 — Quiescent device current test circuit.



NOTE:

CD4000, CD4002, CD4025-
TEST ANY ONE INPUT WITH OTHER INPUTS AT V_{DD} OR V_{SS}.

CD4001 - TEST ANY COMBINATION OF INPUTS.

Fig. 13 — Noise immunity test circuit.

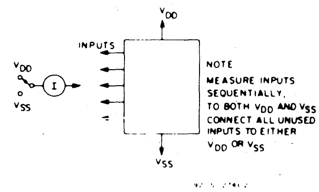


Fig. 14 — Input leakage current test circuit.

COS/MOS 18-Stage Static Shift Register

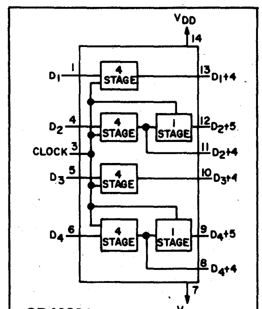
The RCA-CD4006A types are comprised of 4 separate shift register sections: two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent single-rail data path.

A common clock signal is used for all stages. Data are shifted to the next stage on negative-going transitions of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17 and 18 stages can be implemented using one CD4006A package. Longer shift register sections can be assembled by using more than one CD4006A.

Features:

- **Fully static operation**
- **Shifting rates up to 5 MHz**
- **Permanent register storage with clock line high or low — — no information recirculation required**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4006A FUNCTIONAL DIAGRAM

Applications:

- **Serial shift registers**
- **Time delay circuits**
- **Frequency division**

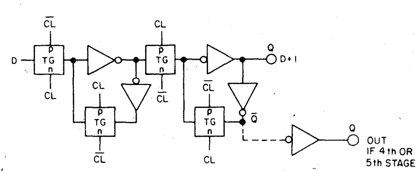
MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	VDD (V)	LIMITS				UNITS
		D,F,H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5 10	80 40	– –	100 50	– –	ns
Clock Pulse Width, t_W	5 10	500 200	– –	830 250	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 2.5	dc dc	0.6 2	MHz
Clock Rise and Fall Time, t_rCL, t_fCL*	5 10	– –	15 5	– –	15 5	μs

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.



TRUTH TABLE FOR SHIFT REGISTER STAGE

D	CL▲	D+1
0	⌐\	0
1	⌐\	1
X	⌐/	NC

1 = HIGH
0 = LOW
NC = NO CHANGE
X = DON'T CARE
▲ = LEVEL CHANGE

92CS-17887R1

Fig. 1 — Logic diagram and truth table (one register stage).

CD4006A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions V_O (V)	V_{IN} (V)	V_{DD} (V)	Limits at Indicated Temperatures (°C) D, F, H Packages −55	+25 Typ.	+25 Limit	+125	E Package −40	+25 Typ.	+25 Limit	+85	Units
Quiescent Device Current, I_L Max.	–	–	5	0.5	0.01	0.5	30	5	0.03	5	70	μA
	–	–	10	1	0.01	1	60	10	0.05	10	140	
	–	–	15	25	0.5	25	1000	250	2.5	250	2500	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink), I_DN Min.	0.5	–	5	0.155	0.25	0.125	0.085	0.072	0.25	0.06	0.048	mA
	0.5	–	10	0.31	0.5	0.25	0.175	0.15	0.5	0.125	0.1	
p-Channel (Source): I_DP Min.	4.5	–	5	-0.125	-0.15	-0.1	-0.07	-0.06	-0.15	-0.05	-0.04	
	9.5	–	10	-0.25	-0.3	-0.2	-0.14	-0.12	-0.3	-0.1	-0.08	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

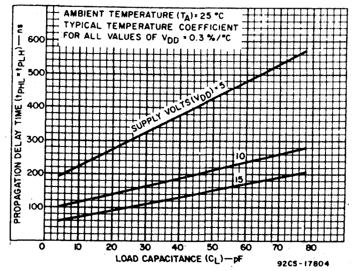


Fig. 2 – Typical propagation delay time vs. load capacitance.

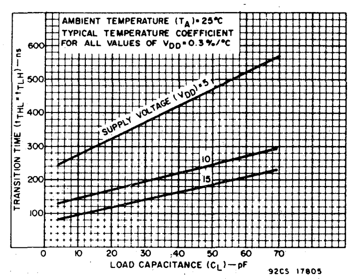


Fig. 3 – Typical transition time vs. load capacitance.

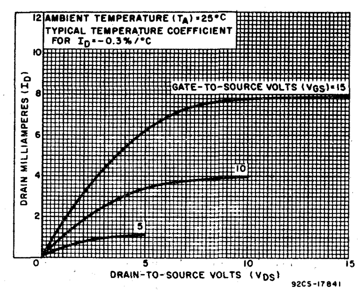
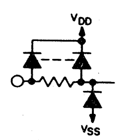


Fig. 5 – Typical output n-channel drain characteristics.



* ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK.

NOTE: ALL "P"-UNIT SUBSTRATES ARE CONNECTED TO V_{DD}
ALL "N"-UNIT SUBSTRATES ARE CONNECTED TO V_{SS}

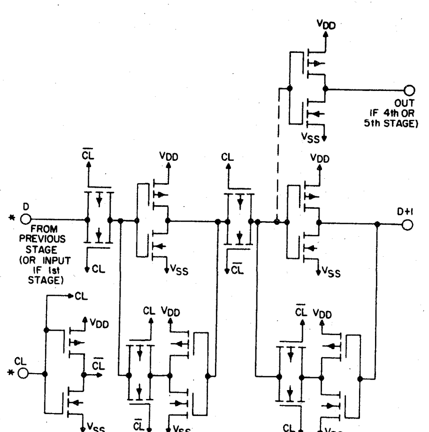


Fig. 4 – Schematic diagram (one register stage).

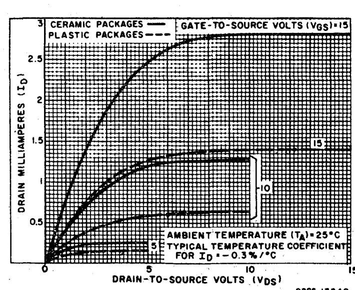


Fig. 6 – Minimum output n-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D,F,H Packages			E Package			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time; t_{PLH}, t_{PHL}		5	–	250	400	–	250	500	ns
		10	–	125	200	–	125	250	
Transition Time; t_{THL}, t_{TLH}		5	–	250	400	–	250	500	ns
		10	–	125	200	–	125	250	
Maximum Clock Input Frequency, f_{CL}		5	1	2.5	–	0.6	2.5	–	MHz
		10	2.5	5	–	2	5	–	
Minimum Clock Pulse Width, t_W		5	–	200	500	–	200	830	ns
		10	–	100	200	–	100	250	
Clock Rise & Fall Time; t_rCL, t_fCL*		5	–	–	15	–	–	15	μs
		10	–	–	5	–	–	5	
Minimum Data Set Up Time, t_S		5	–	50	80	–	50	100	ns
		10	–	25	40	–	25	50	
Average Input Capacitance, C_I	Data Input		–	5	–	–	5	–	pF
	Clock Input		–	30	–	–	30	–	pF

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

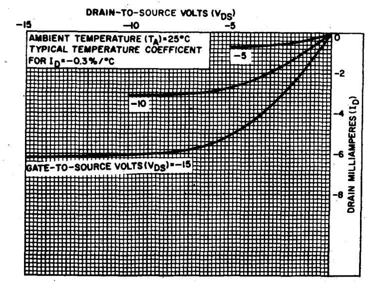


Fig. 7 — Typical output p-channel drain characteristics.

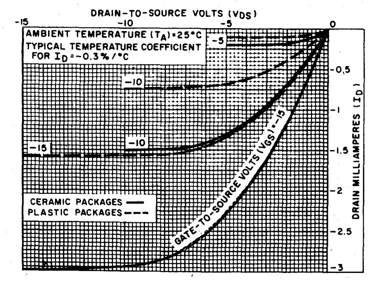


Fig. 8 — Minimum output p-channel drain characteristics.

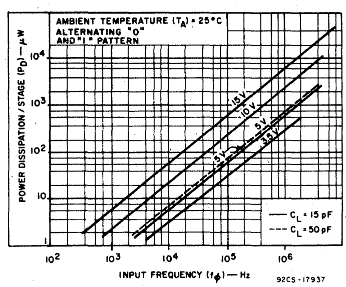


Fig. 9 — Typical dissipation characteristics.

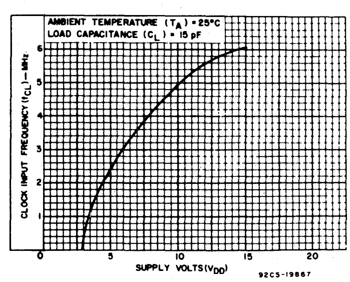


Fig. 10 — Typical clock input frequency vs. supply voltage.

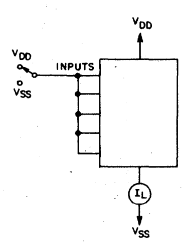


Fig. 11 — Quiescent-device-current test circuit.

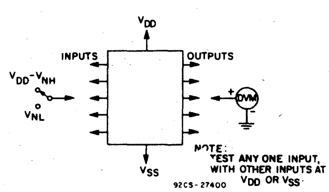


Fig. 12 — Noise-immunity test circuit.

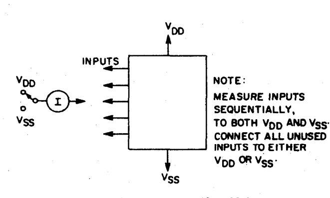


Fig. 13 — Input-leakage-current test circuit.

COS/MOS Dual Complementary Pair Plus Inverter

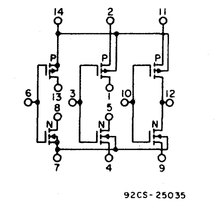
The RCA-CD4007A types are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in Fig. 2.

More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

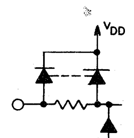
Features:

- **Medium-speed operation. . . .** **$t_{PHL} = t_{PLH}$ = 20 ns (typ.) at C_L = 15 pF, + V_{DD} = 10 V**
- **Low "high" and "low" output impedance. 500 Ω (typ.) at $V_{DD} - V_{SS}$ = 10 V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**



Terminal No.14 – V_{DD}
Terminal No. 7 – V_{SS}

CD4007A SCHEMATIC DIAGRAM



*ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . . +265°C

Applications:

- **Extremely high-input impedance amplifiers**
- **Shapers**
- **Inverters**
- **Threshold detector**
- **Linear amplifiers**

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	D,F,H Packages		E Package		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	12	3	12	V

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
	V_{DD}	D,F,H Packages			E Package			
	(V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time; t_{PLH}, t_{PHL}	5	-	35	60	-	35	75	ns
	10	-	20	40		20	50	
Transition Time; t_{THL}, t_{TLH}	5	–	50	75		50	100	ns
	10	–	30	40		30	50	
Average input Capacitance, C_I	Any Input	–	5	–		5		pF

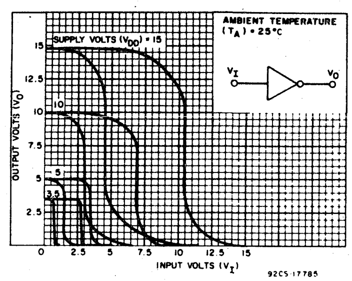


Fig. 1 — Minimum and maximum voltage-transfer characteristics for inverter.

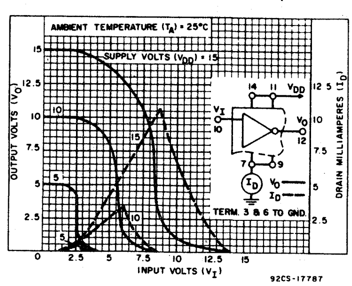


Fig. 2 — Typical current and voltage-transfer characteristics for inverter.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions V_O (V)	V_{IN} (V)	V_{DD} (V)	Limits at Indicated Temperatures (°C) D,F,H Packages −55	+25 Typ.	+25 Limit	+125	E Package −40	+25 Typ.	+25 Limit	+85	Units
Quiescent Device Current:	–	–	5	0.05	0.001	0.05	3	0.5	0.005	0.5	15	
	–	–	10	0.1	0.001	0.1	6	1	0.005	1	30	μA
I_L Max.	–	–	15	2	0.02	2	40	50	0.5	50	500	
Output Voltage Low Level V_{OL}	–	5	5	0 Typ.; 0.05 Max.								
	–	10	10	0 Typ.; 0.05 Max.								V
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								
	7.2	–	10	3 Min.; 4.5 Typ.								V
Inputs High V_{NH}	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low V_{NML}	4.5	–	5	1 Min.								
	9	–	10	1 Min.								V
Inputs High V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink) I_DN Min.	0.4*	V_I =	5	0.75	1	0.6	0.4	0.35	1	0.3	0.24	
	0.5	V_{DD}	10	1.6	2.5	1.3	0.95	1.2	2.5	1	0.8	mA
P-Channel (Source): I_DP Min.	2.5†	V_I =	5	−1.75	−4	−1.4	−1	−1.3	−4	−1.1	−0.9	
	9.5	V_{DD}	10	−1.35	−2.5	−1.1	−0.75	−0.65	−2.5	−0.55	−0.45	
Input Leakage Current: I_{IL}, I_{IH}	– (Any Input)	–	15	$\pm10^{-5}$ Typ., ±1 Max.								μA

*Maximum noise-free low-level bipolar output voltage. †Minimum noise-free high-level bipolar output voltage.

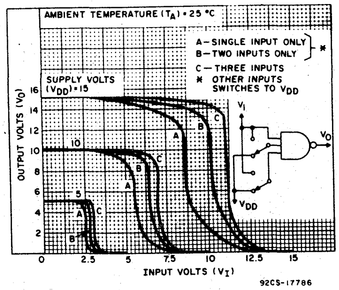


Fig. 3 — Typical voltage-transfer characteristics for NAND gate.

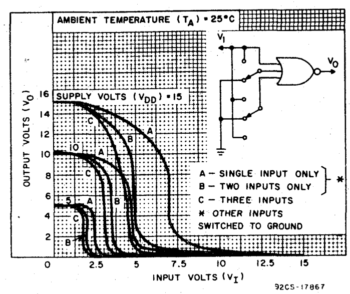


Fig. 4 — Typical voltage-transfer characteristics for NOR gate.

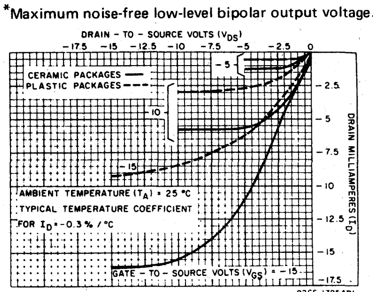


Fig. 5 — Minimum output p-channel drain characteristics.

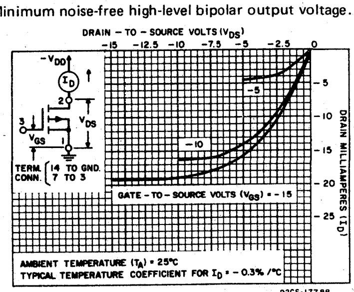


Fig. 6 — Typical output p-channel drain characteristics.

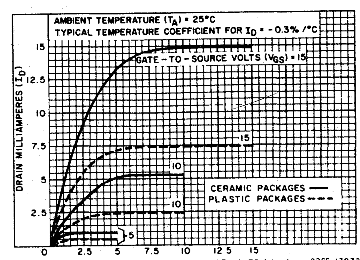


Fig. 7 — Minimum output n-channel drain characteristics.

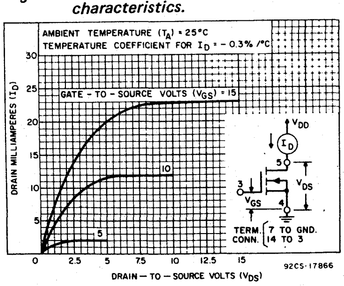


Fig. 8 — Typical output n-channel drain characteristics.

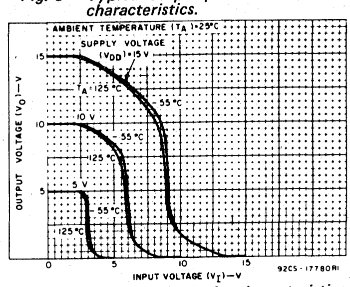


Fig. 9 — Typical voltage-transfer characteristics as a function of temperature.

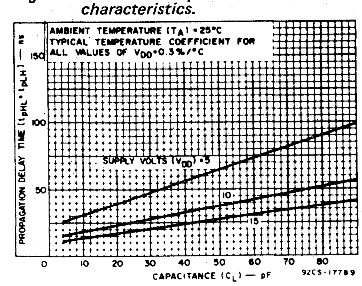


Fig. 10 — Typical propagation-delay time vs. load capacitance.

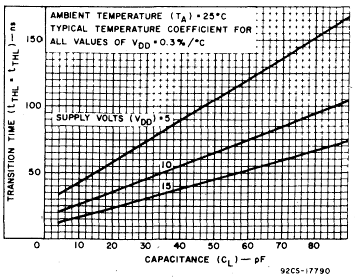


Fig. 11 — Typical transition time vs. load capacitance.

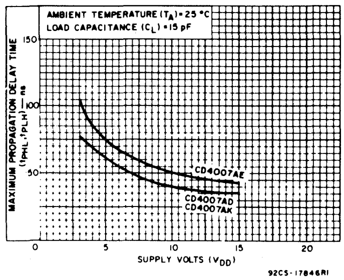


Fig. 12 — Maximum propagation-delay time vs. supply voltage.

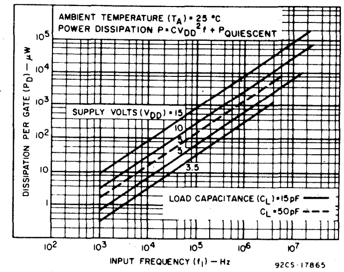
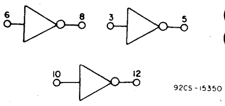
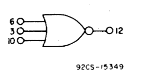


Fig. 13 — Typical dissipation characteristics.



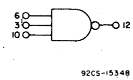
(14,2,11); (8,13); (1,5); (7,4,9)

a) Triple Inverters



(13,2); (1,11); (12,5,8); (7,4,9)

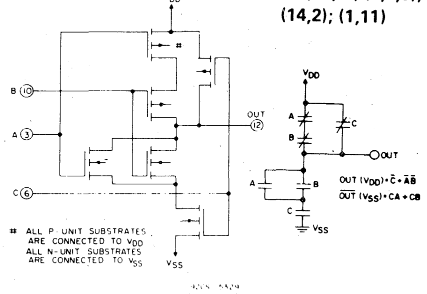
b) 3-Input NOR Gate



(1,12,13); (2,14,11); (4,8); (5,9)

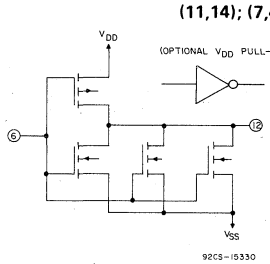
c) 3-Input NAND Gate

(13,12,5); (4,9,8); (14,2); (1,11)



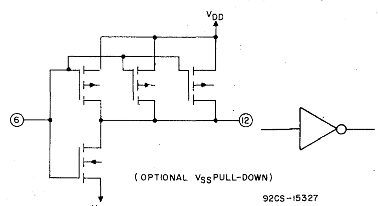
d) Tree (Relay) Logic

(6,3,10); (8.5,12); (11,14); (7,4,9)

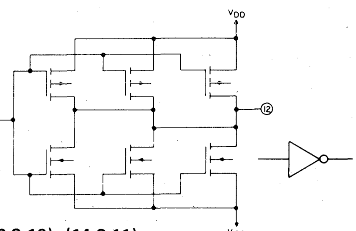


e) High Sink-Current Driver

(6,3,10); (13,1,12); (14,2,11); (7,9)

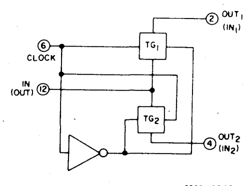


f) High Source-Current Driver



(6,3,10); (14,2,11); (7,4,9); (13,8,1,5,12)

g) High Sink- and Source-Current Driver



(1,5,12); (2,9); (11,4); (8,13,10); (6,3)

h) Dual Bi-Directional Transmission Gating

Fig. 14 — Sample COS/MOS logic circuit arrangements using type CD4007A.

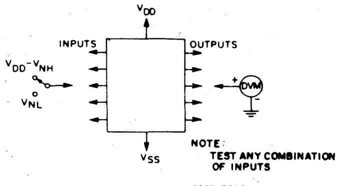


Fig. 15 — Noise-immunity test circuit.

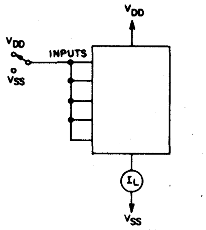


Fig. 16 — Quiescent-device-current test circuit.

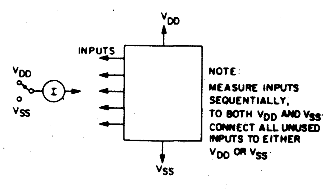


Fig. 17 — Input-leakage-current test circuit.

COS/MOS 4-Bit Full Adder

With Parallel Carry Out

The RCA-CD4008A types consist of four full-adder stages with fast look-ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" bit to permit high-speed operation in arithmetic sections using several CD4008A's. CD4008A inputs include the four sets of bits to be added, A_1 to A_4 and B_1 to B_4, in addition to the "Carry In" bit from a previous section. CD4008A outputs include the four sum bits, S_1 and S_4, in addition to the high-speed "parallel-carry-out" which may be utilized at a succeeding CD4008A section.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications

- Binary addition/arithmetic units

Features:

- **4 sum outputs plus parallel look-ahead carry-output**
- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . +265°C

STATIC ELECTRICAL CHARACTERISTICS

Characteristic		Conditions V_O (V)	V_{IN} (V)	V_{DD} (V)	Limits at Indicated Temperatures (°C) D,F,H Packages −55	+25 Typ.	+25 Limit	+125	E Package −40	+25 Typ.	+25 Limit	+85	Units
Quiescent Device Current, I_L Max.		–	–	5	5	0.3	5	300	50	0.5	50	700	μA
		–	–	10	10	0.5	10	600	500	1	100	1400	
		–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}		–	0,5	5	0 Typ.; 0.05 Max.								V
		–	0,10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}		–	0,5	5	4.95 Min.; 5 Typ.								
		–	0,10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}		4.2	–	5	1.5 Min.; 2.25 Typ.								V
		9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}		0.8	–	5	1.5 Min.; 2.25 Typ.								
		1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}		4.5	–	5	1 Min.								V
		9	–	10	1 Min.								
Inputs High, V_{NMH}		0.5	–	5	1 Min.								
		1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink), I_DN Min.	*	0.5	–	5	0.31	0.5	0.25	0.175	0.155	0.5	0.13	0.105	mA
	*	0.5	–	10	0.93	1.5	0.75	0.53	0.6	1.5	0.5	0.4	
	▲	3	–	5	0.012	0.2	0.01	0.007	0.009	0.2	0.007	0.005	
	▲	3	–	10	0.31	0.5	0.25	0.175	0.24	0.5	0.2	0.16	
p-Channel (Source), I_DP Min.	*	4.5	–	5	-0.31	-0.5	-0.25	-0.175	-0.155	-0.5	-0.13	-0.105	
	*	9.5	–	10	-0.93	-1.5	-0.75	-0.53	-0.6	-1.5	-0.5	-0.4	
	▲	2	–	5	-0.012	-0.2	-0.01	-0.007	-0.008	-0.2	-0.007	-0.005	
	▲	7	–	10	-0.185	-0.3	-0.15	-0.105	-0.12	-0.3	-0.1	-0.08	
Input Leakage Current, I_{IL}, I_{IH} Max.		Any Input		15	$\pm10^{-5}$ Typ.; ±1 Max.								μA

* Carry Output ▲Sum Output

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	Min.	Max.	Units
Supply-Voltage Range (T_A= Full Package-Temp. Range)	3	12	V

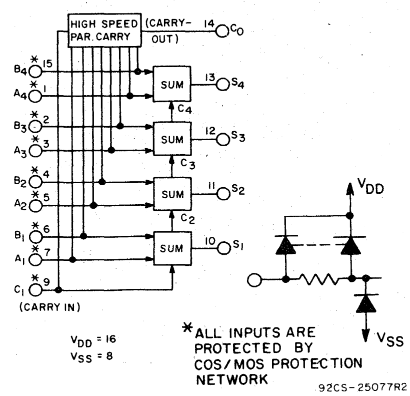


Fig. 1 – CD4008A logic diagram.

TRUTH TABLE

A_i	B_i	C_i	C_O	SUM
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

CD4008A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^{\circ}C$; Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 KΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,H Packages		E Package		
		Typ.	Max.	Typ.	Max.	
Propagation Delay Time: t_{PHL}, t_{PLH} Sum In to Sum Out	5 10	900 325	1300 500	900 325	2000 650	ns
Carry In to Sum Out	5 10	900 325	1300 500	900 325	2000 650	ns
Sum In to Carry Out	5 10	320 120	600 200	320 120	800 240	ns
Carry In to Carry Out	5 10	100 45	175 75	100 45	200 90	ns
Transition Time: t_{THL}, t_{TLH} At Sum Outputs	5 10	1250 550	2200 900	1250 550	2900 1100	ns
At Carry Output	5 10	125 45	225 75	125 45	290 90	ns
Input Capacitance, C_I (Any Input)	–	10	–	10	–	pF

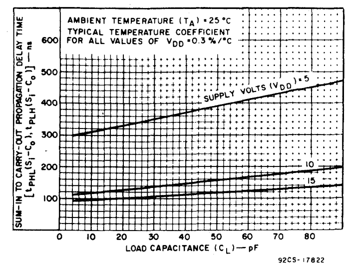


Fig. 2 – Typical sum-in to carry out propagation delay time vs. C_L.

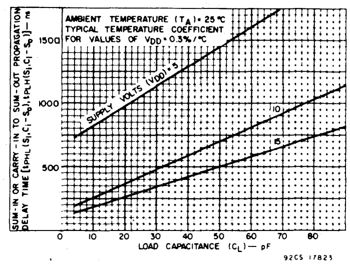


Fig. 3 – Typical sum-in or carry-in to sum-out propagation delay time vs. C_L.

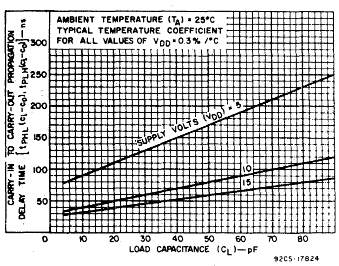


Fig. 4 – Typical carry-in to carry-out propagation delay time vs. C_L.

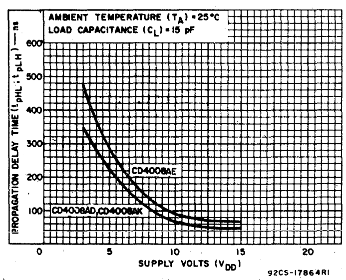


Fig. 5 – Typical maximum propagation delay time vs. V_{DD} for carry-in to carry-out.

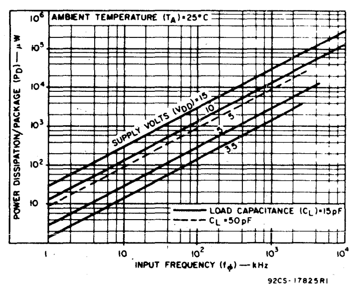


Fig. 6 – Typical dissipation characteristics.

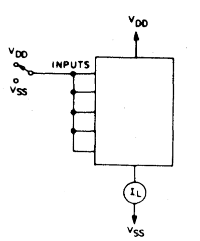


Fig. 7 – Quiescent device current test circuit.

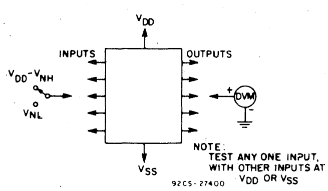


Fig. 8 – Noise immunity test circuit.

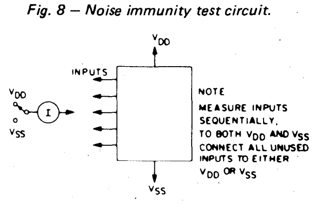


Fig. 9 – Input leakage current test circuit.

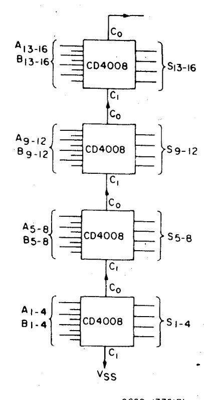


Fig. 10 – Typical connection for a 16-bit adder.

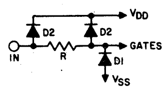
COS/MOS
Hex Buffers/Converters

Inverting Type: CD4009A
Non-Inverting Type: CD4010A

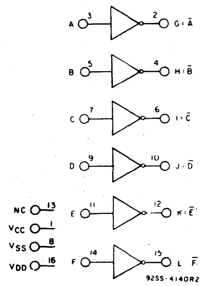
The RCA-CD4009A and CD4010A Hex Buffer/Converters may be used as COS/MOS to TTL or DTL logic-level converters or COS/MOS high sink-current drivers.

The CD4049A and CD4050A are preferred hex buffer replacements for the CD4009A and CD4010A, respectively, in all applications except multiplexers. For applications not requiring high sink current or voltage conversion, the CD4069B Hex Inverter is recommended.

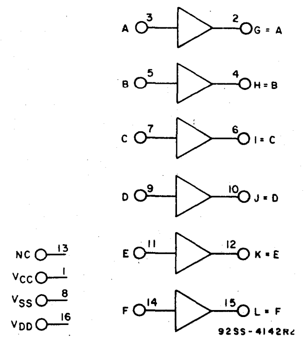
These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK.
92CS-22887R1



CD4009A



CD4010A

Fig. 1 – Logic diagrams.

Features:

- Quiescent current specified to 15 V
- Maximum input leakage of 1 μA at 15 V (full package-temperature range)
- High sink current for driving 2 TTL loads
- High-to-low level logic conversion

Applications:

- COS/MOS to DTL/TTL hex converter
- COS/MOS current "sink" or "source" driver
- COS/MOS high-to-low logic-level converter
- Multiplexer — 1 to 6 or 6 to 1

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range : V_{DD}, V_{CC})	3	12	V
Input Voltage Range (V_I)	V_{CC}*	12	V

* The CD4009 and CD4010 have high-to-low level voltage conversion capability but not low-to-high level, therefore it is recommended that $V_{DD} \geqslant V_I \geqslant V_{CC}$.

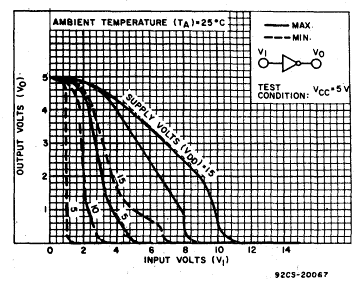


Fig. 2 – Minimum & maximum voltage transfer characteristics – CD4009A.

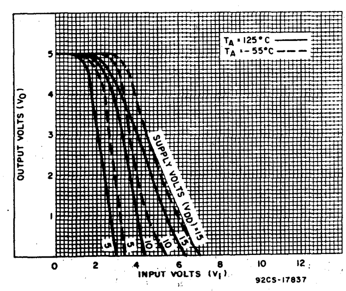


Fig. 3 – Typical voltage transfer characteristics as function of temp. – CD4009A.

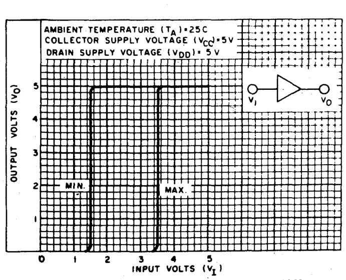


Fig. 4 – Minimum & maximum voltage transfer characteristics (V_{DD} = 5) – CD4010A.

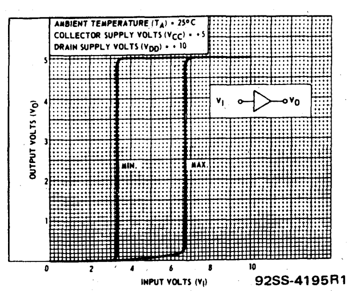


Fig. 5 – Minimum & maximum voltage transfer characteristics (V_{DD} = 10) – CD4010A.

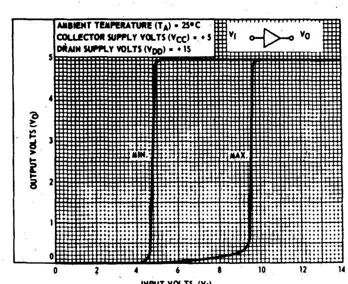


Fig. 6 – Minimum & maximum voltage transfer characteristics (V_{DD} = 15) – CD4010A.

CD4009A, CD4010A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{CC}* (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	0.3	0.01	0.3	20	3	0.03	3	42	μA
	–	–	10	0.5	0.01	0.5	30	5	0.05	5	70	
	–	–	15	10	0.02	10	100	50	0.5	50	500	
Output Voltage: Low-Level, V_{OL}	–	0,5	5	0 Typ.; 0.05 Max.								V
	–	0,10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0,5	5	4.95 Min.; 5 Typ.								
	–	0,10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL} CD4010A	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH} All Types	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Inputs Low, V_{NL} CD4009A	3.6	–	5	1 Min.; 1.5 Typ.								
	7.2	–	10	2 Min.; 3 Typ.								
Noise Margin: Inputs Low, V_{NML} CD4010A	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH} CD4010A	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	3.75	4	3	2.1	3.6	4	3	2.4	mA
	0.5	–	10	10	10	8	5.6	9.6	10	8	6.4	
P-Channel (Source), I_DP Min.	4.6	–	5	-0.31	-0.5	-0.25	-0.175	-0.3	-0.5	-0.25	-0.2	
	2.5	–	5	-1.85	-1.75	-1.25	-0.9	-1.5	-1.75	-1.25	-1	
	9.5	–	10	-0.9	-0.8	-0.6	-0.4	-0.72	-0.8	-0.6	-0.48	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm10^{-5}$ Typ.; ±1 Max.								μA

* $V_{CC} = V_{DD}$

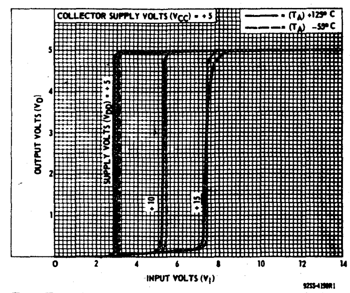


Fig. 7 — Typical voltage transfer characteristics as a function of temperature — CD4010A.

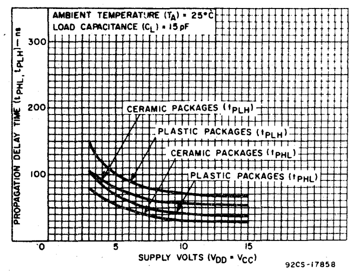


Fig. 8 — Maximum propagation delay time vs. V_{DD} — CD4010A.

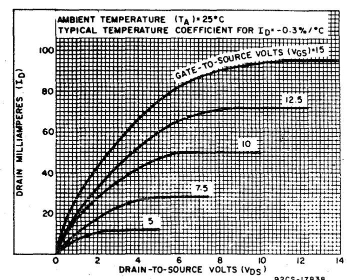


Fig. 9 — Typical n-channel drain characteristics.

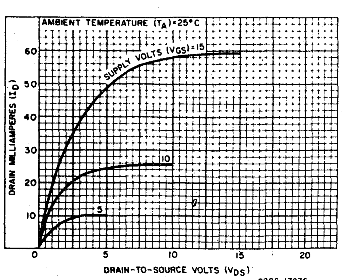


Fig. 10 — Minimum n-channel drain characteristics.

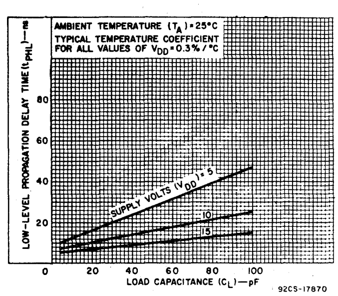


Fig. 11 — Typical high-to-low level propagation delay time vs. C_L.

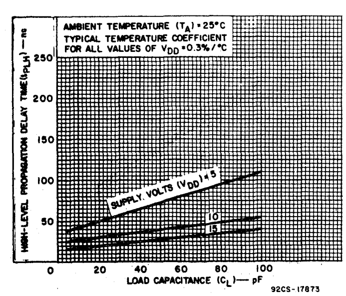


Fig. 12 — Typical low-to-high level propagation delay time vs. C_L.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$; Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 KΩ

CHARACTERISTIC	CONDITION			LIMIT		UNITS
	V_{DD} (V)	V_I (V)	V_{CC} (V)	Typ.	Max.	
D, F, H Packages						
Propagation Delay Time: Low-to-High, t_{PLH}	5	5	5	50	80	ns
	10	10	10	25	55	
	10	10	5	15	30	
High-to-Low, t_{PHL}	5	5	5	15	55	
	10	10	10	10	30	
	10	10	5	10	25	
Transition Time: Low-to-High, t_{TLH}	5	5	5	80	125	ns
	10	10	10	50	100	
High-to-Low, t_{THL}	5	5	5	20	45	
	10	10	10	16	40	
Input Capacitance, C_I CD4009A	–	–	–	15	–	pF
CD4010A	–	–	–	5	–	
E Package						
Propagation Delay Time: Low-to–high, t_{PLH}	5	5	5	50	100	ns
	10	10	10	25	70	
	10	10	5	15	40	
High-to-Low, t_{PHL}	5	5	5	15	70	
	10	10	10	10	40	
	10	10	5	10	35	
Transition Time: Low-to-High, t_{PLH}	5	5	5	80	160	ns
	10	10	10	50	120	
High-to-Low, t_{THL}	5	5	5	20	60	
	10	10	10	16	50	
Input Capacitance, C_I CD4009A	–	–	–	15	–	pF
CD4010A	–	–	–	5	–	

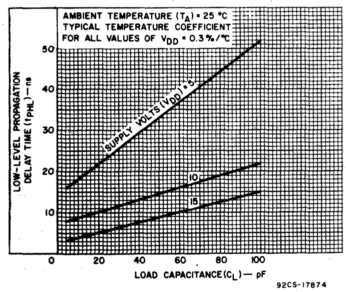


Fig. 13 — Typical high-to-low level propagation delay time vs. C_L (driving TTL, DTL).

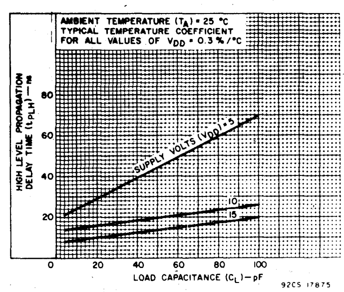


Fig. 14 — Typical low-to-high level propagation delay time vs. C_L (driving TTL, DTL)

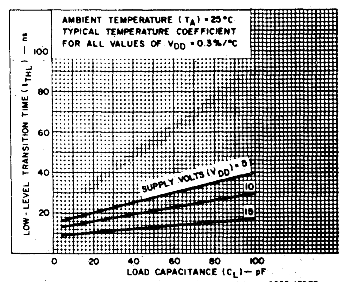


Fig. 15 — Typical high-to-low level transition time vs. C_L.

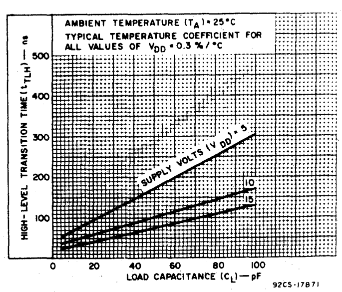


Fig. 16 — Typical low-to-high level transition time vs. C_L.

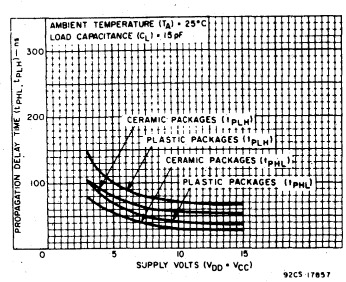


Fig. 17 — Maximum propagation delay time vs. V_{DD} — CD4009A.

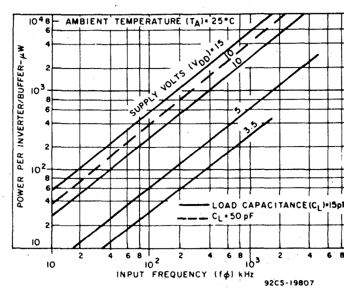


Fig. 18 — Typical dissipation characteristics.

CD4011A, CD4012A, CD4023A Types

COS/MOS NAND Gates

Quad 2 Input – CD4011A
Dual 4 Input – CD4012A
Triple 3 Input – CD4023A

The RCA-CD4011A, CD4012A, and CD-4023A NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of COS/MOS gates.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

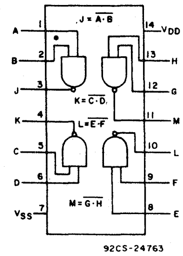
Features:

- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

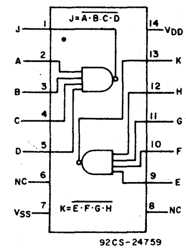
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

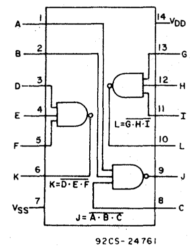
Characteristic	Min.	Max.	Units
Supply Voltage Range (over full package temperature range)	3	12	V



CD4011A

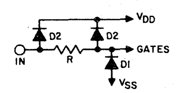


CD4012A



CD4023AH

Fig. 1 – Functional diagrams.



MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . –55 to +125°C
PACKAGE TYPE E . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = –40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . +265°C

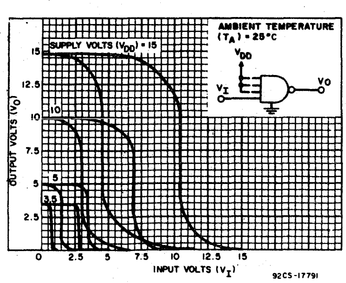


Fig. 2 – Minimum & maximum voltage transfer characteristics.

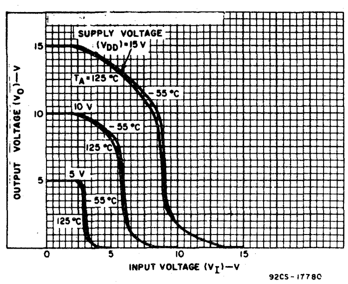


Fig. 3 – Typical voltage transfer characteristics as a function of temperature.

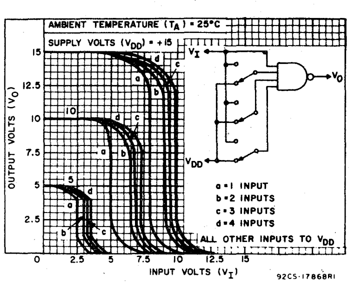


Fig. 4 – Typical multiple input switching transfer characteristics for CD4012A.

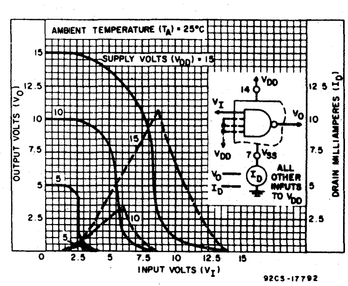


Fig. 5 – Typical current & voltage transfer characteristics.

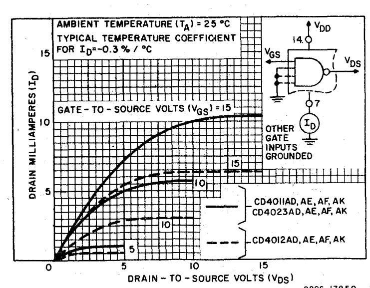


Fig. 6 – Typical n-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	0.05	0.001	0.05	3	0.5	0.005	0.5	15	μA
	–	–	10	0.1	0.001	0.1	6	5	0.005	5	30	
	–	–	15	2	0.02	2	40	50	0.5	50	500	
Output Voltage: Low-Level V_{OL}	–	0,5	5	0 Typ.; 0.05 Max.								V
	–	0,10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}	–	0,5	5	4.95 Min.; 5 Typ.								
	–	0,10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink) I_DN Min. CD4011A CD4023A	0.5	–	5	0.31	0.5	0.25	0.175	0.145	0.5	0.12	0.095	mA
	0.5	–	10	0.62	0.6	0.5	0.35	0.3	0.6	0.25	0.2	
CD4012A	0.5	–	5	0.15	0.25	0.12	0.085	0.072	0.25	0.06	0.05	
	0.5	–	10	0.31	0.6	0.25	0.175	0.155	0.6	0.13	0.105	
P-Channel (Source), I_DP Min. All Types	4.5	–	5	-0.31	-0.5	-0.25	-0.175	-0.145	-0.5	-0.12	-0.095	
	9.5	–	10	-0.75	-1.2	-0.6	-0.4	-0.35	-1.2	-0.3	-0.24	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm10^{-5}$ Typ.; ±1 Max.								μA

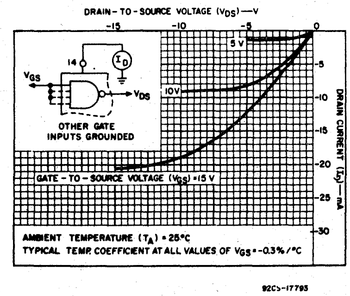


Fig. 7 — Typical p-channel drain characteristics.

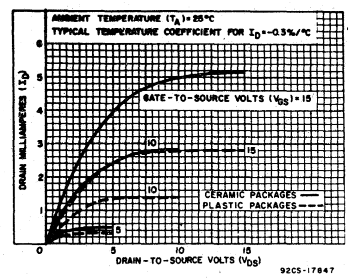


Fig. 8 — Minimum n-channel drain characteristics —CD4011A & CD4023A.

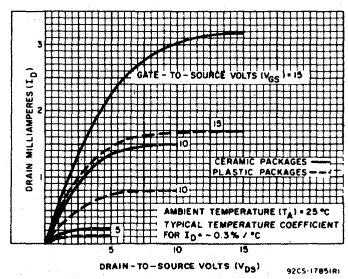


Fig. 9 — Typical n-channel drain characteristics.

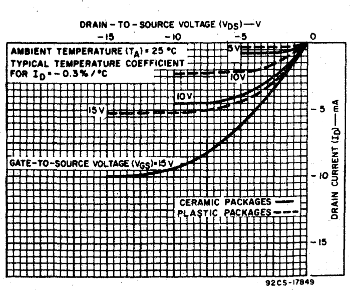


Fig. 10 — Minimum p-channel drain characteristics.

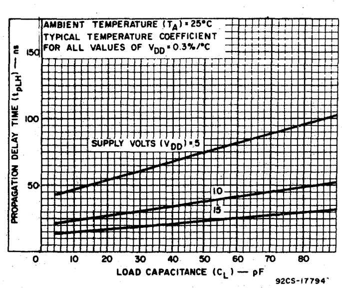


Fig. 11 — Typical low-to-high level propagation delay time vs. C_L.

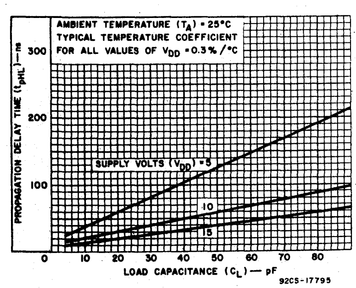


Fig. 12 — Typical high-to-low level propagation delay time vs. C_L — CD4011A, & CD4023A.

CD4011A, CD4012A, CD4023A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^{\circ}C$, $C_L = 15$ pF, Input t_r, $t_f = 20$ ns, $R_L = 200$ KΩ

CHARACTERISTICS	TEST CONDITIONS		LIMITS				UNITS
			D,F,H Packages		E Package		
		V_{DD} (V)	Typ.	Max.	Typ.	Max.	
Propagation Delay Time: Low-to-High Level, t_{PLH}		5	50	75	50	100	ns
		10	25	40	25	50	
High-to-Low Level, t_{PHL} CD4011A and CD4023A		5	50	75	50	100	ns
		10	25	40	25	50	
CD4012A		5	100	150	100	200	ns
		10	50	75	50	100	
Transition Time: Low-to-High Level, t_{TLH}		5	75	100	75	125	ns
		10	40	60	40	75	
High-to-Low Level, t_{THL} CD4011A and CD4023A		5	75	125	75	150	ns
		10	50	75	50	100	
CD4012A		5	250	375	250	500	ns
		10	125	200	125	250	
Input Capacitance, C_I	Any Input		5	–	5	–	pF

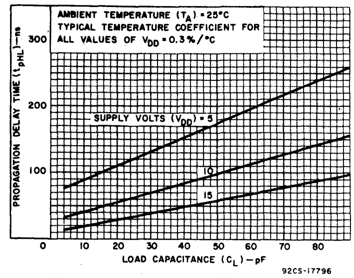


Fig. 13 — Typical high-to-low level propagation delay time vs. C_L — CD4012A.

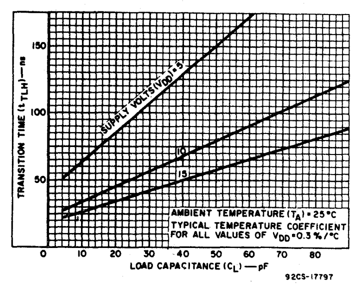


Fig. 14 — Typical low-to-high transition time vs. C_L.

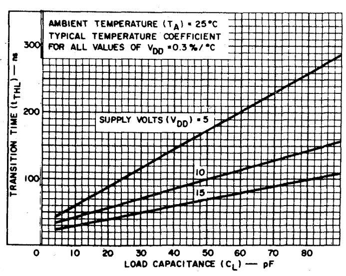


Fig. 15 — Typical high-to-low level transition time vs. C_L — CD4011A & CD4023A.

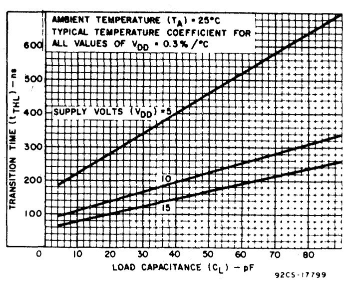


Fig. 16 — Typical high-to-low level transition time vs. C_L — CD4012A.

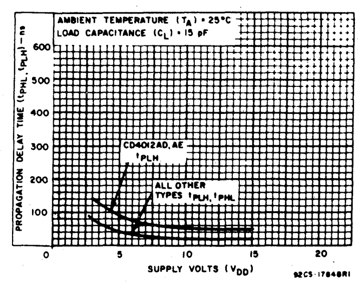


Fig. 17 — Minimum propagation delay time vs. V_{DD}.

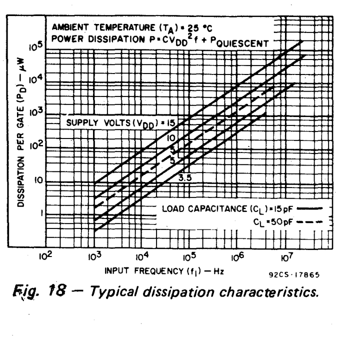


Fig. 18 — Typical dissipation characteristics.

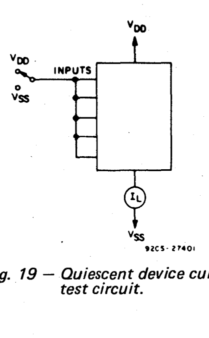


Fig. 19 — Quiescent device current test circuit.

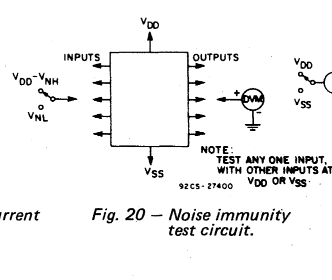


Fig. 20 — Noise immunity test circuit.

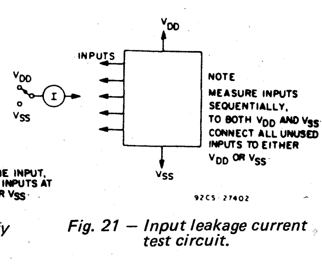


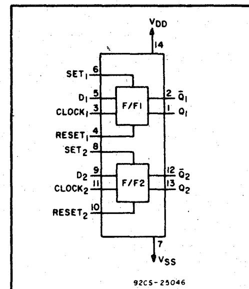
Fig. 21 — Input leakage current test circuit.

Dual 'D'-Type Flip-Flop

The RCA-CD4013A consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs, and Q and $\bar{Q}$ outputs. These devices can be used for shift register applications, and by connecting $\bar{Q}$ output to the data input,* for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse.

Setting or resetting is independent of the clock and is accomplished by a high level on the set (with low-level on reset) or reset (with low-level on set) line, respectively.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4013A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) .... −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
  PACKAGE TYPES D, F, H .... −55 to +125°C
  PACKAGE TYPE E .... −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  (Voltages referenced to V_{SS} Terminal) .... −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
  FOR T_A = −40 to +60°C (PACKAGE TYPE E) .... 500 mW
  FOR T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/°C to 200 mW
  FOR T_A = −55 to +100°C (PACKAGE TYPES D, F) .... 500 mW
  FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) .... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) .... 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C

Features:

- **Set-Reset capability**
- **Static flip-flop operation — retains state indefinitely with clock level either "high" or "low"**
- **Medium-speed operation — 10 MHz (typ.) clock toggle rate at 10 V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 µA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Registers, counters, control circuits**

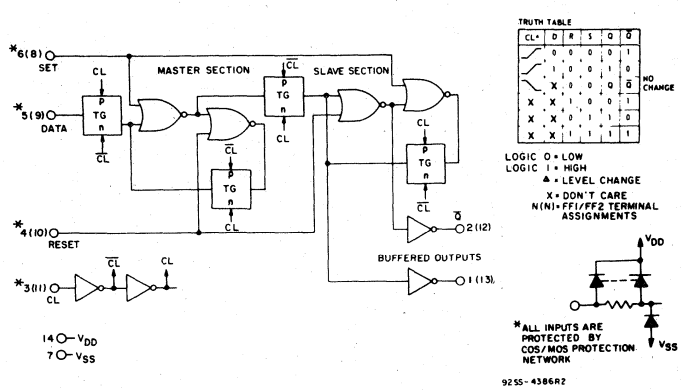


Fig. 1 — Logic diagram and truth table for CD4013A (one of two identical flip flops).

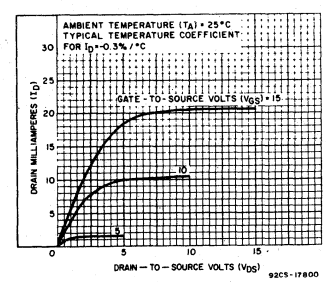


Fig.2 — Typical n-channel drain characteristics.

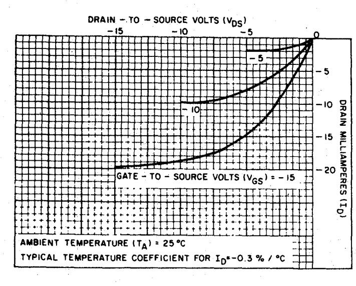


Fig.3 — Typical p-channel drain characteristics.

CD4013A Types

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges –

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,H Packages Min.	Max.	E Package Min.	Max.	UNITS
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	12	3	12	V
Data Setup Time t_S	5	40	–	50	–	ns
	10	20	–	25	–	
Clock Pulse Width t_W	5	200	–	500	–	ns
	10	80	–	100	–	
Clock Input Frequency f_{CL}	5	dc	2.5	dc	1	MHz
	10		7		5	
Clock Rise or Fall Time t_rCL*, t_fCL	5	–	15	–	15	μs
	10	–	5	–	5	
Set or Reset Pulse Width	5	250	–	500	–	ns
	10	100	–	125	–	

* If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

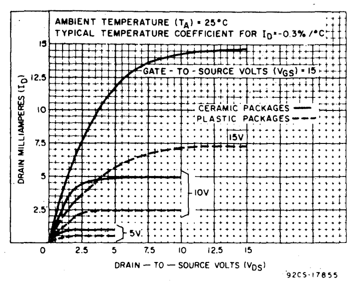


Fig.4 – Minimum n-channel drain characteristics.

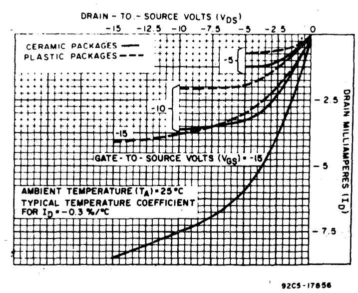


Fig.5 – Minimum p-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,H Packages Min.	Typ.	Max.	E Package Min.	Typ.	Max.	UNITS
Propagation Delay Time: Clock to Q or $\bar{Q}$ Outputs t_{PHL}, t_{PLH}	5	–	150	300	–	150	350	ns
	10	–	75	110	–	75	125	
Set to Q or Reset to $\bar{Q}$ t_{PLH}	5	–	175	300	–	175	350	ns
	10	–	75	110	–	75	125	
Set to $\bar{Q}$ or Reset to Q t_{PHL}	5	–	175	300	–	175	350	ns
	10	–	75	110	–	75	125	
Transition Time, t_{THL}, t_{TLH}	5	–	75	125	–	75	150	ns
	10	–	50	70	–	50	75	
Maximum Clock Input Frequency, f_{CL}	5	2.5	4	–	1	4	–	MHz
	10	7	10	–	5	10	–	
Minimum Clock Pulse Width, t_W	5	–	125	200	–	125	500	ns
	10	–	50	80	–	50	100	
Minimum Set or Reset Pulse Width, t_W	5	–	125	250	–	125	500	ns
	10	–	50	100	–	50	125	
Minimum Data Setup Time, t_S	5	–	20	40	–	20	50	ns
	10	–	10	20	–	10	25	
Clock Rise or Fall Time t_{rCL}, t_{fCL}	5	–	–	15	–	–	15	μs
	10	–	–	5	–	–	5	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

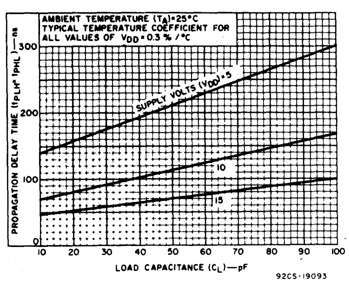


Fig.6 – Typical propagation delay time vs. C_L.

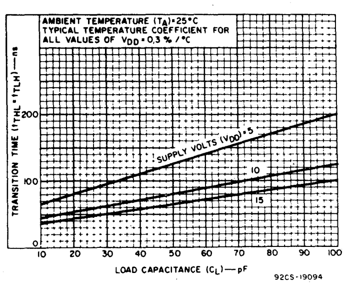


Fig.7 – Typical transition time vs. C_L.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,F,H Packages				E Package				
	V_O	V_{IN}	V_{DD}	−55	+25		+125	−40	+25		+85	
	(V)	(V)	(V)		Typ.	Limit			Typ.	Limit		
Quiescent Device Current, I_L Max.	–	–	5	1	0.005	1	60	10	0.01	10	140	μA
	–	–	10	2	0.005	2	120	20	0.02	20	280	μA
	–	–	15	25	0.5	25	1000	250	2.5	250	2500	μA
Output Voltage: Low-Level, V_{OL}	–	0.5	5	0 Typ.; 0.05 Max.								V
	–	0.10	10	0 Typ.; 0.05 Max.								V
High-Level V_{OH}	–	0.5	5	5 Typ.; 4.95 Min.								V
	–	0.10	10	10 Typ.; 9.95 Min.								V
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	2.25 Typ.; 1.5 Min.								V
	9	–	10	4.5 Typ.; 3 Min.								V
Inputs High V_{NH}	0.8	–	5	2.25 Typ.; 1.5 Min.								V
	1	–	10	4.5 Typ.; 3 Min.								V
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								V
Inputs High, V_{NMH}	0.5	–	5	1 Min.								V
	1	–	10	1 Min.								V
Output Drive Current: N-Channel (Sink) I_DN Min.	0.5	–	5	0.65	1	0.5	0.35	0.35	1	0.3	0.24	mA
	0.5	–	10	1.25	2.5	1	0.75	0.72	2.5	0.6	0.5	mA
P-Channel (Source) I_DP Min.	4.5	–	5	−0.31	−0.5	−0.25	−0.175	−0.17	−0.5	−0.14	−0.12	mA
	9.5	–	10	−0.8	−1.3	−0.65	−0.45	−0.4	−1.3	−0.33	−0.27	mA
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ.; ±1 Max.								μA

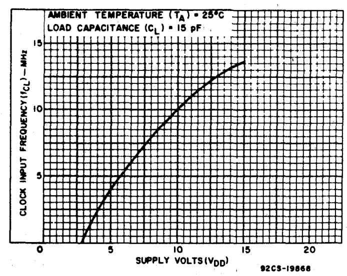


Fig.8 – Typical maximum clock input frequency vs. V_{DD}.

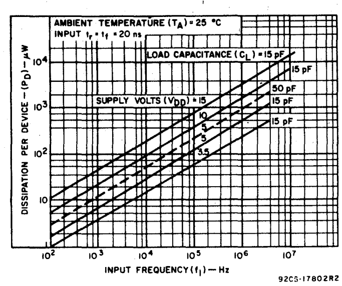


Fig.9 – Typical dissipation characteristics.

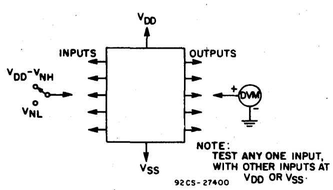


Fig.10 – Noise immunity test circuit.

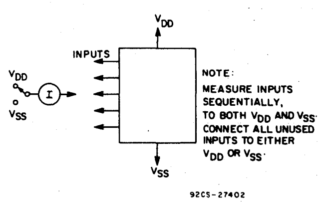


Fig.11 – Input leakage test circuit.

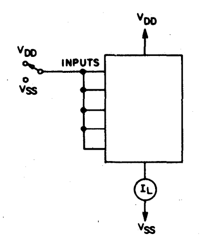


Fig.12 – Quiescent device-current test circuit.

CD4014A Types

COS/MOS 8-Stage Static Shift Register

Synchronous Parallel or Serial Input/Serial Output

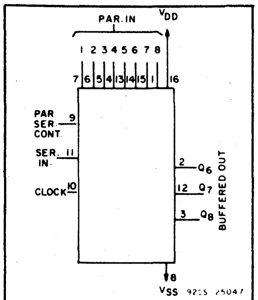
RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,H *Packages*		*E* *Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5 10	350 80	– –	500 100	– –	ns
Clock Pulse Width, t_W	5 10	500 175	– –	830 200	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 3	dc dc	0.6 2.5	MHz
Clock Rise and Fall Time, t_rCL, t_fCL*	5 10	– –	15 5	– –	15 5	μs

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,F,H Packages				*E Package*				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	+25 Typ.	+25 Limit	+125	–40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	5	0.5	5	300	50	0.5	50	700	μA
	–	–	10	10	1	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink), I_DN Min.	0.5	–	5	0.15	0.3	0.12	0.085	0.072	0.3	0.06	0.05	mA
	0.5	–	10	0.31	0.5	0.25	0.175	0.12	0.5	0.1	0.08	
p-Channel (Source): I_DP Min.	4.5	–	5	-0.1	-0.16	-0.08	-0.055	-0.06	-0.16	-0.05	-0.04	
	9.5	–	10	-0.25	-0.44	-0.20	-0.14	-0.12	-0.44	-0.1	-0.08	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm 10^{-5}$ Typ.; ±1 Max.								μA



CD4014A FUNCTIONAL DIAGRAM

The RCA-CD4014A types are 8-stage parallel-input/serial output registers having common CLOCK and PARALLEL/SERIAL CONTROL INPUTS, a single SERIAL DATA INPUT, and individual parallel "JAM" INPUTS to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7. Parallel as well as serial entry is made into the register synchronous with the positive clock line transition and under control of the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. Register expansion using multiple CD4014A packages is permitted.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

CL▲	SER. IN	PAR SER CONTROL	PI-1	PI-n	Q_1 (INTERNAL)	Q_n	
/	X	1	0	0	0	0	
/	X	1	1	0	1	0	
/	X	1	0	1	0	1	
/	X	1	1	1	1	1	
/	0	0	X	X	0	Q_{n-1}	
/	1	0	X	X	1	Q_{n-1}	
\	X	X	X	X	Q_1	Q_n	NC

X = DON'T CARE CASE ▲ = LEVEL CHANGE

NC = NO CHANGE

Fig. 1 – Truth table.

Features:

- Medium speed operation. . . . . 5 MHz (typ.) clock rate at $V_{DD} - V_{SS}$ = 10 V
- Fully static operation
- 8 master-slave flip-flops plus output buffering and control gating
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 µA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Synchronous parallel input/serial output data queueing
- Parallel to serial data conversion
- General-purpose register

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D,F,H Packages			E Package			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time; t_{PLH}, t_{PHL}		5	–	300	750	–	300	1000	ns
		10	–	100	225	–	100	300	
Transition Time; t_{THL}, t_{TLH}		5	–	150	300	–	150	400	ns
		10	–	75	125	–	75	150	
Maximum Clock Input Frequency, f_{CL}		5	1	2.5	–	0.6	2.5	–	MHz
		10	3	5	–	2.5	5	–	
Minimum Clock Pulse Width, t_W		5	–	200	500	–	200	830	ns
		10	–	100	175	–	100	200	
Clock Rise & Fall Time; t_rCL, t_fCL*		5	–	–	15	–	–	15	µs
		10	–	–	5	–	–	5	
Minimum Data Set Up Time, t_S		5	–	100	350	–	100	500	ns
		10	–	50	80	–	50	100	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

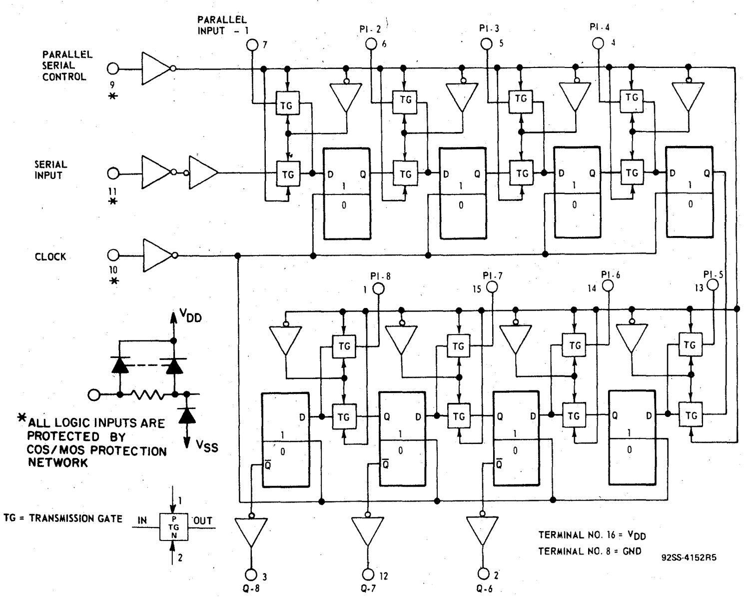


Fig. 5 – Logic block diagram.

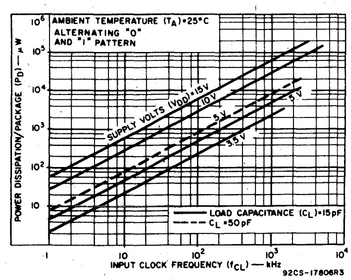


Fig. 2 – Typical dissipation characteristics.

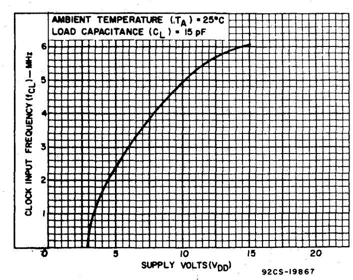


Fig. 3 – Typical clock input frequency vs. supply voltage.

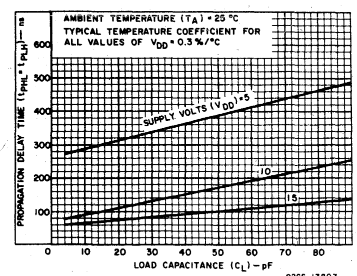


Fig. 4 – Typical propagation delay time vs. load capacitance.

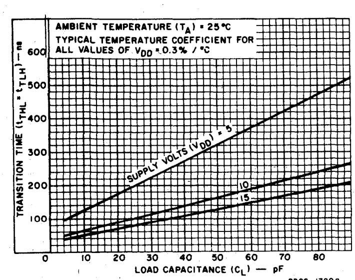


Fig. 6 – Typical transition time vs. load capacitance.

CD4015A Types

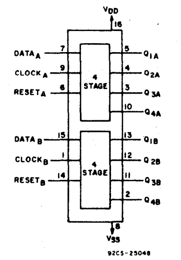
COS/MOS Dual 4-Stage Static Shift Register

With Serial Input/Parallel Output

The RCA-CD4015A consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the DATA input is transferred into the first register stage and shifted over one stage at each positive-going clock transition.

Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one CD4015A package, or to more than 8 stages using additional CD4015A's is possible.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4015A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . -65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . -55 to +125°C
PACKAGE TYPE E . . . . -40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal). . . . . -0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = -40 to + 60°C (PACKAGE TYPE E) . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . Derate Linearly at 12mW/°C to 200 mW
FOR T_A = -55 to + 100°C (PACKAGE TYPES D, F) . . . . 500 mW
FOR T_A = + 100 to +125°C (PACKAGE TYPES D, F) . . . .Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES). . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . .-0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:*

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5 10	350 80	– –	500 100	– –	ns
Clock Pulse Width, t_W	5 10	500 175	– –	830 200	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 3	dc dc	0.6 2.5	MHz
Clock Rise and Fall Time, t_rCL, t_fCL*	5 10	– –	15 5	– –	15 5	µs
Clock Reset Pulse Width, t_W	5 10	500 175	– –	830 200	– –	ns

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

Features:

- **Medium speed operation. . . . . 5 MHz (typ.) clock rate at $V_{DD} - V_{SS}$ = 10V**
- **Fully static operation**
- **8 master-slave flip-flops plus output buffering**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 µA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Serial-input/parallel-output data queueing**
- **Serial to parallel data conversion**
- **General-purpose register**

TRUTH TABLE

CL▲	D	R	Q_1	Q_n
↑	0	0	0	Q_{n-1}
↑	1	0	1	Q_{n-1}
↓	X	0	Q_1	Q_n (NO CHANGE)
X	X	1	0	0

▲= LEVEL CHANGE
X = DON'T CARE CASE

Fig. 1 — Truth table.

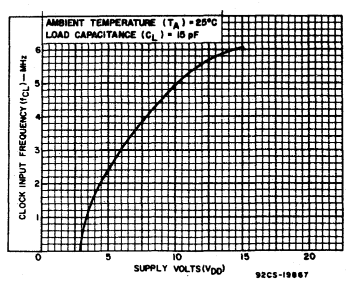


Fig. 2 — Typical clock input frequency vs. supply voltage.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) D, F, H PACKAGES -55	+25 TYP.	+25 LIMIT	+125	E PACKAGE -40	+25 TYP.	+25 LIMIT	+85	UNITS
Quiescent Device Current, I_L Max.	–	–	5	5	0.5	5	300	50	0.5	50	700	µA
	–	–	10	10	1	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max								V
	–	10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.5	–	5	0.15	0.3	0.12	0.085	0.072	0.3	0.06	0.05	mA
	0.5	–	10	0.31	0.5	0.25	0.175	0.12	0.5	0.1	0.08	
P-Channel (Source): I_DP Min.	4.5	–	5	-0.1	-0.16	-0.08	-0.055	-0.06	-0.16	-0.05	-0.04	
	9.5	–	10	-0.25	-0.44	-0.20	-0.14	-0.12	-0.44	-0.1	-0.08	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm10^{-5}$ Typ., ±1 Max.								µA

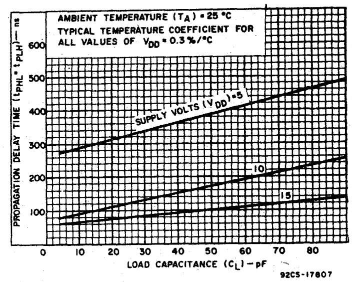


Fig. 3. – Typical propagation-delay time vs. load capacitance.

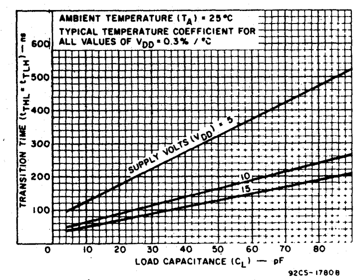


Fig. 4 – Typical transition time vs load capacitance.

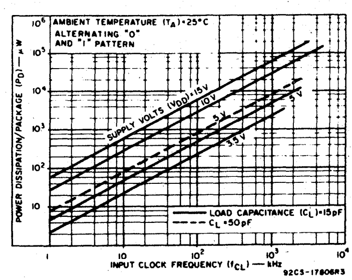


Fig. 5 – Typical dissipation characteristics.

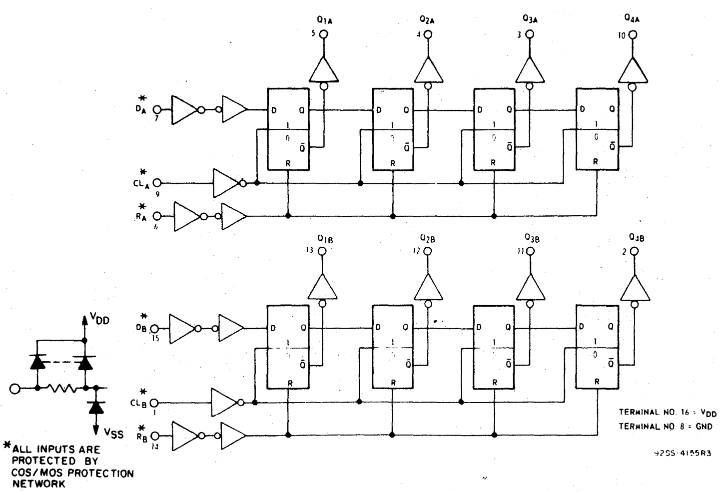


Fig. 6 – Logic diagram.

CD4015A Types

DYNAMIC ELECTRICAL CHARACTERISTICS
at $T_A = 25°C$, Input t_r, $t_f = 20$ ns, $C_L = 15$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS D, F, H PACKAGES MIN.	TYP.	MAX.	E PACKAGE MIN.	TYP.	MAX.	UNITS
CLOCKED OPERATION									
Propagation Delay Time; T_{PLH}, T_{PHL}		5	–	300	750	–	300	1000	ns
		10	–	100	225	–	100	300	
Transition Time; t_{THL}, t_{TLH}		5	–	150	300	–	150	400	ns
		10	–	75	125	–	75	150	
Minimum Clock Pulse Width, t_W		5	–	200	500	–	200	830	ns
		10	–	100	175	–	100	200	
Clock Rise & Fall Time; t_rCL, t_fCL*		5	–	–	15	–	–	15	μs
		10	–	–	5	–	–	5	
Minimum Data Set-up Time, t_S		5	–	100	350	–	100	500	ns
		10	–	50	80	–	50	100	
Maximum Clock Input Frequency, f_{CL}		5	1	2.5	–	0.6	2.5	–	MHz
		10	3	5	–	2.5	5	–	
Average Input Capacitance, C_I			–	5	–	–	5	–	pF
RESET OPERATION									
Propagation Delay Time, T_{PHL}		5	–	300	750	–	300	1000	ns
		10	–	100	225	–	100	300	
Minimum Reset Pulse Width t_W		5	–	200	500	–	200	830	ns
		10	–	100	175	–	100	200	

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitve load.

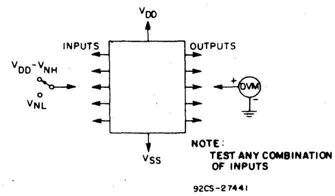


Fig. 7 — Noise-immunity test circuit.

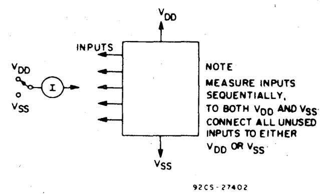
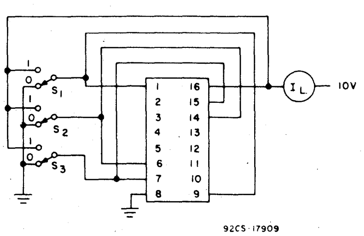


Fig. 8 — Input-leakage-current test circuit.

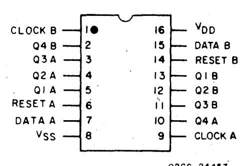


Test performed with the following sequence of "1's" and "0's"

	S_1	S_2	S_3
Test	0	1	0
Don't Test	0	0	1
Don't Test	1	0	1
Don't Test	0	0	0
Don't Test	1	0	0
Don't Test	0	0	1
Test	1	0	1
Don't Test	0	0	0
Test	1	0	0

Fig. 9 — Quiescent-device-current test circuit.

TERMINAL DIAGRAM
Top View



COS/MOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

The RCA-CD4016A Series types are quad bilateral switches intended for the transmission or multiplexing of analog or digital signals. Each of the four independent bilateral switches has a single control signal input which simultaneously biases both the p and n device in a given switch ON or OFF.

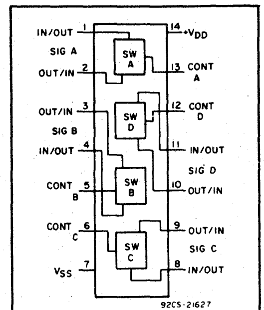
These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **15-V digital or ± 7.5-V peak-to-peak switching**
- **280-Ω typical ON resistance for 15-V operation**
- **Switch ON resistance matched to within 10 Ω typ. over 15-V signal-input range**
- **High ON/OFF output-voltage ratio: 65 dB typ. @ f_{is} = 10 kHz, R_L = 10 kΩ**
- **High degree of linearity: <0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 V_{p-p}, $V_{DD}-V_{SS} \geqslant$ 10 V, R_L = 10 kΩ**
- **Extremely low OFF switch leakage resulting in very low offset current and high effective OFF resistance: 100 pA typ. @ $V_{DD}-V_{SS}$ = 10 V, T_A = 25°C**
- **Extremely high control input impedance (control circuit isolated from signal circuit: 10^{12} Ω typ.**
- **Low crosstalk between switches: –50 dB typ. @ f_{is} = 0.9 MHz, R_L = 1 kΩ**
- **Matched control-input to signal-output capacitance: Reduces output signal transients**
- **Frequency response, switch ON = 40 MHz (typ.)**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**

Applications:

- **Analog signal switching/multiplexing**
  - **Signal gating**
  - **Squelch control**
  - **Chopper**
- **Modulator**
- **Demodulator**
- **Commutating switch**
- **Digital signal switching/multiplexing**
- **COS/MOS logic implementation**
- **Analog-to-digital & digital-to-analog conversion**
- **Digital control of frequency, impedance, phase, and analog-signal gain**



FUNCTIONAL DIAGRAM

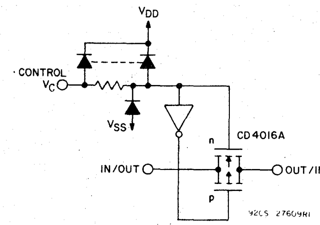


Fig. 1—Schematic diagram — 1 of 4 identical sections.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS Min.	LIMITS Max.	UNITS
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	12	V

TYPICAL "ON" RESISTANCE CHARACTERISTICS

CHARACTERISTIC*	SUPPLY CONDITIONS V_{DD} (V)	V_{SS} (V)	LOAD CONDITIONS R_L = 1kΩ VALUE (Ω)	V_{is} (V)	R_L = 10kΩ VALUE (Ω)	V_{is} (V)	R_L = 100kΩ VALUE (Ω)	V_{is} (V)
R_{ON}	+15	0	200	+15	200	+15	180	+15
			200	0	200	0	200	0
R_{ON}(max.)	+15	0	300	+11	300	+9.3	320	+9.2
R_{ON}	+10	0	290	+10	250	+10	240	+10
			290	0	250	0	300	0
R_{ON}(max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
R_{ON}	+ 5	0	860	+ 5	470	+ 5	450	+ 5
			600	0	580	0	800	0
R_{ON}(max.)	+ 5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
R_{ON}	+7.5	–7.5	200	+7.5	200	+7.5	180	+7.5
			200	-7.5	200	7.5	180	-7.5
R_{ON}(max.)	+7.5	–7.5	290	+0.25	280	+25	400	+0.25
R_{ON}	+ 5	– 5	260	+ 5	250	+ 5	240	+ 5
			310	– 5	250	5	240	– 5
R_{ON}(max.)	+ 5	– 5	600	+0.25	580	+0.25	760	+0.25
R_{ON}	+2.5	-2.5	590	+2.5	450	+2.5	490	+2.5
			720	–2.5	520	–2.5	520	–2.5
R_{ON}(max.)	+2.5	–2.5	232k	+0.25	300k	+0.25	870k	+0.25

* Variation from a perfect switch, R_{ON} = 0Ω.

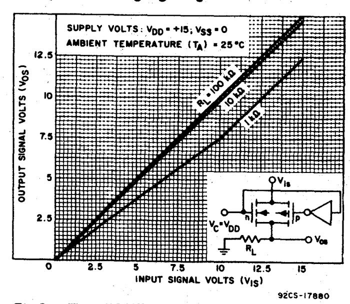


Fig.2 – Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +15 V, V_{SS} = 0 V.

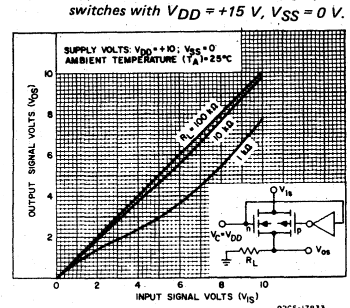


Fig.3 – Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +10 V, V_{SS} = 0 V.

CD4016A Types

ELECTRICAL CHARACTERISTICS (All inputs. . . . . $V_{SS} \leq V_I \leq V_{DD}$)

Recommended DC Supply Voltage ($V_{DD}-V_{SS}$). . 3 to 15 V)

Characteristic	Test Conditions (All Voltage Values are in Volts)		V_{DD} (V)	Limits: Values at −55°C, +25°C, +125°C Apply to D, F, H Packages; Values at −40°C, +25°C, +85°C Apply to E Package: −55°	−40°	+85°	+125°	+25°C Typ.	+25°C Max.	Unit
Quiescent Device Current, I_L max (All switches ON or all Switches OFF) D,F,H Pkgs.			5	0.25	–	–	10	0.01	0.25	μA
			10	0.5	–	–	20	0.01	0.5	
			15	2	–	–	40	0.01	2	
E,Y Pkgs.			5	–	0.25	5	–	–	0.25	μA
			10	–	0.5	10	–	–	0.5	
			15	–	2	20	–	–	2	
Signal Inputs (V_{is}) and Outputs (V_{os})										
	$V_C=V_{DD}$	V_{SS}	V_{is}	Typ/Max	Typ/Max	Typ/Max	Typ/Max			
ON Resistance, R_{ON}	$R_L = 10\ k\Omega$●									Ω
	+7.5	−7.5	+7.5	120/360	130/370	260/520	300/600	200	400	
			−7.5	120/360	130/370	260/520	300/600	200	400	
			±0.25	130/775	160/790	400/1080	470/1230	280	850	
	+5	−5	+5	130/600	150/610	340/840	400/960	250	660	
			−5	130/600	150/610	340/840	400/960	250	660	
			±0.25	325/1870	370/1900	770/2380	900/2600	580	2000	
	+15	0	+15	120/360	130/370	260/520	300/600	200	400	
			+0.25	120/360	130/370	260/520	300/600	200	400	
			+9.3	150/775	180/790	400/1080	490/1230	300	850	
	+10	0	+10	130/600	150/610	340/840	400/960	250	660	
			+0.25	130/600	150/610	340/840	400/960	250	660	
			+5.6	300/1870	350/1900	750/2380	880/2600	560	2000	
ΔON Resistance Between Any 2 of 4 Switches ΔR_{ON}	$R_L = 10\ k\Omega$●									Ω
	+7.5	−7.5	±7.5	–	–	–	–	10	–	
	+5	−5	±5	–	–	–	–	15	–	
Sine Wave Response (Distortion)	+5	−5	5 p-p▲							
	$R_L = 10\ k\Omega$, $f_{is} = 1$ kHz			–	–	–	–	0.4	–	%
Frequency Response Switch ON (Sine-Wave Input)	$V_{DD}=+5$, $V_C=V_{SS}=-5$		−5 p-p							
	$R_L = 1\ k\Omega$; $20 \log_{10} \frac{V_{os}}{V_{is}} = -3$ dB			–	–	–	–	40	–	MHz
Feedthrough Switch OFF	+5	−5	−5 p-p							
	$R_L = 1\ k\Omega$; $20 \log_{10} \frac{V_{os}}{V_{is}} = -50$ dB			–	–	–	–	1.25	–	MHz
Input or Output Leakage Current Switch OFF (Effective OFF Resistance)	V_{DD}	$V_C=V_{SS}$								
	+7.5	−7.5	±7.5	–	–	–	–	±100	–	pA
	+5	−5	±5	–	–	–	–	$\pm 10 \times 10^{-3}$	±125*	nA

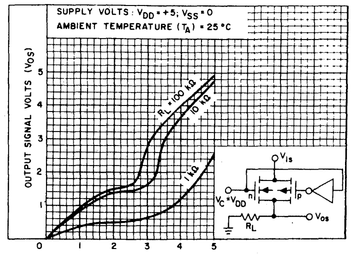


Fig. 4 – Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = 0 V.

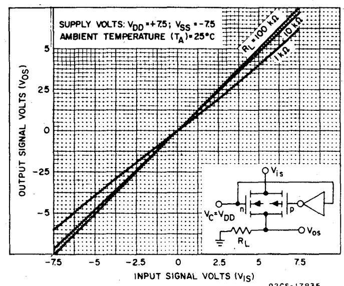


Fig.5 – Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +7.5 V, V_{SS} = -7.5 V.

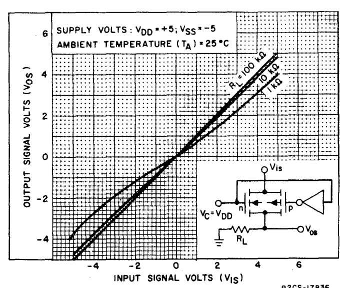


Fig.6 – Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = -5 V.

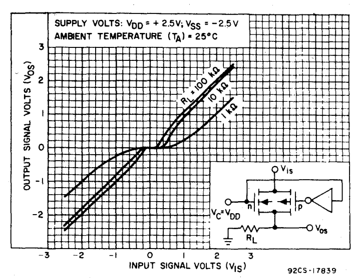


Fig.7 – Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +2.5 V, V_{SS} = -2.5 V.

ELECTRICAL CHARACTERISTICS (Cont'd) . . . . $V_{SS} \leq V_I \leq V_{DD}$)
Recommended DC Supply Voltage (V_{DD}–V_{SS}) . . 3 to 15 V)

Characteristic	Test Conditions — All Voltage Values are in Volts	V_{DD} (V)	Limits: Values at –55°C,+25°C,+125°C Apply to D,F,H Packages; Values at –40°C,+25°C,+85°C Apply to E Package — –55°	–40°	+85°	+125°	+25°C Typ.	+25°C Max.	Unit
Crosstalk Between Any 2 of 4 Switches (f = –50 dB)	$V_C(A)=V_{DD}=+5$, $V_C(B)=V_{SS}=-5$, $V_{is}(A)$ = 5 p-p, R_L=1 kΩ, $20 \log_{10} \frac{V_{os}(B)}{V_{is}(A)} = -50$ dB		–	–	–	–	0.9	–	MHz
Propagation Delay (Signal Input to Signal Output) t_{pd}	$V_C = V_{DD}$ = 10, V_{SS} = GND, C_L = 50 pF, V_{is} = 10 Sq. Wave, t_r, t_f = 20 ns	5					20	50	ns
		10					10	25	ns
Capacitance: Input, C_{is}	V_{DD}=+5, $V_{CC}=V_{SS}=-5$		–	–	–	–	4	–	pF
Output, C_{os}			–	–	–	–	4	–	pF
Feedthrough, C_{ios}			–	–	–	–	0.2	–	pF
Control (V_C)†									
Switch Threshold Voltage, V_{TH}	$V_{is} \leq V_{DD}$, I_{is}=10µA, V_{DD}-V_{SS}=15,10,5		0.7min 2.9max	– –	– –	0.2min 2.4max	0.5min 1.5	2.7	V
Input Leakage Current, I_{IL} max	$V_{is} \leq V_{DD}$	15	±10^{-5} typ; ±1 max.						µA
Crosstalk (Control Input to Signal Output)	V_C=10 (Sq.Wave), t_r,t_f=20 ns, R_L=10 kΩ	10	–	–	–	–	50	–	mV
Turn-On Propagation Delay, t_p dc	V_{DD}–V_{SS}=10, V_C =10 (See Fig.25), t_r,t_f=20 ns, C_L=15 pF, R_L= 1 kΩ	5	–	–	–	–	20	40	ns
		10	–	–	–	–	10	20	ns
Maximum Allowable Control Input Repetition Rate	V_{DD}=10, V_{SS}=GND, R_L=1 kΩ, C_L=15 pF, V_{CC}=10(Sq.Wave), t_r,t_f = 20 ns		–	–	–	–	10	–	MHz
Av. Input Capacitance, C_I			–	–	–	–	5	–	pF

* Limit determined by minimum feasible leakage current measurement for automatic testing.
▲ Symmetrical about 0 volts.
● For all test conditions.
† All control inputs protected by COS/MOS protection network.

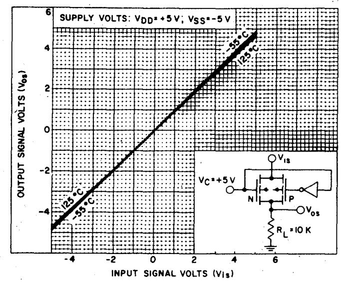


Fig.8 – Typ. "ON" characteristics as a function of temp. for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = -5 V.

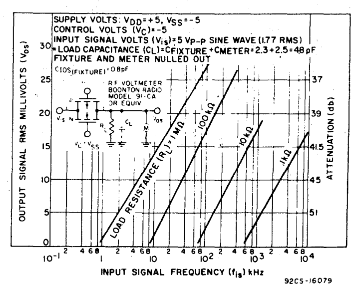


Fig.9 – Typ. feedthru vs. frequency – switch "OFF".

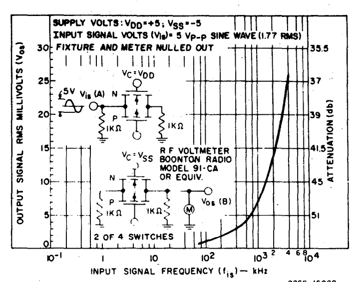


Fig.10 – Typical crosstalk between switch circuits in the same package.

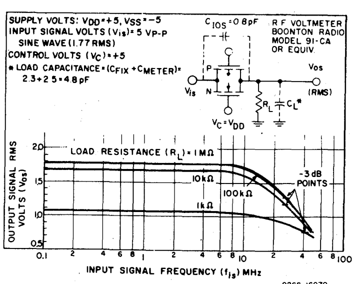


Fig.11 – Typical switch frequency response – switch "ON".

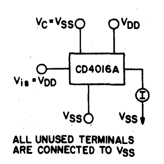


Fig.12 – "OFF" switch input or output leakage current test circuit.

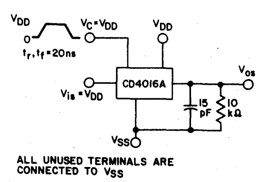


Fig.13 – Test circuit for square-wave response.

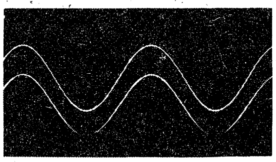


Fig. 14 – Typical sine wave response of V_{DD} = +7.5 V, V_{SS} = –7.5 V.

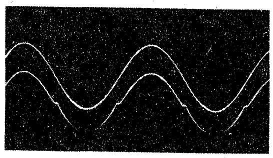


Fig. 15 – Typical sine wave response of V_{DD} = +2.5 V, V_{SS} = –2.5 V.

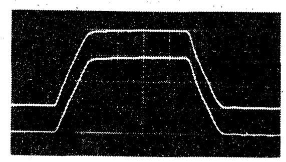


Fig. 16 – Typical square wave response at V_{DD} = V_C = +15 V, V_{SS} = Gnd.

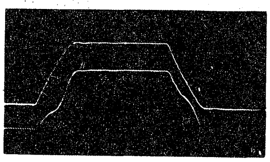


Fig. 17 – Typical square wave response at V_{DD} = V_C = +5 V, V_{SS} = Gnd.

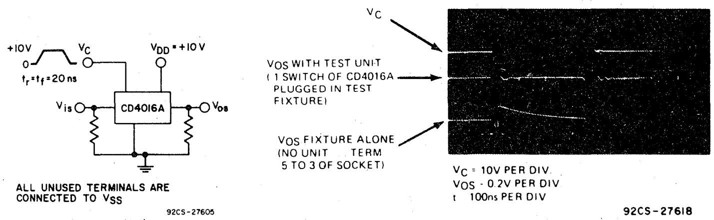


Fig. 18 – Crosstalk-control input to signal output.

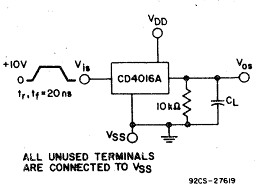


Fig. 19 – Propagation delay time signal input (V_{IS}) to signal output (V_{OS}).

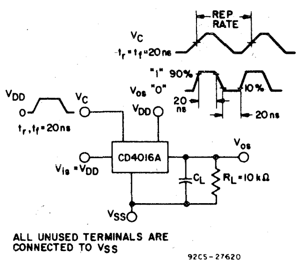


Fig. 20 – Max. allowable control-input repetition rate.

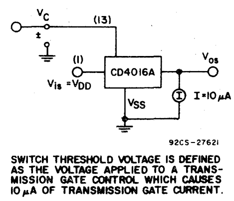


Fig. 21 – Switch threshold voltage.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	–65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	–55 to +125°C
PACKAGE TYPE E	–40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	–0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F,)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F,)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

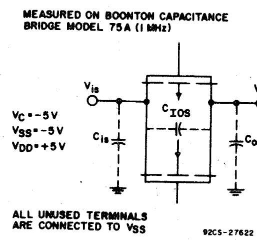


Fig. 22 – Capacitance C_{IOS} and C_{OS}.

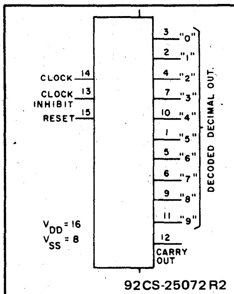
COS/MOS Decade Counter/Divider

Plus 10 Decoded Decimal Outputs

The RCA-CD4017A consists of a 5-stage Johnson decade counter and an output decoder which converts the Johnson binary code to a decimal number. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal.

The decade counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the clock INHIBIT signal is high. A high reset signal clears the decade counter to its zero count. Use of the Johnson decade counter configuration permits high speed operation, 2-input decimal decode gating, and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 10 decoded outputs are normally low and go high only at their respective decimal time slot. Each decoded output remains high for one full clock cycle. A CARRY-OUT (C_{OUT}) signal completes one cycle every 10 clock input cycles and is used to clock the succeeding decade directly in a multi-decade counting chain.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4017A
FUNCTIONAL DIAGRAM

Features:

- **Synchronous decade counter plus 10 decoded outputs**
- **Fully static operation**
- **Medium speed operation...**
  ...5 MHz (typ.) at $V_{DD} - V_{SS}$ = 10 V
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Decade counter/decimal decode display**
- **Frequency division**
- **Counter control/timers**
- **Divide by N counting**
  N = 2 – 10 with one CD4017A and one one CD4001A
  N > 10 with multiple CD4017A's
- **For further application information, see ICAN-6166 "COS/MOS MSI Counter and Register Design & Applications"**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	–65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	–55 to +125°C
PACKAGE TYPE E	–40 to + 85°C
DC SUPPLY-VOLTAGE RANGE (V_{DD})	
(Voltages referenced to V_{SS} Terminal)	–0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to 100°C (PACKAGE TYPES D, F)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

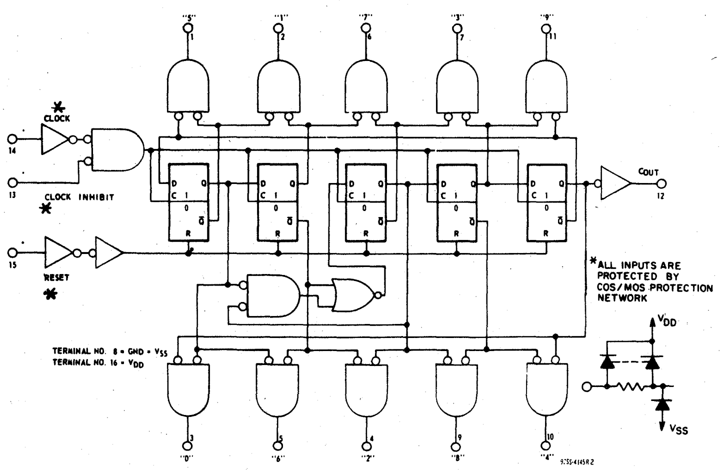


Fig. 1 – Logic diagram.

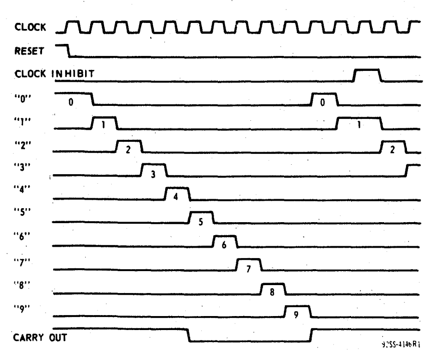


Fig. 2 – Timing diagram.

CD4017A Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, F, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	µA
	–	–	10	10	0.5	10	600	100	1	100	1400	µA
	–	–	15	50	1	50	2000	500	5	500	5000	µA
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								V
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								V
	–	0	10	9.95 Min.; 10 Typ.								V
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								V
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								V
	1	–	10	3 Min.; 4.5 Typ.								V
Noise Margin Inputs Low V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								V
Inputs High, V_{NMH}	0.5	–	5	1 Min.								V
	1	–	10	1 Min.								V
Output Drive Current: N-Channel (Sink)												mA
I_{DN} Min, Decoded Outputs	0.5	–	5	0.06	0.1	0.05	0.035	0.03	0.1	0.025	0.02	mA
	0.5	–	10	0.12	0.4	0.1	0.07	0.085	0.4	0.07	0.055	mA
I_{DN} Min, Carry Output	0.5	–	5	0.185	0.4	0.15	0.105	0.095	0.4	0.08	0.065	mA
	0.5	–	10	0.45	1	0.35	0.25	0.3	1	0.25	0.2	mA
P-Channel (Source)												mA
I_{DP} Min, Decoded Outputs	4.5	–	5	–0.0375	–0.075	–0.03	–0.021	–0.018	–0.075	–0.015	–0.012	mA
	9.5	–	10	–0.12	–0.2	–0.1	–0.07	–0.085	–0.2	–0.07	–0.055	mA
I_{DP} Min, Carry Output	4.5	–	5	–0.185	–0.4	–0.15	–0.105	–0.095	–0.4	–0.08	–0.065	mA
	9.5	–	10	–0.45	–1	–0.35	–0.25	–0.3	–1	–0.24	–0.20	mA
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								µA

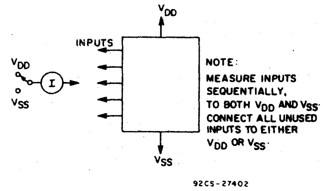


Fig. 10 – Input-leakage-current test circuit.

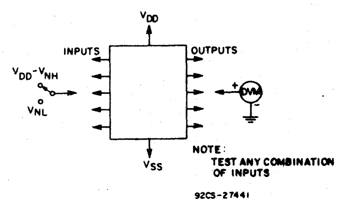


Fig. 11 – Noise-immunity test circuit.

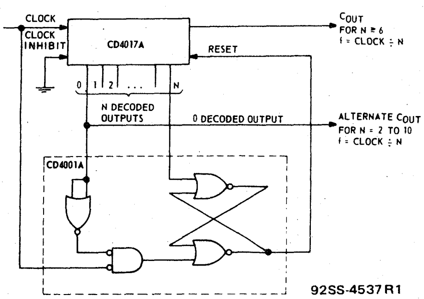


Fig. 12 – Divide by N counter (N ⩽ 10) with N decoded outputs.

When the Nth decoded output is reached (Nth clock pulse) the S-R flip flop (constructed from two NOR gates of the CD4001A) generates a reset pulse which clears the CD4017A to its zero count. At this time, if the Nth decoded output is greater than or equal to 6, the C_{OUT} line goes high to clock the next CD4017A counter section. The "0" decoded output also goes high at this time. Coincidence of the clock low and decoded "0" output low resets the S-R flip flop to enable the CD4017A. If the Nth decoded output is less than 6, the C_{OUT} line will not go high and, therefore, cannot be used. In this case "0" decoded output may be used to perform the clocking function for the next counter.

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted.*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS D, F, H PACKAGES MIN.	MAX.	E PACKAGE MIN.	MAX.	UNITS
Supply Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V
Clock Inhibit Setup Time, t_S	5 10	500 200	– –	700 300	– –	ns
Clock Pulse Width, t_W	5 10	500 170	– –	830 250	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 3	dc dc	0.6 2	MHz
Clock Rise or Fall Time, t_rCL, t_fCL	5 10	– –	15 15	– –	15 15	μs
Reset Pulse Width, t_W	5 10	500 165	– –	830 250	– –	ns
Reset Removal Time	5 10	750 225	– –	1000 275	– –	ns

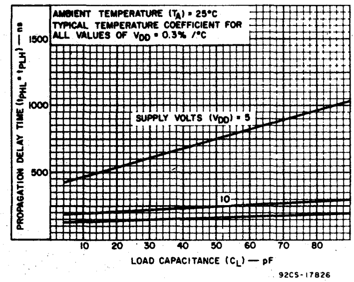


Fig. 3 – Typical propagation delay time vs. C_L for decoded outputs.

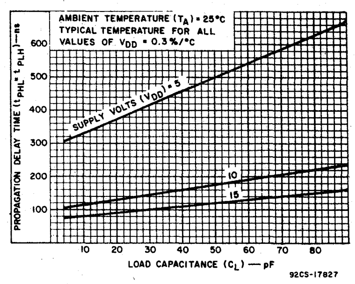


Fig. 4 – Typical propagation delay time vs. C_L for carry output.

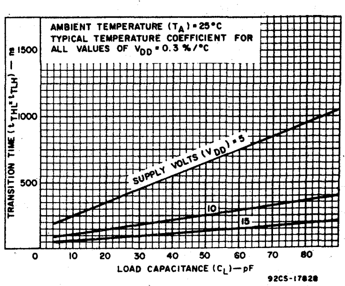


Fig. 5 – Typical transition time vs. C_L for decoded outputs.

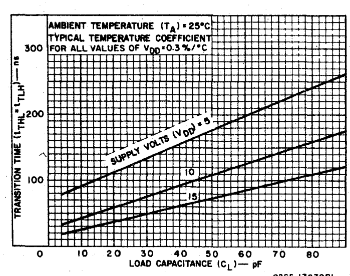


Fig. 6 – Typical transition time vs. C_L for carry output.

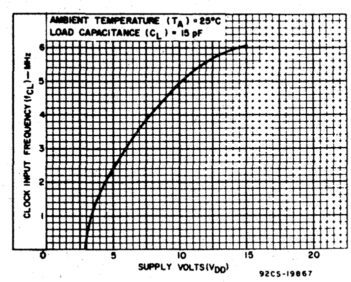


Fig. 7 – Typical clock input frequency vs. V_{DD}.

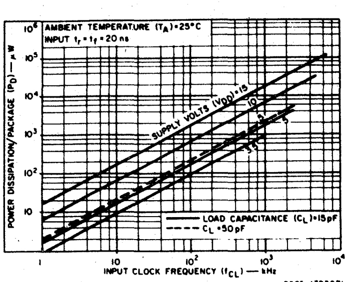
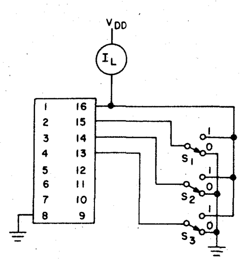


Fig. 8 – Typical dissipation characteristics.



Test performed with the following sequence of "1's and "O's" at each switch.

S_1	S_2	S_3	S_1	S_2	S_3
1	1	1	0	1	0
0	0	0	0	0	0
0	1	0	0	1	0
0	0	0	0	0	0
0	1	0	0	1	0
0	0	0	0	0	0
			0	1	0

Fig. 9 – Quiescent device current test circuit.

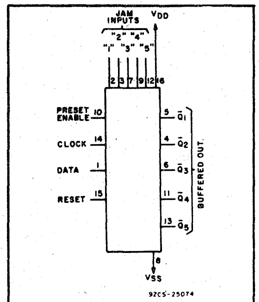
DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D, F, H PACKAGES			E PACKAGE			
		V_{DD} (V)	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
CLOCKED OPERATION									
Propagation Delay Time; t_{PHL} t_{PLH} Carry Out Line		5	–	350	1000	–	350	1300	ns
		10	–	125	250	–	125	300	
Decode Out Lines		5	–	500	1200	–	500	1600	
		10	–	200	400	–	200	500	
Transition Time; t_{THL}, t_{TLH} Carry Out Line		5	–	100	300	–	100	350	ns
		10	–	50	150	–	50	200	
Decode Out Lines		5	–	300	900	–	300	1200	
		10	–	125	350	–	125	450	
Maximum Clock Input Frequency, f_{CL}*		5	1	2.5	–	0.6	2.5	–	MHz
		10	3	5	–	2	5	–	
Minimum Clock Pulse Width, t_W		5	–	200	500	–	200	830	ns
		10	–	100	170	–	100	250	
Clock Rise & Fall Time; t_rCL, t_fCL		5	–	–	15	–	–	15	μs
		10	–	–	15	–	–	15	
Minimum Clock Inhibit Set-Up Time, t_s		5	–	175	500	–	175	700	ns
		10	–	75	200	–	75	300	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
RESET OPERATION									
Propagation Delay Time; t_{PHL} To Carry Out Line		5	–	350	1000	–	350	1300	ns
		10	–	125	250	–	125	300	
To Decode Out Lines		5	–	450	1200	–	450	1600	
		10	–	200	400	–	200	500	
Minimum Reset Pulse Width, t_W		5	–	200	500	–	200	830	ns
		10	–	100	165	–	100	250	
Minimum Reset Removal Time		5	–	300	750	–	300	1000	ns
		10	–	100	225	–	100	275	

*Measured with respect to carry output line

COS/MOS Presettable Divide-By-'N' Counter



CD4018A FUNCTIONAL DIAGRAM

The RCA-CD4018A types consist of 5 Johnson-Counter stages, buffered $\bar{Q}$ outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\bar{Q}5$, $\bar{Q}4$, $\bar{Q}3$, $\bar{Q}2$, $\bar{Q}1$ signals, respectively, back to the DATA input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a CD4011A gate package to properly gate the feedback connection to the DATA input. Divide-by functions greater than 10 can be achieved by use of multiple CD4018A units. The counter is advanced one count at the positive clock-signal transition. A high RESET signal clears the counter to an all-zero condition. A high PRESET-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **Medium speed operation . . . . 5 MHz (typ.) at $V_{DD} - V_{SS}$ = 10 V**
- **Fully static operation**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counters**
- **Fixed and programmable counters greater than 10**
- **Programmable decade counters**
- **Divide-by-"N" counters/frequency synthesizers**
- **Frequency division**
- **Counter control/timers**

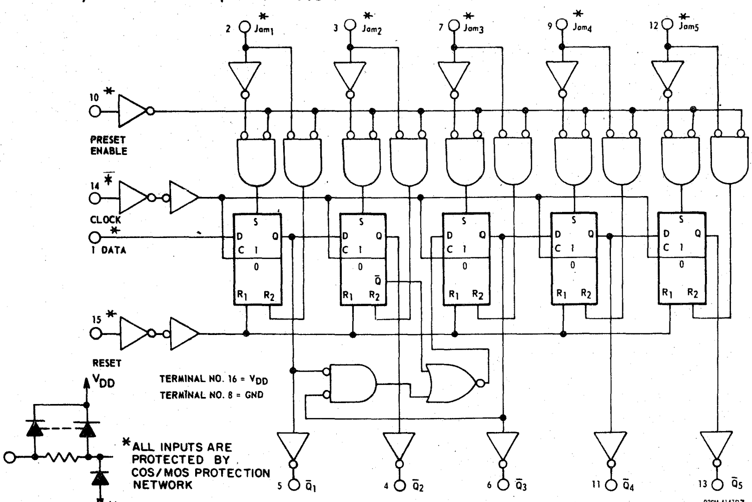


Fig. 1 — Logic diagram.

("DATA" INPUT TIED TO $\bar{Q}_5$ FOR DECADE COUNTER CONFIGURATION)

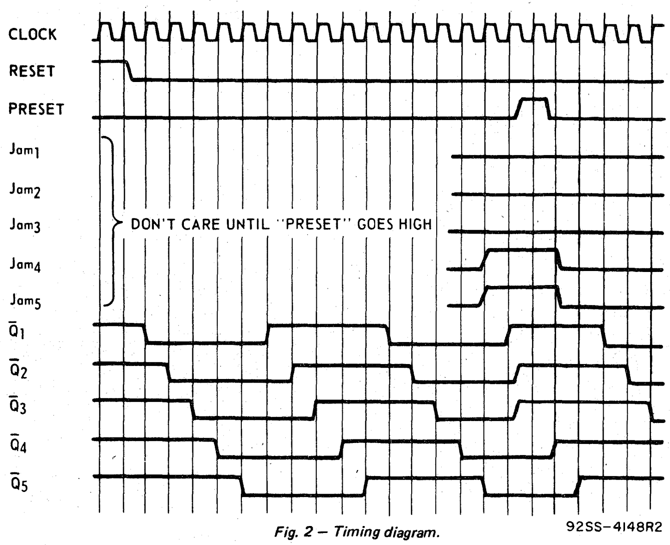


Fig. 2 — Timing diagram.

EXTERNAL CONNECTIONS FOR DIVIDE BY 10, 9, 8, 7, 6, 5, 4, 3 OPERATION

DIVIDE BY 10	$\bar{Q}_5$	CONNECTED BACK TO "DATA"	NO EXTERNAL COMPONENTS REQUIRED
DIVIDE BY 8	$\bar{Q}_4$		
DIVIDE BY 6	$\bar{Q}_3$		
DIVIDE BY 4	$\bar{Q}_2$		
DIVIDE BY 2	$\bar{Q}_1$		

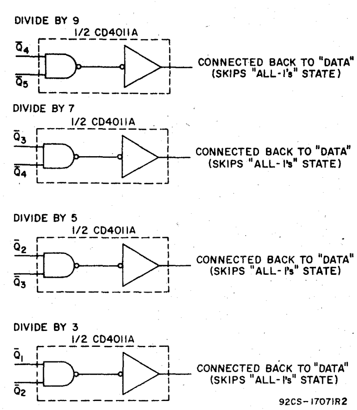


Fig. 3 — External connections for divide by 10, 9, 8, 7, 6, 5, 4, 3, 2 operation.

CD4018A Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS D,F,H Packages Min.	Typ.	Max.	LIMITS E Package Min.	Typ.	Max.	UNITS
CLOCKED OPERATION								
Propagation Delay Time; t_{PLH}, t_{PHL} To $\overline{Q}_5$ Output	5	–	350	1000	–	350	1300	ns
	10	–	125	250	–	125	300	
To Other Outputs	5	–	500	1200	–	500	1600	
	10	–	200	400	–	200	500	
Transition Time; t_{THL}, t_{TLH} To $\overline{Q}_5$ Output	5	–	100	300	–	100	350	ns
	10	–	50	150	–	50	200	
To Other Outputs	5	–	300	900	–	300	1200	ns
	10	–	125	350	–	125	450	
Maximum Clock Input Frequency, f_{CL}	5	1	2.5	–	0.6	2.5	–	MHz
	10	3	5	–	2	5	–	
Min. Clock Pulse Width, t_W	5	–	200	500	–	200	830	ns
	10	–	100	170	–	100	250	
Clock Rise & Fall Time; t_rCL, t_fCL	5	–	–	15	–	–	15	µs
	10	–	–	15	–	–	15	
Min. Data Input Set-Up Time, t_S	5	–	175	500	–	175	700	ns
	10	–	75	200	–	75	300	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF
PRESET* OR RESET OPERATION								
Propagation Delay Time: t_{PLH}, t_{PHL} To $\overline{Q}_5$ Output	5	–	350	1000	–	350	1300	ns
	10	–	125	250	–	125	300	
To Other Outputs	5	–	500	1200	–	500	1600	
	10	–	200	400	–	200	500	
Min. Preset or Reset Pulse Width t_W	5	–	200	500	–	200	830	ns
	10	–	100	165	–	100	250	
Min. Preset or Reset Removal Time	5	–	300	750	–	300	1000	
	10	–	100	225	–	100	275	

* At PRESET ENABLE OR JAM Inputs.

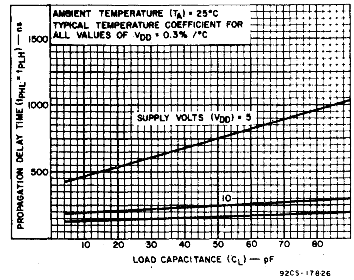


Fig. 4 — Typical propagation delay time vs. load capacitance for decoded outputs.

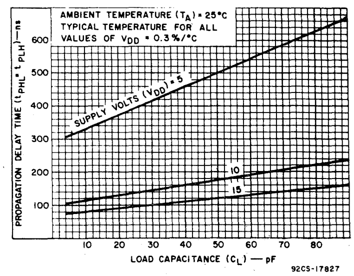


Fig. 5 — Typical propagation delay time vs. load capacitance for $\overline{Q}_5$ output.

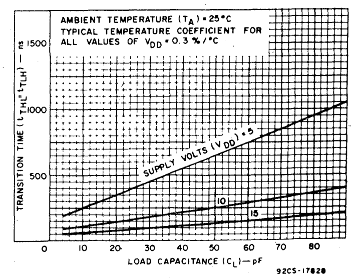


Fig. 6 — Typical transition time vs. load capacitance for decoded outputs.

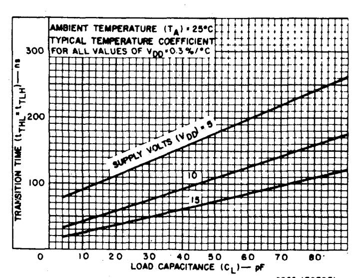


Fig. 7 — Typical transition time vs. load capacitance for $\overline{Q}_5$ output.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,H Packages Min.	Max.	E Package Min.	Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5 10	500 200	– –	700 300	– –	ns
Clock Pulse Width, t_W	5 10	500 170	– –	830 250	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 3	dc dc	0.6 2	MHz
Clock Rise and Fall Time, t_rCL, t_fCL	5 10	– –	15 15	– –	15 15	μs
Preset or Reset Pulse Width, t_W	5 10	500 165	– –	830 250	– –	ns
Preset or Reset Removal Time	5 10	750 225	– –	1000 275	– –	ns

STATIC ELECTRICAL CHARACTERISTICS

Characteristic		Conditions V_O (V)	V_{IN} (V)	V_{DD} (V)	Limits at Indicated Temperatures (°C) D,F,H packages −55	+25 Typ.	+25 Limit	+125	E Package −40	+25 Typ.	+25 Limit	+85	Units
Quiescent Device Current I_L Max.		–	–	5	5	0.3	5	300	50	0.5	50	700	μA
		–	–	10	10	0.5	10	600	100	1	100	1400	
		–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}		–	5	5	0 Typ.; 0.05 Max.								V
		–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}		–	0	5	4.95 Min.; 5 Typ.								
		–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity. Inputs Low, V_{NL}		4.2	–	5	1.5 Min.; 2.25 Typ.								V
		9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}		0.8	–	5	1.5 Min.; 2.25 Typ.								
		1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}		4.5	–	5	1 Min.								V
		9	–	10	1 Min.								
Inputs High, V_{NMH}		0.5	–	5	1 Min.								
		1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) I_{DN} Min.	$\bar{Q}_5$	0.5	–	5	0.18	0.4	0.15	0.105	0.095	0.4	0.08	0.065	mA
		0.5	–	10	0.45	1	0.35	0.25	0.3	1	0.25	0.2	
	$\bar{Q}_1,\bar{Q}_2$	0.5	–	5	0.06	0.1	0.05	0.035	0.03	0.1	0.025	0.02	
	$\bar{Q}_3,\bar{Q}_4$	0.5	–	10	0.25	0.4	0.2	0.14	0.18	0.4	0.15	0.12	
p-Channel (Source) I_{DP} Min.	$\bar{Q}_5$	4.5	–	5	-0.185	-0.4	-0.15	-0.105	-0.095	-0.4	-0.08	-0.065	
		9.5	–	10	-0.45	-1	-0.35	-0.25	-0.3	-1	-0.25	-0.2	
	$\bar{Q}_1,\bar{Q}_2$	4.5	–	5	-0.075	-0.15	-0.06	-0.04	-0.035	-0.15	-0.03	-0.024	
	$\bar{Q}_3,\bar{Q}_4$	9.5	–	10	-0.25	-0.4	-0.2	-0.14	-0.18	-0.4	-0.15	-0.12	
Input Leakage Current, I_{IL}, I_{IH} Max.		Any Input –	–	15	$\pm10^{-5}$ Typ., ±1 Max.								μA

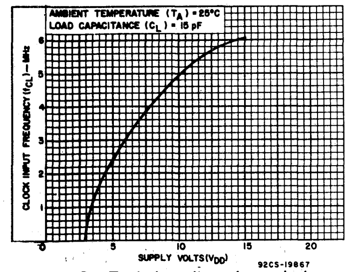


Fig. 8 – Typical maximum input clock frequency vs. supply voltage.

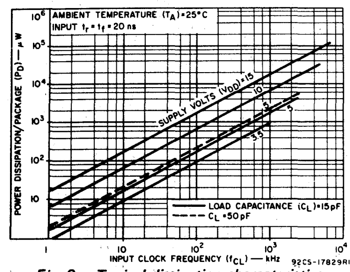


Fig. 9 – Typical dissipation characteristics

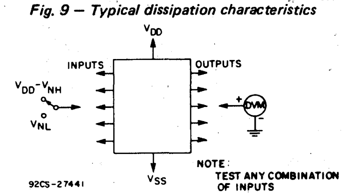
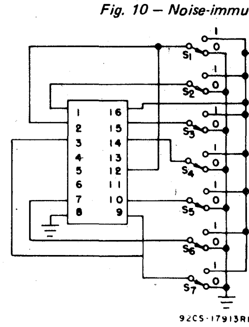


Fig. 10 – Noise-immunity test circuit



Test performed with the following sequence of "1's" and "O's" at each switch.

S_1	S_2	S_3	S_4	S_5	S_6	S_7
0	1	1	0	0	0	0
1	1	1	0	0	1	1
1	0	1	0	1	1	1
0	1	0	0	1	0	0
0	1	0	0	1	0	1
1	0	0	1	1	1	0
0	0	0	1	0	0	0
0	0	0	0	0	0	0
1	0	0	0	1	0	0
0	0	0	0	0	1	0
0	0	0	0	0	0	0

Fig. 11 – Quiescent-device-current test circuit.

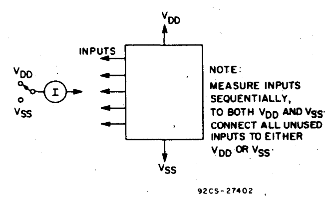


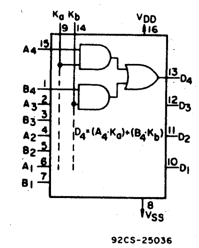
Fig. 12 – Input-leakage-current test circuit.

CD4019A Types

COS/MOS Quad AND/OR Select Gate

The RCA-CD4019A types are comprised of four AND/OR select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_a and K_b. In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical A + B function.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4019A
FUNCTIONAL DIAGRAM

Features:

- **Medium-speed operation .....**
  ... $t_{PHL} = t_{PLH}$ = 50 ns (typ.) at C_L = 15 pF, V_{DD} = 10 V
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **AND-OR select gating**
- **Shift-right/shift-left registers**
- **True/complement selection**
- **AND/OR/Exclusive-OR selection**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) .... –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H .... –55 to +125°C
PACKAGE TYPE E .... –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): .... –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = –40 to +60°C (PACKAGE TYPE E) .... 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) ...... Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F) .... 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) ... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) .... 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS .... –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max .... +265°C

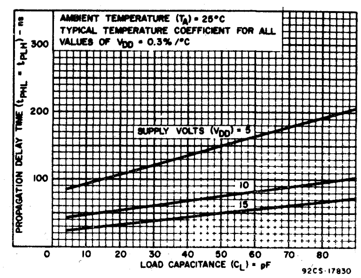


Fig. 2 — Typical propagation delay time vs. load capacitance.

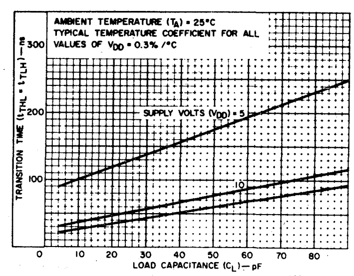


Fig. 3 — Typical transition time vs. load capacitance.

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,H Packages		E Package		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	

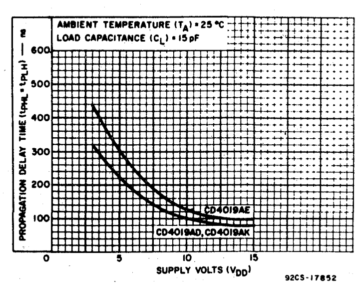


Fig. 4 — Maximum propagation delay time vs. supply voltage.

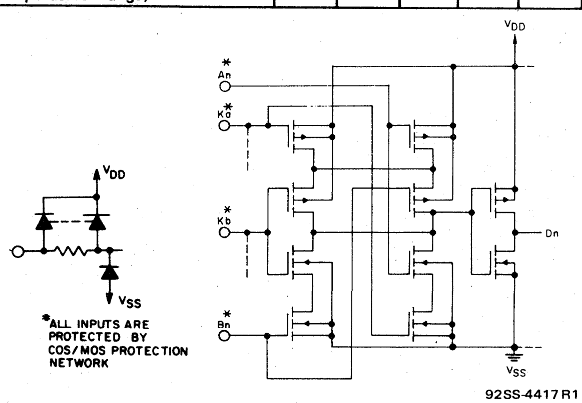


Fig. 1 — Schematic diagram for 1 of 4 identical stages.

STATIC ELECTRICAL CHARACTERISTCS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,F,H Packages				*E Package*				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.03	5	300	50	0.1	50	700	μA
	–	–	10	10	0.05	10	600	100	0.2	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) I_DN Min.	0.5	–	5	0.6	0.9	0.45	0.3	0.37	1	0.3	0.23	mA
	0.5	–	10	0.9	1.5	0.75	0.55	0.8	1.5	0.65	0.5	
p-Channel (Source): I_DP Min.	4.5	–	5	-0.31	-0.5	-0.25	-0.175	-0.145	-0.5	-0.12	-0.095	
	9.5	–	10	-0.95	-1.5	-0.7	-0.5	-0.6	-1.5	-0.5	-0.4	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm10^{-5}$ Typ., ±1 Max.								μA

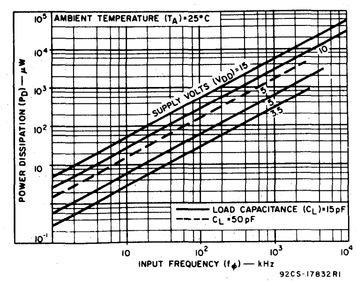


Fig. 5 — Typical dissipation characteristics. (per output).

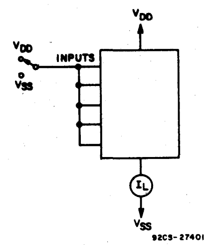


Fig. 6 — Quiescent-device-current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D,F,H Packages			*E Package*			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time; t_{PLH}, t_{PHL}		5	–	100	225	–	100	300	ns
		10	–	50	100	–	50	125	
Transition Time; t_{THL}, t_{TLH}		5	–	100	200	–	100	275	ns
		10	–	40	65	–	40	80	
Average Input Capacitance, C_I	All A and B Inputs		–	5	–	–	5	–	pF
	K_a and K_b Inputs		–	12	–	–	12	–	pF

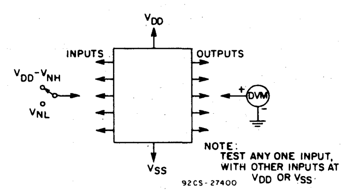


Fig. 7 — Noise-immunity test circuit.

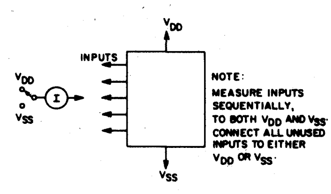
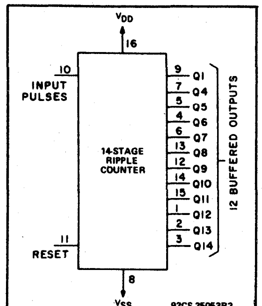


Fig. 8 — Input-leakage-current test circuit.

COS/MOS 14-Stage Ripple-Carry Binary Counter/Divider

The RCA-CD4020 consists of a PULSE INPUT shaping circuit, RESET line driver circuitry, and 14 ripple-carry binary counter stages. Buffered outputs are externally available from stages 1 and 4 through 14. The counter is reset to its all-zeroes state by a high level on the RESET inverter input line. Each counter stage is a static master-slave flip-flop. The counter is advanced one count on the negative-going transition of each INPUT PULSE.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4020A FUNCTIONAL DIAGRAM

Features:
- Medium speed operation . . . 7 MHz (typ.) at $V_{DD}-V_{SS}$ = 10 V
- Low output impedance
- Common reset
- Fully static operation
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:
- Frequency-dividing circuits
- Time-delay circuits
- Counter control
- Counting functions

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,H Packages Min.	Max.	E Package Min.	Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Input Pulse Width, t_W	5	335	–	500	–	ns
	10	125	–	165	–	
Input Pulse Frequency, f_ϕ	5	dc	1.5	dc	1.5	MHz
	10	dc	4	dc	4	
Input Pulse Rise or Fall Time, $t_{r\phi}, t_{f\phi}$	5	–	15	–	15	μs
	10	–	15	–	15	
Reset Pulse Width, t_W	5	2500	–	3000	–	ns
	10	475	–	550	–	

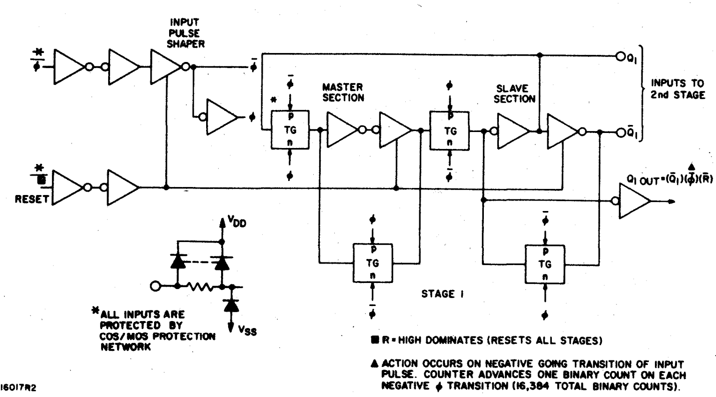


Fig. 1—Logic diagram for 1 of 14 binary stages.

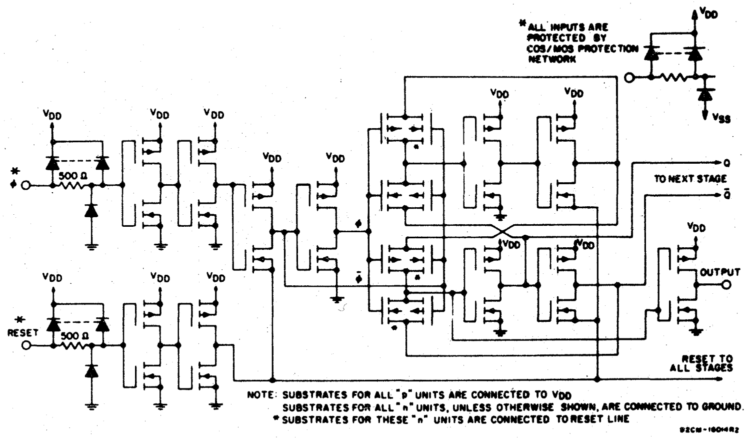


Fig. 2 — Schematic diagram of pulse shapers and 1 of 14 binary stages.

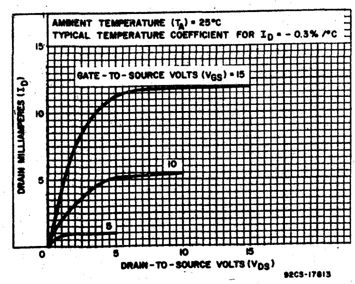


Fig. 3—Typical output n-channel drain characteristics.

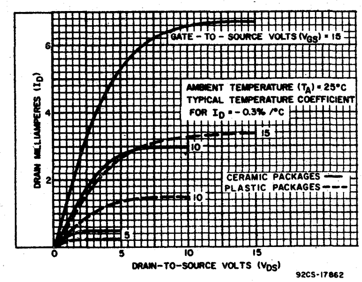


Fig. 4—Minimum output n-channel drain characteristics.

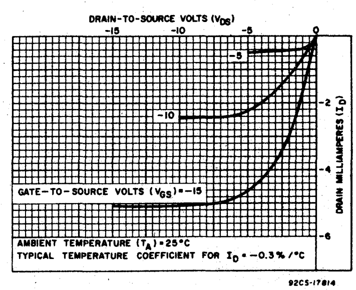


Fig. 5—Typical output p-channel drain characteristics.

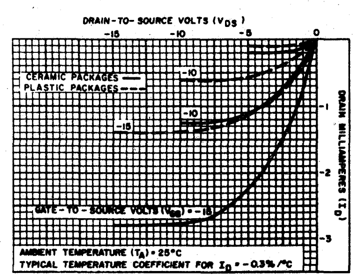


Fig. 6—Minimum output p-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,F,H Packages				*E Package*				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	15	0.5	15	900	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	2.5	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High-Level, V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.5	–	5	0.09	0.2	0.075	0.05	0.09	0.33	0.08	0.065	mA
	0.5	–	10	0.185	0.4	0.15	0.105	0.16	0.5	0.10	0.10	
P-Channel (Source) I_DP Min.	4.5	–	5	−0.11	−0.25	−0.09	−0.065	−0.09	−0.25	−0.06	−0.05	
	9.5	–	10	−0.25	−0.5	−0.20	−0.14	−0.18	−0.5	−0.15	−0.12	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm10^{-5}$ Typ., ±1 Max.								μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r,t_f = 20 ns, C_L = 15 pF, R_L 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS D,F,H Packages Min.	Typ.	Max.	LIMITS E Package Min.	Typ.	Max.	UNITS
Clocked Operation									
Propagation Delay Time,* t_{PLH}, t_{PHL}		5	–	450	600	–	450	650	ns
		10	–	150	225	–	150	250	
Transition Time, t_{THL}, t_{TLH}		5	–	450	600	–	450	650	ns
		10	–	200	300	–	200	350	
Maximum Input Pulse Frequency, f_ϕ		5	1.5	2.5	–	1.5	2.5	–	MHz
		10	4	6	–	4	6	–	
Minimum Input Pulse Width, t_W		5	–	200	335	–	200	500	ns
		10	–	70	125	–	70	165	
Input Pulse Rise & Fall Time, $t_{r\phi}$,$t_{f\phi}$		5	–	–	15	–	–	15	μs
		10	–	–	15	–	–	15	
Average Input Capacitance, C_I	Any Input		–	–	5	–	–	5	pF
Reset Operation									
Propagation Delay Time,* t_{PHL}		5	–	2000	3000	–	2000	3500	ns
		10	–	500	775	–	500	300	
Minimum Reset Pulse Width, t_W		5	–	1800	2500	–	1800	3000	ns
		10	–	300	475	–	300	550	

* Propagation delay is from input pulse to Q_1 output.

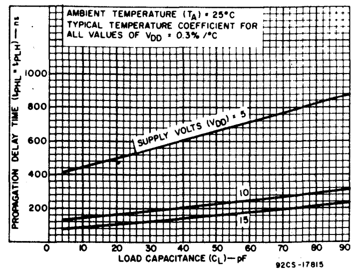


Fig. 7—Typical propagation delay time vs. C_L.

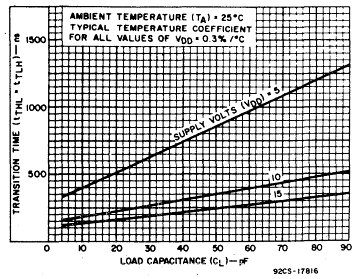


Fig. 8—Typical transition time vs. C_L.

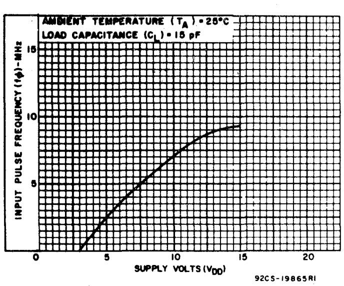


Fig. 9—Typical clock input frequency vs. V_{DD}.

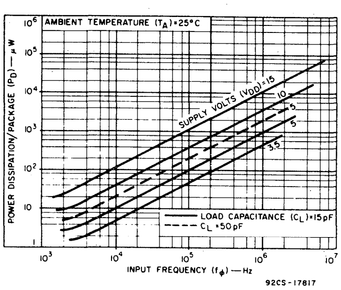


Fig. 10—Typical dissipation characteristics.

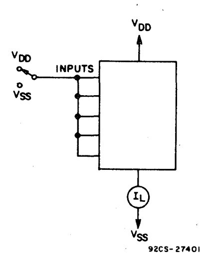


Fig. 11—Quiescent-device-current test circuit.

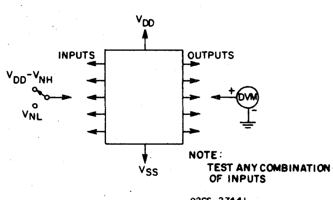


Fig. 12—Noise-immunity test circuit.

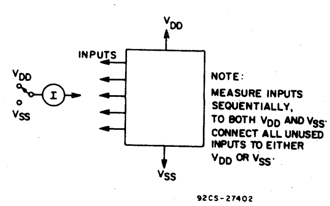


Fig. 13—Input-leakage-current test circuit.

COS/MOS 8-Stage Static Shift Register

Asynchronous Parallel Input/Serial Output,
Synchronous Serial Input/Serial Output

The RCA-CD4021A types are 8-stage parallel or serial-input/serial-output shift registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL DATA input, and individual parallel Jam inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. Q outputs are available from the sixth, seventh, and eighth stages.

When the PARALLEL/SERIAL CONTROL input is low, data are serially shifted into the 8-stage register synchronously with the positive-going transition of the CLOCK pulse.

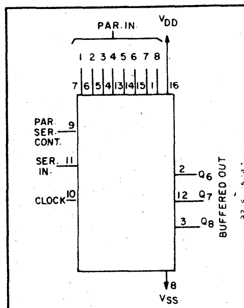
Features:

- **Asynchronous parallel or synchronous serial operation under control of parallel/serial control-input**
- **Individual JAM inputs to each register stage**
- **Master-slave flip-flop register stages**
- **Fully static operation...... DC to 5 MHz**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

When the PARALLEL/SERIAL CONTROL input is high, data are jammed into the 8-stage register via the parallel input lines asynchronously with the clock line.

Register expansion is possible using additional CD4021A packages.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4021A
FUNCTIONAL DIAGRAM

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, F, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current I_L Max.	–	–	5	5	0.5	5	300	50	0.5	50	700	μA
	–	–	10	10	1	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity; Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.5	–	5	0.15	0.3	0.12	0.085	0.072	0.3	0.06	0.05	mA
	0.5	–	10	0.31	0.5	0.25	0.175	0.12	0.5	0.1	0.08	
P-Channel (Source) I_DP Min.	4.5	–	5	-0.1	-0.16	-0.08	-0.055	-0.06	-0.16	-0.05	-0.04	
	9.5	–	10	-0.25	-0.44	-0.20	-0.14	-0.12	-0.44	-0.1	-0.08	
Input Leakage Current, I_{IL}, I_{IH}	Any Input											
	–	–	15	$\pm 10^{-5}$ Typ., ± 1 Max.								

Applications:

- **Parallel to serial data conversion**
- **Asynchronous parallel input/serial output data queueing**
- **General purpose register**

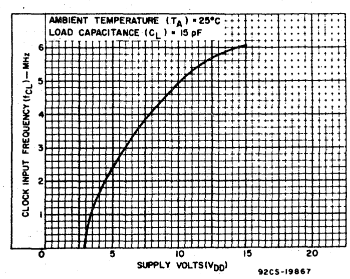


Fig. 1 — Typical clock input frequency vs. supply voltage.

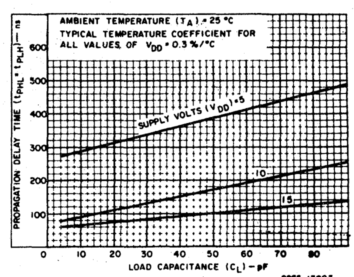


Fig. 2 — Typical propagation delay time vs. load capacitance.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A)
PACKAGE TYPES D, F, H . . . . –55 to +125°C
PACKAGE TYPE E . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = –40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

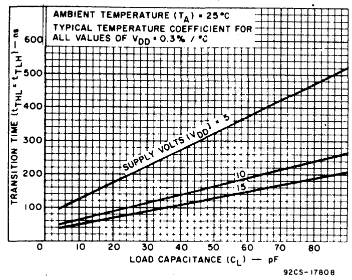


Fig. 3 — Typical transition time vs. load capacitance.

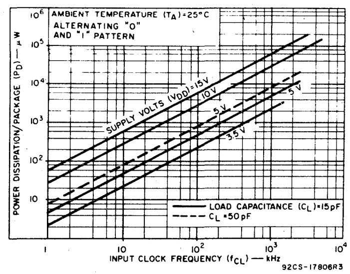


Fig. 4 — Typical dissipation characteristics.

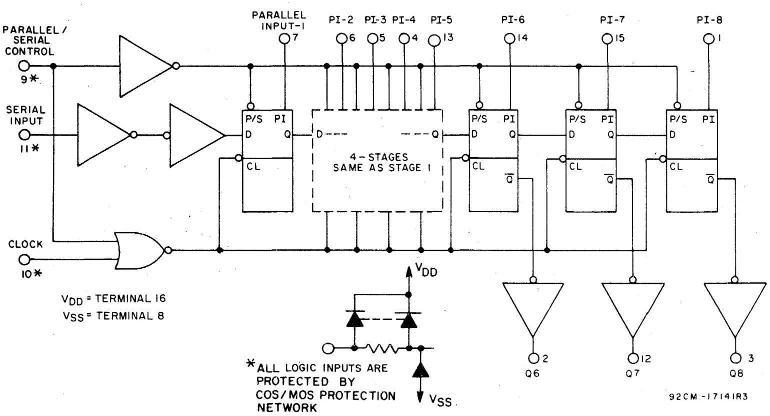


Fig. 5 — Logic diagram.

TRUTH TABLE

CL▲	Serial Input	Parallel/ Serial Control	PI-1	PI-n	Q_1 (Internal)	Q_n
X	X	1	0	0	0	0
X	X	1	0	1	0	1
X	X	1	1	0	1	0
X	X	1	1	1	1	1
_/‾	0	0	X	X	0	Q_{n-1}
_/‾	1	0	X	X	1	Q_{n-1}
‾_	X	0	X	X	Q_1	Q_n

▲ = LEVEL CHANGE X = DON'T CARE CASE
NO CHANGE 92CS-17141R3

Fig. 6 — Truth table.

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:*

CHARACTERISTIC	VDD (V)	LIMITS D, F, H PACKAGES MIN.	LIMITS D, F, H PACKAGES MAX.	LIMITS E PACKAGE MIN.	LIMITS E PACKAGE MAX.	UNITS
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5 10	350 80	– –	500 100	– –	ns
Clock Pulse Width, t_W	5 10	500 175	– –	830 200	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 3	dc dc	0.6 2.5	MHz
Clock Rise and Fall Time, t_rCL, t_fCL*	5 10	– –	15 5	– –	15 5	μs

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

DYNAMIC ELECTRICAL CHARACTERISTICS

at $T_A = 25^oC$, Input t_r, $t_f = 20$ ns, $C_L = 15$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS D, F, H PACKAGES MIN.	TYP.	MAX.	E PACKAGE MIN.	TYP.	MAX.	UNITS
Propagation Delay Time,** t_{PLH}, t_{PHL}	5	–	300	750	–	300	1000	ns
	10	–	100	225	–	300	300	
Transition Time; t_{THL}, t_{TLH}	5	–	150	300	–	150	400	ns
	10	–	75	125	–	75	150	
Maximum Clock Input Frequency, f_{CL}	5	1	2.5	–	0.6	2.5	–	MHz
	10	3	5	–	2.5	5	–	
Minimum Clock Pulse Width, t_W	5	–	200	500	–	200	830	ns
	10	–	100	175	–	100	200	
Clock Rise & Fall Time; t_rCL & t_fCL*	5	–	–	15	–	–	15	µs
	10	–	–	5	–	–	5	
Minimum Data Set Up Time, t_S	5	–	100	350	–	100	500	ns
	10	–	50	80	–	50	100	
Minimum High-Level Parallel/Serial Control Pulse Width t_W	5	–	200	500	–	200	830	ns
	10	–	100	175	–	100	200	
Input Capacitance C_I	Any Input	–	5	–	–	5	–	pF

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

**From Clock or Parallel/Serial Control Input

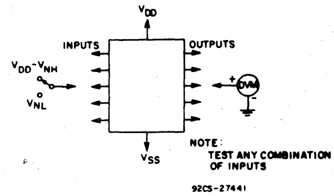


Fig. 7 – Noise-immunity test circuit.

Test performed with the following sequence of "One's" and "Zero's".

S_1	S_2	S_3	S_4	S_5
0	0	1	0	0
1	0	1	1	1
1	0	1	0	1
0	1	1	1	1
0	1	0	0	0

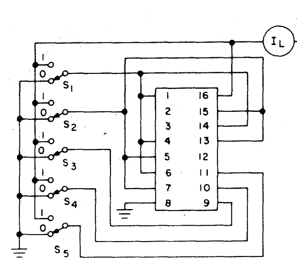


Fig. 8 – Quiescent device current test circuit.

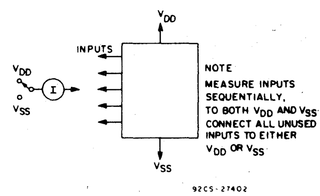


Fig. 9 – Input-leakage-current test circuit.

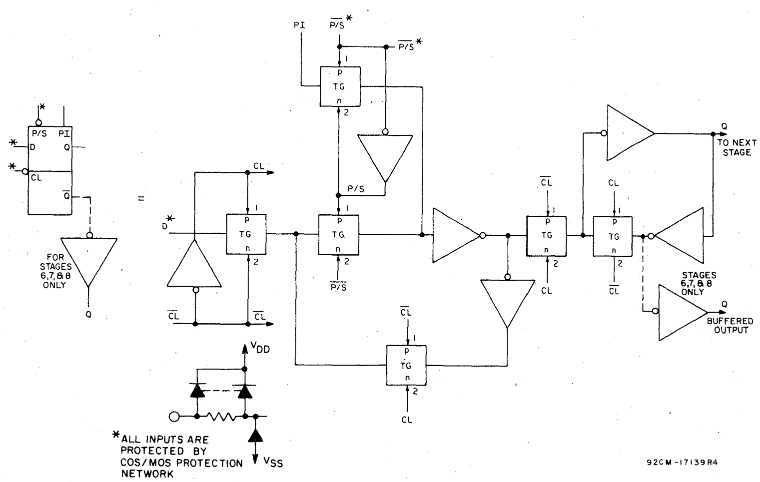


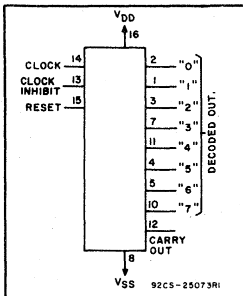
Fig. 10 – One typical stage and its equivalent detailed circuit.

COS/MOS Divide-By-8 Counter/Divider With 8 Decoded Outputs

The RCA-CD4022A types consist of a 4-stage divide-by-8 Johnson counter, associate decode output gating and a CARRY-OUT BIT. The counter is cleared to its zero count by a high RESET signal. The counter is advanced on the positive CLOCK-signal transition provided the CLOCK INHIBIT signal is low.

Use of the Johnson divide-by-8 counter configuration permits high-speed operation, 2-input decode gating, and spike-free decoder outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 8 decode gating outputs are normally low and go high only at their respective decoded time slot. Each decode gate output remains high for one full clock cycle. The CARRY-OUT signal completes one cycle every 8 CLOCK-INPUT cycles and is used as a ripple-carry signal to directly clock a succeeding counter package in a multi-package counting system.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4022A
FUNCTIONAL DIAGRAM

Features:

- **Medium speed operation .... 5 MHz (typ.) at $V_{DD} - V_{SS} = 10$ V**
- **Divide by N counting; N = 2 to 8 with one CD4022A plus one CD4001A package**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

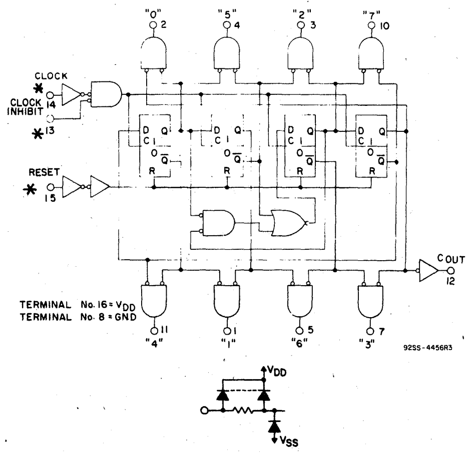
- **Binary counting/decoding**
- **Binary frequency division**
- **Binary counter control/timers**

MAXIMUM RATINGS, ***Absolute-Maximum Values:***

STORAGE-TEMPERATURE RANGE (T_{stg}) .... −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H .... −55 to +125°C
PACKAGE TYPE E .... −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): .... −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = −40 to +60°C (PACKAGE TYPE E) .... 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F) .... 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) .... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) .... 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max .... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	VDD (V)	LIMITS D,F,H Packages Min.	Max.	E Package Min.	Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Clock Inhibit Setup Time, t_S	5 10	175 75	– –	175 75	– –	ns
Clock Pulse Width, t_W	5 10	500 170	– –	830 250	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 3	dc dc	0.6 2	MHz
Clock Rise and Fall Time, t_rCL, t_fCL	5 10	– –	15 15	– –	15 15	μs
Reset Pulse Width	5 10	300 150	– –	600 300	–	ns
Reset Removal Time	5 10	752 225	– –	1000 275	– –	ns



*ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

Fig. 1 – Logic diagram.

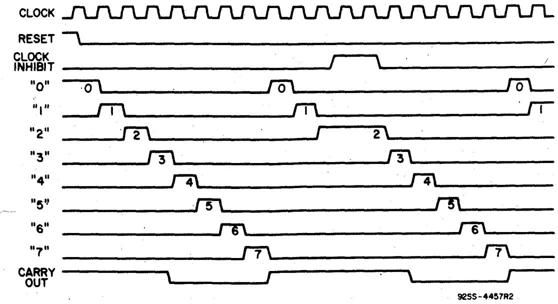


Fig. 2 – Timing diagram.

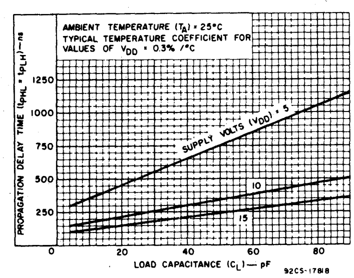


Fig. 3 – Typical propagation delay time vs. load capacitance for decoded outputs.

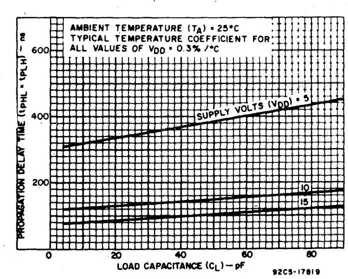


Fig. 4 – Typical propagation delay time vs. load capacitance for carry output.

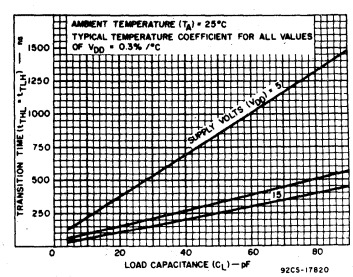


Fig. 5 – Typical transition time vs. load capacitance for decoded outputs.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic		Conditions			Limits at Indicated Temperatures (°C)								Units
					D,F,H Packages				E Package				
		V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.		–	–	5	5	0.3	5	300	50	0.5	50	700	μA
		–	–	10	10	0.5	10	600	100	1	100	1400	
		–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level V_{OL}		–	5	5	0 Typ.; 0.05 Max.								V
		–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}		–	0	5	4.95 Min.; 5 Typ.								
		–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}		4.2	–	5	1.5 Min.; 2.25 Typ.								V
		9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}		0.8	–	5	1.5 Min.; 2.25 Typ.								
		1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}		4.5	–	5	1 Min.								V
		9	–	10	1 Min.								
Inputs High, V_{NMH}		0.5	–	5	1 Min.								
		1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) I_DN Min.	Decoded Outputs	0.5	–	5	0.062	0.15	0.05	0.035	0.03	0.15	0.025	0.02	mA
		0.5	–	10	0.12	0.3	0.1	0.07	0.06	0.3	0.05	0.04	
	Carry Output	0.5	–	5	0.185	0.5	0.15	0.105	0.095	0.5	0.08	0.065	
		0.5	–	10	0.375	1	0.3	0.21	0.155	1	0.13	0.105	
p-Channel (Source): I_DP Min.	Decoded Outputs	4.5	–	5	-0.038	-0.075	-0.03	-0.021	-0.018	-0.075	-0.015	-0.012	
		9.5	–	10	-0.12	-0.15	-0.1	-0.07	-0.06	-0.15	-0.05	-0.04	
	Carry Output	4.5	–	5	-0.185	-0.4	-0.15	-0.105	-0.095	-0.4	-0.08	-0.065	
		9.5	–	10	-0.375	-0.8	-0.3	-0.21	-0.155	-0.8	-0.13	-0.105	
Input Leakage Current, I_{IL}, I_{IH}		Any Input –	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

CD4022A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		D,F,H Packages			E Package			
	V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLOCKED OPERATION								
Propagation Delay Time: t_{PHL}, t_{PLH} Carry-Out Line	5	–	325	1000	–	325	1300	ns
	10	–	125	250	–	125	500	
Decode Out Lines	5	–	400	1200	–	400	1600	ns
	10	–	200	400	–	200	800	
Transition Time: t_{THL}, t_{TLH} Carry-Out Line	5	–	85	300	–	85	340	ns
	10	–	50	100	–	50	200	
Decode-Out Lines	5	–	300	900	–	300	1200	ns
	10	–	125	250	–	125	500	
Min. Clock Pulse Width, t_W	5	–	250	500	–	250	830	ns
	10	–	85	170	–	85	250	
Clock Rise and Fall Time, t_{rCL}, t_{fCL}	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Min. Clock Inhibit Set-Up Time, t_S	5		175	350		175	700	ns
	10		75	150		75	300	
Max. Clock Input Frequency, f_{CL}*	5	1	2.5	–	0.6	2.5	–	MHz
	10	3	5	–	2	5	–	
Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF
RESET OPERATION								
Propagation Delay Time: t_{PHL}, t_{PLH} Carry-Out Line	5	–	300	900	–	300	1200	ns
	10	–	125	250	–	125	500	
Decode-Out Line	5	–	500	1250	–	500	2500	ns
	10	–	200	400	–	200	800	
Min. Reset Pulse Width, t_W	5	–	150	300	–	150	600	ns
	10	–	75	150	–	75	300	
Min. Reset Removal Time	5	–	300	752	–	300	1000	ns
	10	–	100	225	–	100	275	

* Measured with respect to carry output line

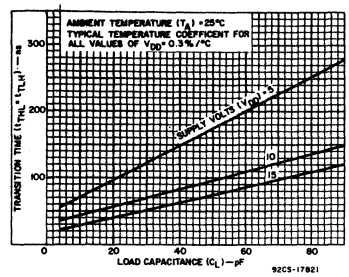


Fig. 6 – Typical transition time vs. load capacitance for carry output.

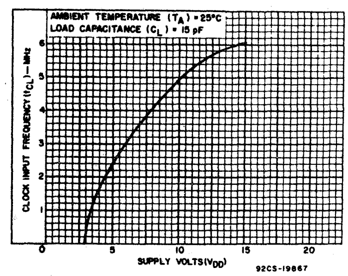


Fig. 7 – Typical clock input frequency vs. supply voltage.

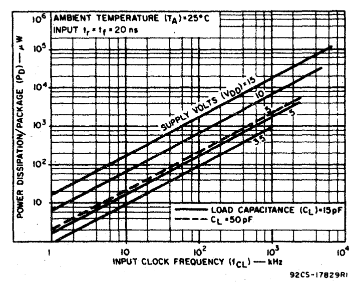


Fig. 8 – Typical dissipation characteristics.

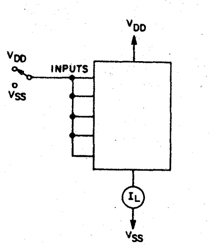


Fig. 9 – Quiescent-device-current test circuit.

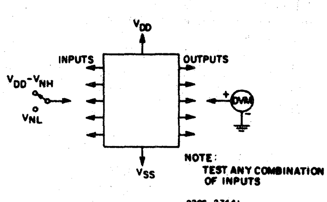


Fig. 10 – Noise-immunity test circuit.

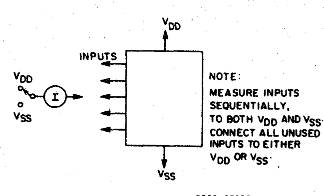


Fig. 11 – Input-leakage-current test circuit.

COS/MOS 7-Stage Binary Counter

With Buffered Reset

The RCA-CD4024A consists of an INPUT PULSE shaping circuit, RESET line driver circuitry, and seven binary counter stages. The counter is reset to "zero" by a high level on the RESET input. Each counter stage is a static master-slave flip-flop. The counter state is advanced one count on the negative-going transition of each INPUT PULSE.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 12-lead hermetic TO-5-style package (T suffix) 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

- **Frequency-dividing circuits**
- **Time-delay circuits**
- **Counter control**
- **D/A counter and switch on one chip**

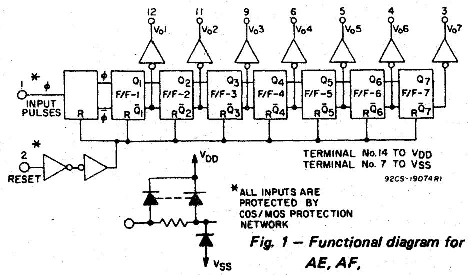
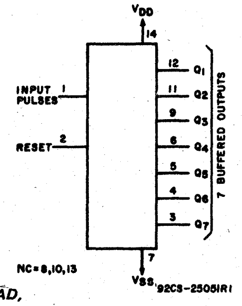


Fig. 1 – Functional diagram for CD4024AD, AE, AF,



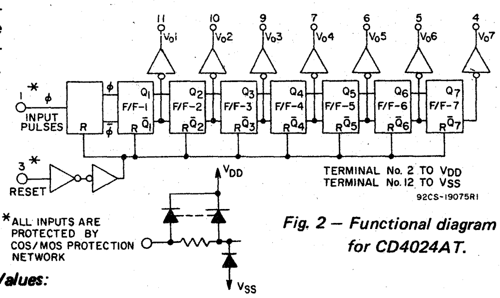
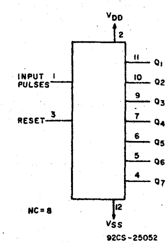


Fig. 2 – Functional diagram for CD4024AT.



MAXIMUM RATINGS, ***Absolute-Maximum Values:***

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES (D,F,T,H) . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D,F,T) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D,F,T) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,T,H Packages Min.	Max.	E Package Min.	Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Clock Pulse Width, t_W	5	330	–	500	–	ns
	10	125	–	165	–	
Clock Input Frequency, f_{CL}	5	dc	1.5	dc	1	MHz
	10	dc	4	dc	3	
Clock Rise or Fall Time, t_rCL, t_fCL	5	15	–	15	–	μs
	10	15	–	15	–	
Reset Pulse Width, t_W	5	500	–	600	–	ns
	10	300	–	350	–	

Features:

- **Medium-speed operation . . . . . . 7-MHz (typ.) input pulse rate at $V_{DD} - V_{SS}$ = 10 V**
- **Low high-and-low level output impedance . . 700Ω and 500Ω (typ.), respectively at $V_{DD} - V_{SS}$ = 10 V**
- **Fully static operation**
- **Common reset**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

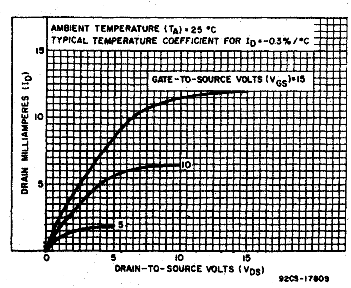
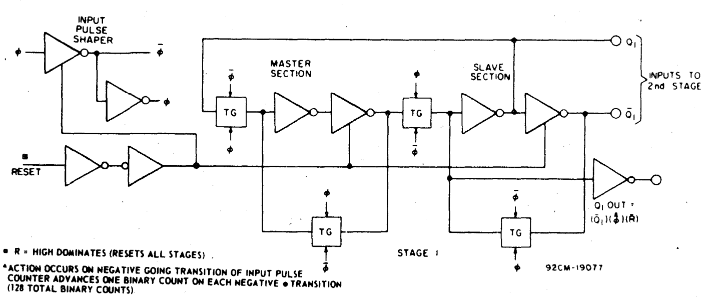


Fig. 3 – Typical output n-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions V_O (V)	V_{IN} (V)	V_{DD} (V)	Limits at Indicated Temperatures (°C) D,F,T,H Packages −55	+25 Typ.	+25 Limit	+125	E Package −40	+25 Typ.	+25 Limit	+85	Units
Quiescent Device Current, I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	μA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink), I_DN Min.	0.5	–	5	0.31	0.5	0.25	0.175	0.15	0.5	0.12	0.095	mA
	0.5	–	10	0.62	1	0.5	0.35	0.31	1	0.25	0.2	
p-Channel (Source) I_DP Min.	4.5	–	5	-0.19	-0.3	-0.15	-0.105	-0.145	-0.3	-0.12	-0.095	
	9.5	–	10	-0.45	-0.7	-0.35	-0.25	-0.31	-0.7	-0.25	-0.2	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm 10^{-5}$ Typ.; ±1 Max.								μA



EQUATIONS FOR STAGES 2 TO 7

$Q_{2OUT} = (\bar{Q}_2)(Q_1)(\overset{\blacktriangle}{\bullet})(R)$ $Q_{5OUT} = (\bar{Q}_5)(Q_1)(Q_2)(Q_3)(Q_4)(\overset{\blacktriangle}{\bullet})(\bar{R})$

$Q_{3OUT} = (\bar{Q}_3)(Q_1)(Q_2)(\overset{\blacktriangle}{\bullet})(\bar{R})$ $Q_{6OUT} = (\bar{Q}_6)(Q_1)(Q_2)(Q_3)(Q_4)(Q_5)(\overset{\blacktriangle}{\bullet})(\bar{R})$

$Q_{4OUT} = (\bar{Q}_4)(Q_1)(Q_2)(Q_3)(\overset{\blacktriangle}{\bullet})(\bar{R})$ $Q_{7OUT} = (\bar{Q}_7)(Q_1)(Q_2)(Q_3)(Q_4)(Q_5)(Q_6)(\overset{\blacktriangle}{\bullet})(\bar{R})$

Fig. 7 — Logic block diagram (pulse shaper and 1 binary stage).

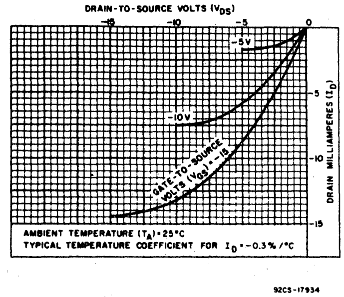


Fig. 4 — Typical output p-channel drain characteristics.

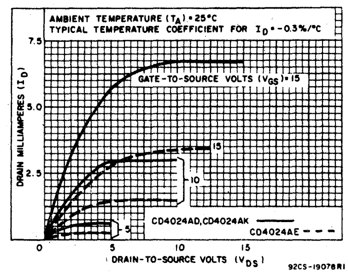


Fig. 5 — Minimum output n-channel drain characteristics.

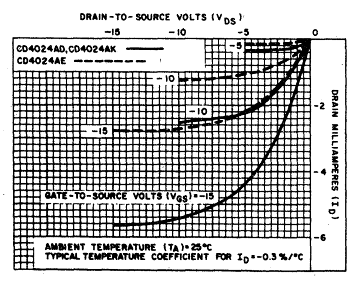


Fig. 6 — Minimum output p-channel drain characteristics.

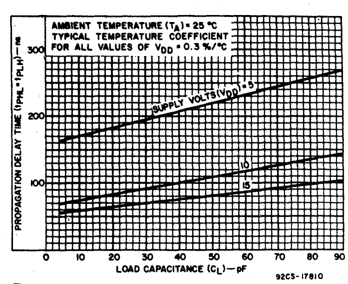


Fig. 8 — Typical propagation delay time vs. C_L.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS D,F,T,H Packages Min.	Typ.	Max.	E Package Min.	Typ.	Max.	UNITS
φ INPUT OPERATION									
Propagation Delay Time;* t_{PLH}, t_{PHL}		5	–	175	350	–	175	400	ns
		10	–	80	125	–	80	150	
Transition Time; t_{THL}, t_{TLH}		5	–	175	225	–	175	250	ns
		10	–	80	125	–	80	150	
Maximum Pulse Input Frequency, f_ϕ		5	1.5	2.5	–	1	2.5	–	MHz
		10	4	7	–	3	7	–	
Minimum Input Pulse Width, t_W		5	–	200	330	–	200	500	ns
		10	–	140	125	–	140	165	
Input Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$		5	–	–	15	–	–	15	μs
		10	–	–	10	–	–	10	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
RESET OPERATION									
Propagation Delay Time; T_{PLH}, T_{PHL}		5	–	500	700	–	500	800	ns
		10	–	250	350	–	250	400	
Minimum Reset Pulse Width; t_W		5	–	375	500	–	375	600	ns
		10	–	200	300	–	200	350	

* Propagation delay time is from input pulse to Q_1 output.

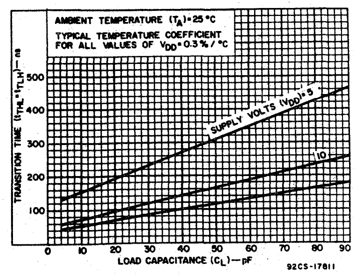


Fig. 9 — Typical transition time vs. C_L.

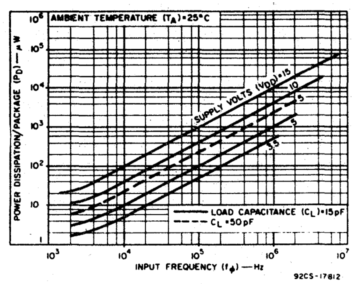


Fig. 10 — Typical dissipation characteristics.

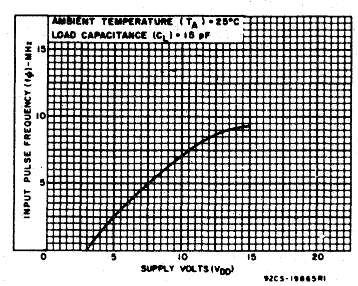


Fig. 11 — Typical input pulse frequency vs. V_{DD}.

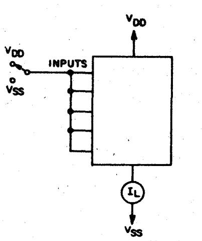


Fig. 12 — Quiescent-device-current test circuit.

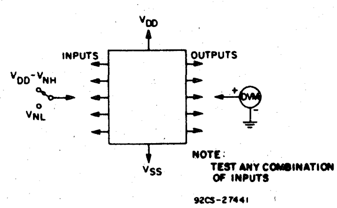


Fig. 13 — Noise-immunity test circuit.

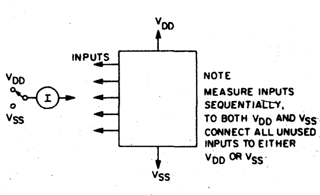


Fig. 14 — Input-leakage-current test circuit.

CD4026A, CD4033A Types

COS/MOS Decade Counters/Dividers

With Decoded 7-Segment Display Outputs and:
Display Enable – CD4026A
Ripple Blanking – CD4033A

The RCA–CD4026A and CD4033A each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving each stage in a numerical display.

These devices are particularly advantageous in display applications where low power dissipation and/or low package count are important.

Inputs common to both types are CLOCK, RESET, & CLOCK INHIBIT; common outputs are CARRY OUT and the seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the CD4026A include DISPLAY ENABLE input and DISPLAY ENABLE and UNGATED "C-SEGMENT" outputs. Signals peculiar to the CD4033 are RIPPLE-BLANKING INPUT and LAMP TEST INPUT and a RIPPLE-BLANKING OUTPUT.

A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transistion if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. The CLOCK INHIBIT signal can be used as a negative-edge clock if the clock line is held high. Antilock gating is provided on the Johnson counter, thus assuring proper counting sequence. The CARRY-OUT (C_{OUT}) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain.

The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven segment display device used for representing the decimal numbers 0 to 9. The 7-segment outputs go high on selection in the CD4033A; in the CD4026A theses outputs go high only when the DISPLAY ENABLE IN is high.

CD4026A

When the DISPLAY ENABLE IN is low the seven decoded outputs are forced low regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The CARRY OUT and UNGATED"C-SEGMENT" signals are not gated by the DISPLAY ENABLE and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

CD4033A

The CD4033A has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.07000 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the CD4033A associated with the most significant digit in the display to a low-level voltage and connecting the RBO terminal of that stage to the RBI terminal of the CD4033A in the next-lower significant position in the display. This procedure is continued for each succeeding CD4033A on the integer side of the display.

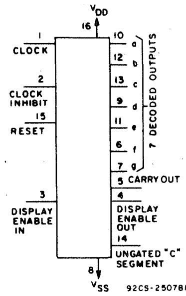
On the fraction side of the display the RBI of the CD4033A associated with the least significant bit is connected to a low level voltage and the RBO of that CD4033A is connected to the RBI terminal of the CD4033A in the next more-significant-bit position. Again, this procedure is continued for all CD4033A's on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high level voltage(instead of to the RBO of the next more-significant-stage). For Example: optional zero → 0.7346.

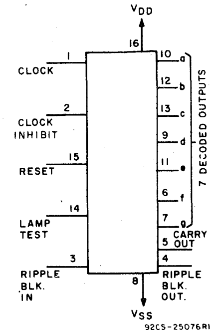
Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the CD4033A associated with it to a high-level voltage.

Ripple blanking of non-significant zeros provides an appreciable savings in display power.

The CD4033A has a LAMP TEST input which, when connected to a high-level voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the high state.



CD4026A



CD4033A

FUNCTIONAL DIAGRAMS

Features:

- **Counter and 7-segment decoding in one package**
- **Easily interfaced with 7-segment display types**
- **Fully static counter operation: DC to 2.5 MHz (typ.)**
- **Ideal for low-power displays**
- **Display Enable Output (CD4026A)**
- **"Ripple Blanking" and Lamp Test (CD4033A)**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 µA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Decade counting/7-segment decimal display**
- **Frequency division/7-segment decimal displays**
- **Clock/watches/timers (e.g. ÷ 60, ÷ 60, ÷ 12 counter/display)**
- **Counter/display driver for meter applications**

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	–65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	–55 to +125°C
PACKAGE TYPE E	–40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal):	–0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)	
FOR T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max	+265°C

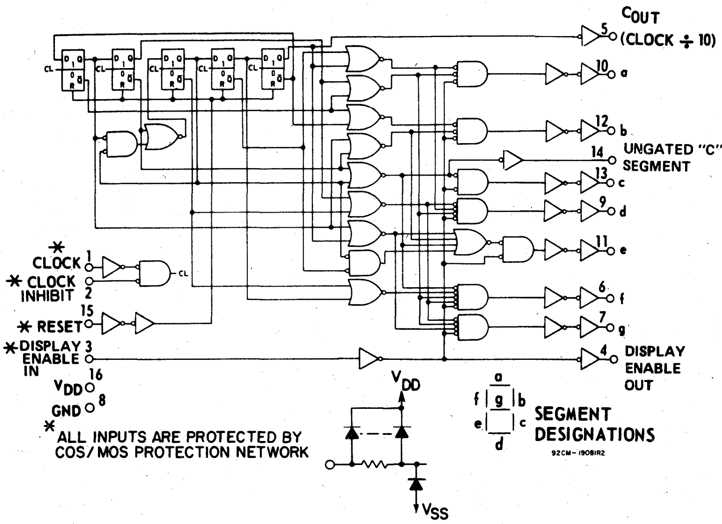


Fig. 1 – CD4026A logic diagram.

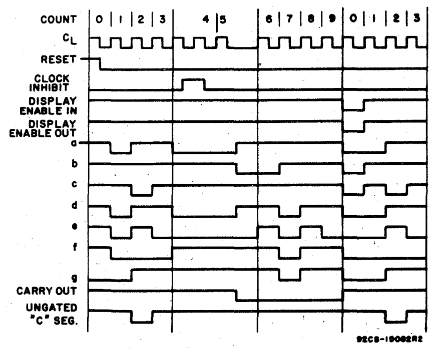


Fig. 2 – CD4026A timing diagram.

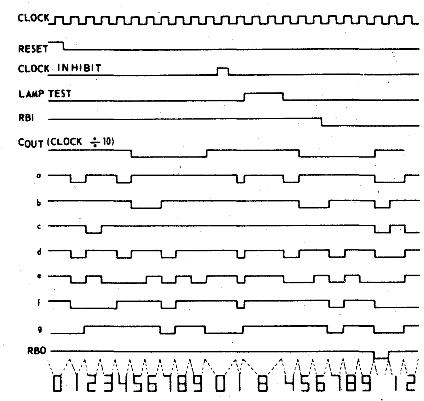


Fig. 4 – CD4033A timing diagram.

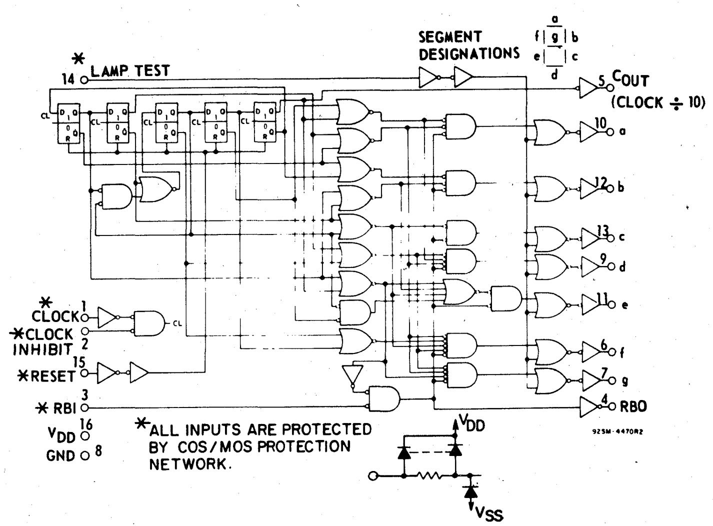


Fig. 3 – CD4033A logic diagram.

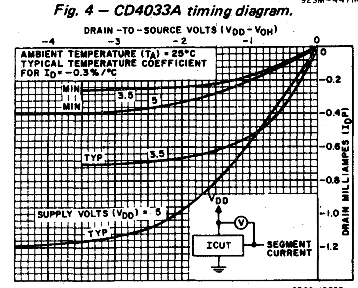


Fig. 5 – Minimum and typical output p-channel decoded drain characteristics @ V_{DD}=3.5 & 5 V.

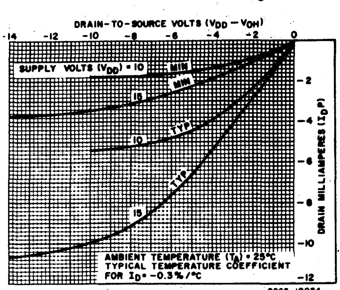


Fig. 6 – Minimum and typical output p-channel decoded drain characteristics @ V_{DD}=10 & 15 V.

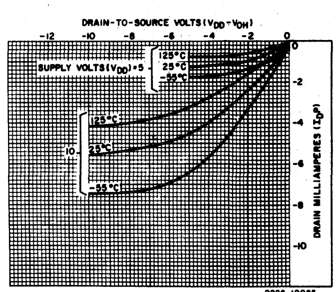


Fig. 7 – Typical output p-channel decoded drain characteristics as a function of temperature.

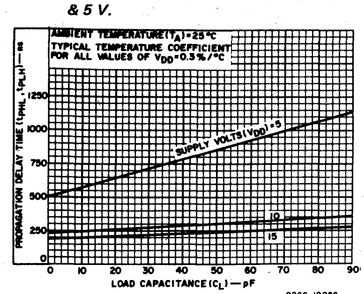


Fig. 8 – Typical propagation delay time vs. C_L for decoded outputs.

CD4026A, CD4033A Types

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,H Packages Min.	LIMITS D,F,H Packages Max.	LIMITS E Package Min.	LIMITS E Package Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Clock Inhibit Setup Time, t_S	5 10	500 200	– –	700 300	– –	ns
Clock Pulse Width, t_W	5 10	330 170	– –	500 250	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1.5 3	dc dc	1 2	MHz
Clock Rise or Fall Time, t_rCL, t_fCL	5 10	– –	15 15	– –	15 15	µs
Reset Pulse Width, t_W	5 10	330 165	– –	550 250	– –	ns
Reset Removal Time	5 10	750 225	– –	1000 275	– –	ns

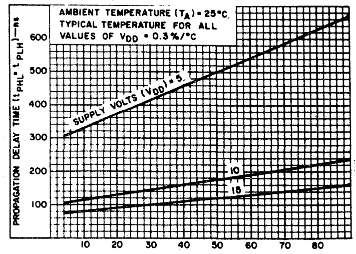


Fig. 9 – Typical propagation delay time vs. C_L for carry outputs.

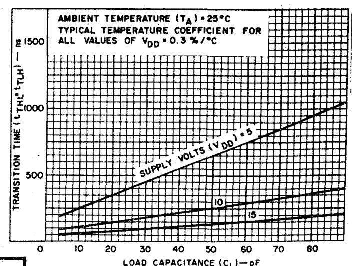


Fig. 10 – Typical transition time vs. C_L for decoded outputs.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions V_O (V)	Conditions V_{IN} (V)	Conditions V_{DD} (V)	D,F,H Packages –55	D,F,H +25 Typ.	D,F,H +25 Limit	D,F,H +125	E Package –40	E +25 Typ.	E +25 Limit	E +85	Units
Quiescent Device Current I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	µA
	–	–	10	10	0.5	10	600	100	1	100	1400	µA
	–	–	15	50	1	50	2000	500	5	500	5000	µA
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								V
High Level, V_{OH}	–	0	5	4.95 Min.; 5 Typ.								V
	–	0	10	9.95 Min.; 10 Typ.								V
Noise Immunity: Inputs Low, V_{NL}		–	5	1.5 Min.; 2.25 Typ.								V
		–	10	3 Min.; 4.5 Typ.								V
Inputs High, V_{NH}		–	5	1.5 Min.; 2.25 Typ.								V
			10	3 Min.; 4.5 Typ.								V
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								V
Inputs High, V_{NMH}	0.5	–	5	1 Min.								V
	1	–	10	1 Min.								V
Output Drive Current n-Channel (Sink), I_DN Min. – Decoded Outputs	0.5	–	5	0.15	0.24	0.12	0.09	0.08	0.24	0.06	0.05	mA
	0.5	–	10	0.32	0.5	0.25	0.18	0.15	0.5	0.12	0.1	mA
Carry Output	0.5	–	5	0.12	0.4	0.15	0.1	0.095	0.4	0.08	0.06	mA
	0.5	–	10	0.45	1	0.35	0.25	0.3	1	0.25	0.2	mA
p-Channel (Source), I_DP Min. – Decoded Outputs	4.5	–	5	-0.21	-0.28	-0.14	-0.1	-0.09	-0.28	-0.07	-0.06	mA
	9.5	–	10	-0.45	-0.6	-0.3	-0.22	-0.2	-0.6	-0.15	-0.13	mA
Carry Output	4.5	–	5	-0.12	-0.4	-0.15	-0.1	-0.095	-0.4	-0.08	-0.06	mA
	9.5	–	10	-0.45	-1	-0.35	-0.25	-0.3	-1	-0.24	-0.2	mA
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm10^{-5}$ Typ., ±1 Max.								µA

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^{\circ}C$, Input t_r, t_f = 20 ns, C_L = 15 pF, $R_L = 200\ k\Omega$

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS D,F,H Packages Min.	Typ.	Max.	LIMITS E Package Min.	Typ.	Max.	UNITS
CLOCKED OPERATION									
Propagation Delay Time; t_{PLH}, t_{PHL} Carry Out Line		5	–	350	1000	–	350	1300	ns
		10	–	125	250	–	125	300	
Decode Out Lines		5	–	600	1700	–	600	2200	ns
		10	–	250	500	–	250	700	
Transition Time; t_{THL}, t_{TLH} Carry Out Line		5	–	100	300	–	100	350	ns
		10	–	50	150	–	50	200	
Decode Out Lines		5	–	300	900	–	300	1200	ns
		10	–	125	350	–	125	450	
Maximum Clock Input Frequency, f_{CL} ▲		5	1.5	2.5	–	1	2.5	–	MHz
		10	3	5	–	2	5	–	
Min. Clock Pulse Width, t_W		5	–	200	330	–	200	500	ns
		10	–	100	170	–	100	250	
Clock Rise & Fall Time; t_rCL, t_fCL		5	–	–	15	–	–	15	µs
		10	–	–	15	–	–	15	
Min. Clock Inhibit Set Up Time, t_S		5	–	175	500	–	175	700	ns
		10	–	75	200	–	75	300	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
RESET OPERATION									
Propagation Delay Time: t_{PLH}, t_{PHL} To Carry Out Line		5	–	350	1000	–	350	1300	ns
		10	–	125	250	–	125	300	
To Decode Out Lines		5	–	550	1400	–	550	1900	ns
		10	–	240	500	–	240	600	
Min. Reset Pulse Width t_W		5	–	200	330	–	200	500	ns
		10	–	100	165	–	100	250	
Min. Reset Removal Time		5	–	300	750	–	300	1000	ns
		10	–	100	225	–	100	275	

▲ Measured with respect to carry out line.

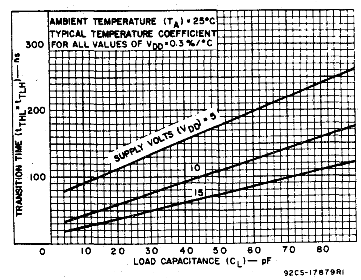


Fig. 11 – Typical transition time vs. C_L for carry output.

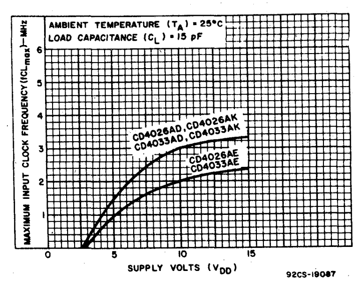


Fig. 12 – Maximum input clock frequency vs. V_{DD}.

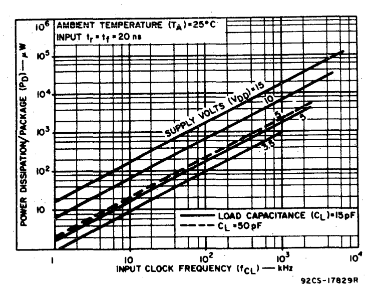


Fig. 13 – Typical dissipation characteristics.

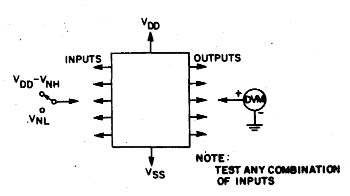


Fig. 14 – Noise immunity test circuit.

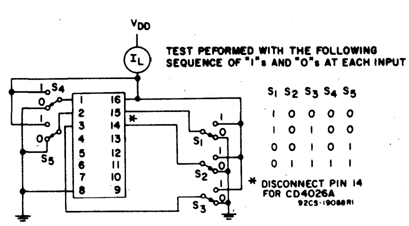


Fig. 15 – Quiescent-device-current test circuit.

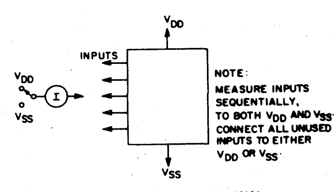


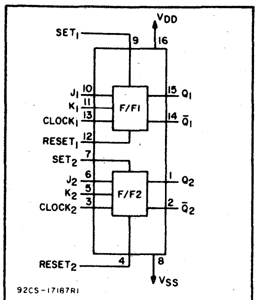
Fig. 16 – Input-leakage-current test circuit.

CD4027A Types

COS/MOS Dual J-K Master-Slave Flip-Flop

The RCA-CD4027A is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset, and Clock input signals. Buffered Q and $\overline{Q}$ signals are provided as outputs. This input-output arrangement provides for compatible operation with the RCA-CD4013A dual D-type flip-flop.

The CD4027A is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.



CD4027A
FUNCTIONAL DIAGRAM

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . -65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . -55 to +125°C
PACKAGE TYPE E . . . . -40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . -0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = -40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = -55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . -0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted.*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD} (V)	LIMITS D, F, H PACKAGES MIN.	LIMITS D, F, H PACKAGES MAX.	LIMITS E PACKAGE MIN.	LIMITS E PACKAGE MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5 10	150 50	– –	200 75	– –	ns
Clock Pulse Width, t_W	5 10	330 110	– –	500 165	– –	ns
Clock Input Frequency (Toggle Mode) f_{CL}	5 10	dc	1.5 4.5	dc	1 3	MHz
Clock Rise or Fall Time, t_rCL,* t_fCL	5 10	– –	15 5	– –	15 5	μs
Set or Reset Pulse Width, t_W	5 10	200 80	– –	300 120	– –	ns

*If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

Features:

- Set-Reset capability
- Static flip-flop operation—retains state indefinitely with clock level either "high" or "low"
- Medium-speed operation—10 MHz (typ.) clock toggle rate at 10V
- Quiescent current specified to 15 V
- Maximum input leakage of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications

- Registers, counters, control circuits

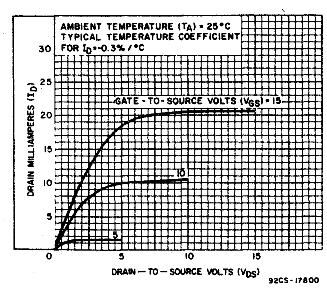
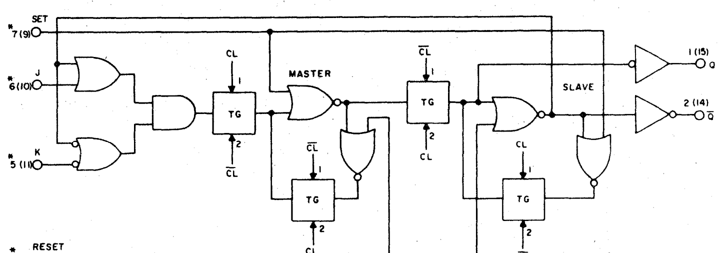
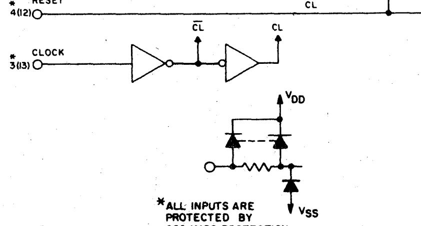


Fig. 1 — Typical n-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, F, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.			5	1	0.005	1	60	10	0.01	10	140	μA
			10	2	0.005	2	120	20	0.05	20	280	
			15	25	0.5	25	1000	250	2.5	250	2500	
Output Voltage: Low Level, V_{OL}	–	0.5	5	0 Typ.; 0.05 Max								V
	–	0.10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0.5	5	5 Typ.; 4.95 Min.								
	–	0.10	10	10 Typ.; 9.95 Min.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	2.25 Typ.; 1.5 Min.								V
	9	–	10	4.5 Typ.; 3 Min.								
Inputs High V_{NH}	0.8	–	5	2.25 Typ.; 1.5 Min.								
	1	–	10	4.5 Typ.; 3 Min.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N Channel (Sink), I_DN Min.	0.5	–	5	0.65	1	0.5	0.35	0.35	1	0.3	0.24	mA
	0.5	–	10	1.25	2.5	1	0.75	0.72	2.5	0.6	0.5	
P-Channel (Source): I_DP Min.	4.5	–	5	-0.31	-0.5	-0.25	-0.175	-0.17	-0.5	-0.14	-0.12	
	9.5	–	10	-0.8	-1.3	-0.65	-0.45	-0.4	-1.3	-0.33	-0.27	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm10^{-5}$ Typ., ±1 Max.								μA





PRESENT STATE					CL	NEXT STATE	
INPUTS				OUTPUT		OUTPUTS	
J	K	S	R	Q		Q	Q̄
1	X	0	0	0	↗	1	0
X	0	0	0	1	↗	1	0
0	X	0	0	0	↗	0	1
X	1	0	0	1	↗	0	1
X	X	0	0	X	↘	NO CHANGE	
X	X	1	0	X	X	1	0
X	X	0	1	X	X	0	1
X	X	1	1	X	X	*	*

LOGIC 1 = HIGH LEVEL
LOGIC 0 = LOW LEVEL
X - DON'T CARE

92CM-17188R4

Fig. 2 — Logic diagram & truth table for CD4027A (one of two identical J-K flip flops).

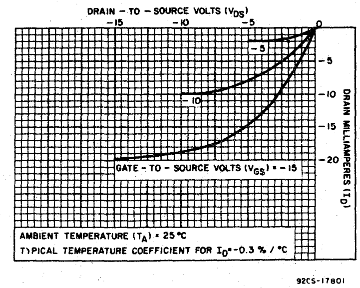


Fig. 3 — Typical p-channel drain characteristics.

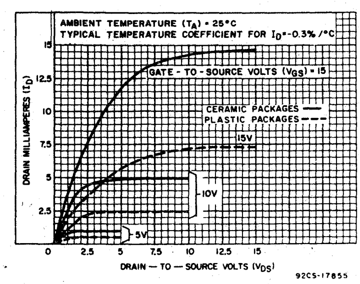


Fig. 4 — Minimum n-channel drain characteristics.

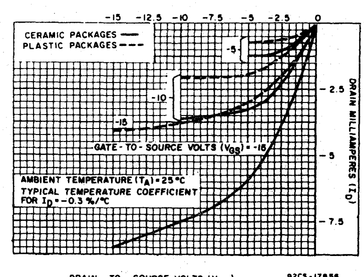


Fig. 5 — Minimum p-channel drain characteristics.

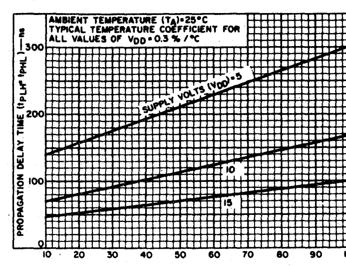


Fig. 6 — Typical propagation delay time vs. C_L.

CD4027A Types

DYNAMIC ELECTRICAL CHARACTERISTICS
at $T_A = 25^\circ C$, Input t_r, $t_f = 20$ ns, $C_L = 15$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS D, F, H PACKAGES MIN.	TYP.	MAX.	E PACKAGE MIN.	TYP.	MAX.	UNITS
Propagation Delay Time: Clock to Q or $\overline{Q}$ Outputs t_{PHL}, t_{PLH}	5	–	200	400	–	150	400	ns
	10	–	100	200	–	75	150	
Set to Q or Reset to $\overline{Q}$, t_{PLH}	5	–	175	225	–	175	350	ns
	10	–	75	110	–	75	150	
Set to $\overline{Q}$ or Reset to Q, t_{PHL}	5	–	175	225	–	175	350	ns
	10	–	75	110	–	75	150	
Transition Time t_{THL}, t_{TLH}	5	–	75	125	–	75	250	ns
	10	–	50	70	–	50	140	
Maximum Clock Input Frequency (Toggle Mode) f_{CL}	5	1.5	3	–	1	3	–	MHz
	10	4.5	8	–	3	8	–	
Minimum Clock Pulse Width, t_W	5	–	165	330	–	165	500	ns
	10	–	65	110	–	65	165	
Minimum Set or Reset Pulse Width, t_W	5	–	125	200	–	125	300	ns
	10	–	50	80	–	50	120	
Minimum Data Setup Time, t_S	5	–	70	150	–	70	200	ns
	10	–	25	50	–	25	75	
Clock Rise or Fall Time, t_{rCL}, t_{fCL}	5	–	–	15	–	–	15	us
	10	–	–	5	–	–	5	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

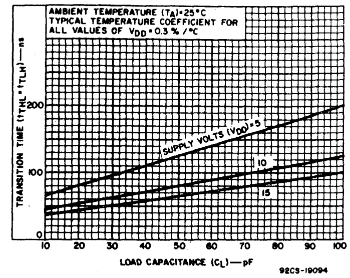


Fig.7 – Typical transition time vs. C_L.

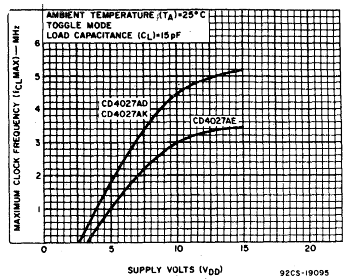


Fig.8 – Typical maximum clock input frequency vs. supply voltage.

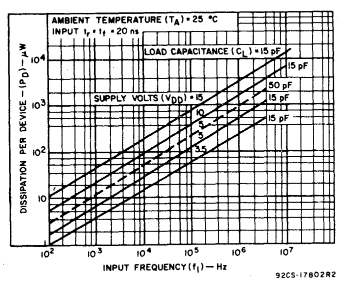


Fig.9 – Typical dissipation characteristics.

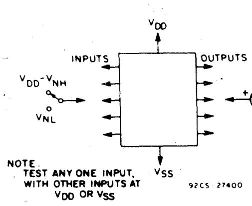


Fig. 10 – Noise immunity test circuit.

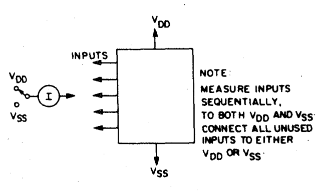


Fig. 11 – Input leakage current test circuit.

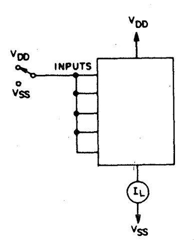
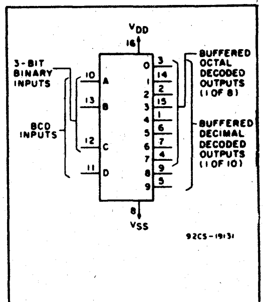


Fig. 12 – Quiescent device current test circuit.

COS/MOS
BCD-to-Decimal Decoder

The RCA-CD4028A types are BCD-to-decimal or binary-to-octal decoders consisting of pulse-shaping circuits on all 4 inputs, decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7. A high-level signal at the D input inhibits octal decoding and causes outputs 0 through 7 to go low. If unused, the D input must be connected to V_{SS}. High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4028A
FUNCTIONAL DIAGRAM

Features:

- **BCD-to-decimal decoding or binary-to-octal decoding**
- **High decoded output drive capability... ...8 mA (typ.) sink or source**
- **"Positive logic" inputs and outputs... ...decoded outputs go high on selection**
- **Medium-speed operation... ...t_{THL}, t_{TLH} = 30 ns (typ.) @ V_{DD} = 10 V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Code conversion**
- **Address decoding—memory selection control**
- **Indicator-tube decoder**

MAXIMUM RATINGS, ***Absolute-Maximum Values:***

STORAGE-TEMPERATURE RANGE (T_{stg}) .... −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H .... −55 to +125°C
PACKAGE TYPE E .... −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages references to V_{SS} Terminal) .... −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = −40 to +60°C (PACKAGE TYPE E) .... 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) ...... Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F) .... 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) ... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) .... 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	VDD (V)	LIMITS				UNITS
		D, F, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V

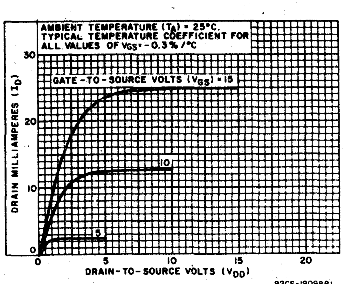


Fig. 1 — Typical output n-channel drain characteristics.

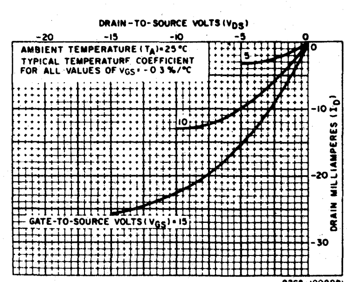


Fig. 2 — Typical output p-channel drain characteristics.

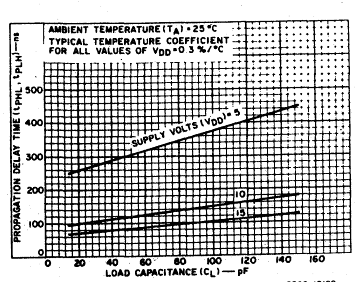


Fig. 3 — Typical propagation delay time vs. C_L.

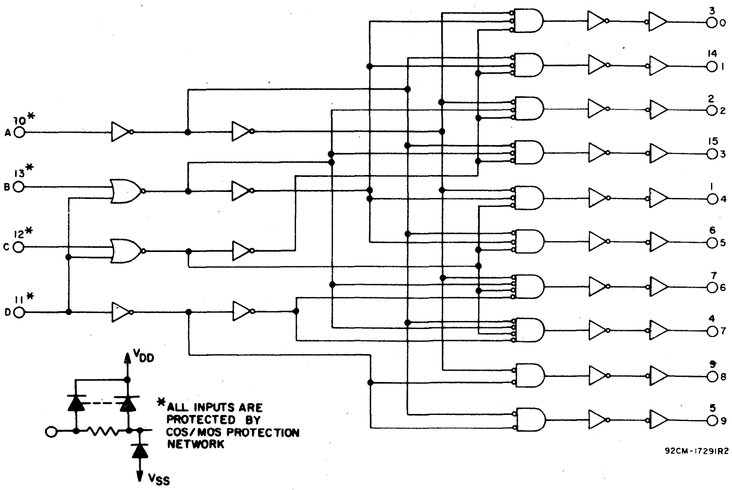


Fig. 4 — Logic diagram.

TABLE I – TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9	
0	0	0	0	1	0	0	0	0	0	0	0	0	0	*
0	0	0	1	0	1	0	0	0	0	0	0	0	0	*
0	0	1	0	0	0	1	0	0	0	0	0	0	0	*
0	0	1	1	0	0	0	1	0	0	0	0	0	0	*
0	1	0	0	0	0	0	0	1	0	0	0	0	0	*
0	1	0	1	0	0	0	0	0	1	0	0	0	0	*
0	1	1	0	0	0	0	0	0	0	1	0	0	0	*
0	1	1	1	0	0	0	0	0	0	0	1	0	0	*
1	0	0	0	0	0	0	0	0	0	0	0	1	0	*
1	0	0	1	0	0	0	0	0	0	0	0	0	1	*
1	0	1	0	0	0	0	0	0	0	0	0	1	0	**
1	0	1	1	0	0	0	0	0	0	0	0	0	1	**
1	1	0	0	0	0	0	0	0	0	0	0	1	0	**
1	1	0	1	0	0	0	0	0	0	0	0	0	1	**
1	1	1	0	0	0	0	0	0	0	0	0	1	0	**
1	1	1	1	0	0	0	0	0	0	0	0	0	1	**

* WHERE 1 = HIGH LEVEL
0 = LOW LEVEL

** EXTRAORDINARY STATES

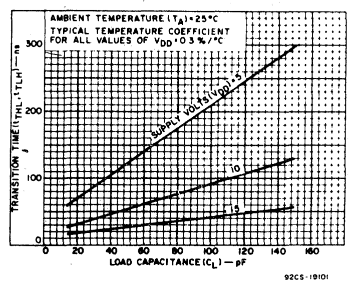


Fig. 5 — Typical transition time vs. C_L.

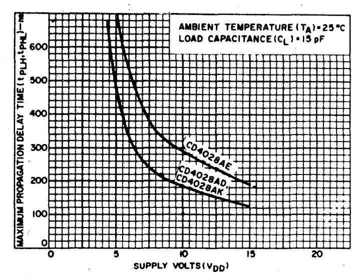


Fig. 6 — Maximum propagation delay time vs. V_{DD}.

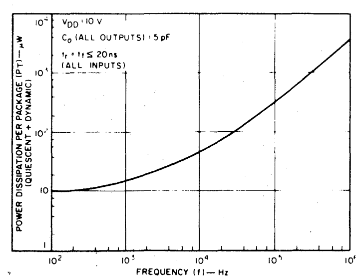


Fig. 7 — Dissipation vs. input frequency.

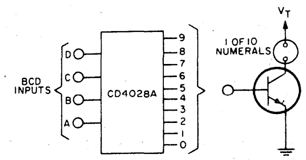
STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, F, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.5	5	300	50	5	50	700	μA
	–	–	10	10	1	10	600	100	10	100	1400	
	–	–	15	50	1	50	2000	500	10	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current N-Channel (Sink), I_{DN} Min.	0.5	–	5	0.75	1.2	0.6	0.45	0.35	1.2	0.3	0.25	mA
	0.5	–	10	1.5	2.4	1.2	0.9	0.7	2.4	0.6	0.5	
P-Channel (Source), I_{DP} Min.	4.5	–	5	-0.7	-0.9	-0.45	-0.32	-0.32	-0.9	-0.22	-0.18	
	9	–	10	-1.4	-1.9	-0.95	-0.65	-0.65	-1.9	-0.48	-0.4	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm10^{-5}$ Typ., ±1 Max.								μA

DYNAMIC ELECTRICAL CHARACTERISTICS

at $T_A = 25^oC$, Input t_r, $t_f = 20\,ns$, $C_L = 15\,pF$, $R_L = 200\,k\Omega$

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D, F, H PACKAGES			E PACKAGE			
		V_{DD} (V)	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Propagation Delay Time; t_{PLH}, t_{PHL}		5	–	250	480	–	250	700	ns
		10	–	100	180	–	100	290	
Transition Time; t_{THL}, t_{TLH}		5	–	60	150	–	60	300	ns
		10	–	30	75	–	30	150	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF



▲ (Trademark) Burroughs Corp. 92CS-17295R1

TUBE REQUIREMENTS

Type	V_T (Vdc)	mA/numeral
Burroughs B4081	170	1.4
B4336/718	170	2
B4032	170	1.4
B4021	120	1.4

TRANSISTOR CHARACTERISTICS
Leakage with transistor cutoff ≤ 0.05mA
$V_{(BR)CEO}$ ≥ 70V

Fig. 9 – Neon readout (Nixie Tube▲) display application.

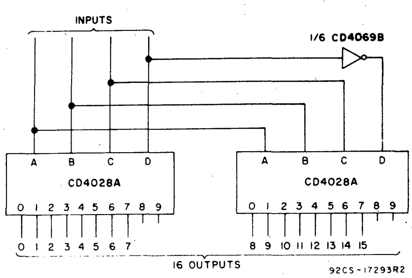


Fig. 8 — Code conversion circuit.

The circuit shown in Fig. 9 converts any 4-bit code to a decimal or hexadecimal code. Table 2 shows a number of codes and the decimal or hexadecimal number in these codes which must be applied to the input terminals of the CD4028A to select a particular output. For example: in order to get a high on output No. 8 the input must be either an 8 expressed in 4-Bit Binary code, a 15 expressed in 4-Bit Gray code, or a 5 expressed in Excess-3 code.

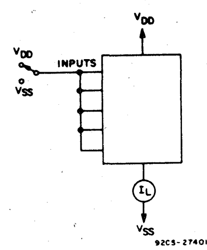


Fig. 10 – Quiescent-device-current test circuit.

TABLE II – CODE CONVERSION CHART

INPUTS D C B A	Hexa-Decimal: 4-BIT BINARY	Hexa-Decimal: 4-BIT GRAY	Decimal: EXCESS-3	Decimal: EXCESS-3 GRAY	Decimal: AIKEN	Decimal: 4-2-2-1	OUTPUT NUMBER 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
0 0 0 0	0	0			0	0	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 1	1	1			1	1	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 1 0	2	3		0	2	2	0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 1 1	3	2	0	3	3		0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
0 1 0 0	4	7	1	4	4		0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0
0 1 0 1	5	6	2			3	0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0
0 1 1 0	6	4	3	1		4	0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0
0 1 1 1	7	5	4	2			0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0
1 0 0 0	8	15	5				0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0
1 0 0 1	9	14	6			5	0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0
1 0 1 0	10	12	7	9		6	0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0
1 0 1 1	11	13	8		5		0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0
1 1 0 0	12	8	9	5	6		0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0
1 1 0 1	13	9		6	7	7	0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0
1 1 1 0	14	11		8	8	8	0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0
1 1 1 1	15	10		7	9	9	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

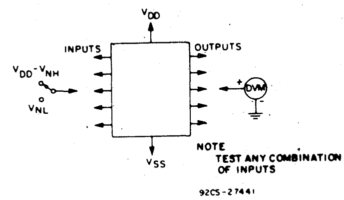


Fig. 11 – Noise-immunity test circuit.

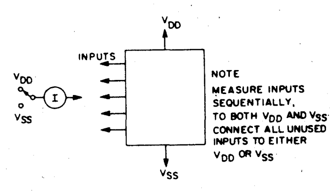


Fig. 12 – Input-leakage-current test circuit.

CD4029A Types

COS/MOS Presettable Up/Down Counter

Binary or BCD-Decade

The RCA-CD4029A consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single CLOCK, CARRY-IN (CLOCK INHIBIT), BINARY/DECADE, UP/DOWN, PRESET ENABLE, and four individual JAM signals and a CARRY OUT signal are provided as outputs.

A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET-ENABLE signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the CARRY-IN and PRESET ENABLE signals are low. Advancement is inhibited when the CARRY-IN or PRESET ENABLE signals are high. The CARRY-OUT signal is normally high and goes low when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the CARRY-IN signal is low. The CARRY-IN signal in the high state can thus be considered a CLOCK INHIBIT. The CARRY-IN terminal must be connected to V_{SS} when not in use.

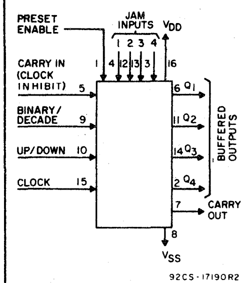
Binary counting is accomplished when the BINARY/DECADE input is high; the counter counts in the decade mode when the BINARY/DECADE input is low. The counter counts Up when the UP/DOWN INPUT is high, and Down when the UP/DOWN INPUT is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement as shown in Fig. 13.

Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:
- Medium speed operation . . . 5 MHz (typ.) @ C_L=15 pF and $V_{DD}-V_{SS}$=10 V
- Multi-package parallel clocking for synchronous high speed output response or ripple clocking for slow clock input rise and fall times
- "Preset Enable" and individual "Jam" inputs provided
- Binary or decade up/down counting
- BCD outputs in decade mode
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:
- Programmable binary and decade counting/frequency synthesizers-BCD output
- Analog to digital and digital to analog conversion
- Up/Down binary counting
- Magnitude and sign generation
- Up/Down decade counting
- Difference counting



CD4029A
Functional Diagram

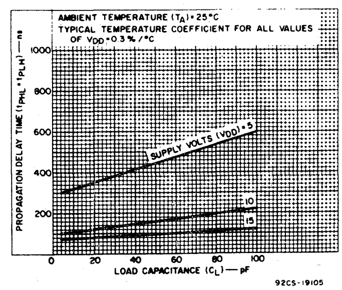


Fig. 1– Typical propagation delay time vs. C_L for Q outputs.

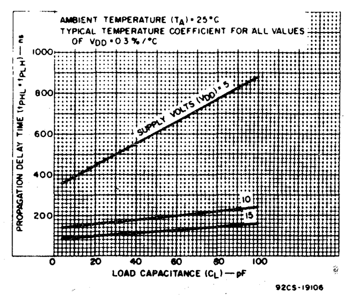


Fig. 2– Typical propagation delay time vs. C_L for carry output.

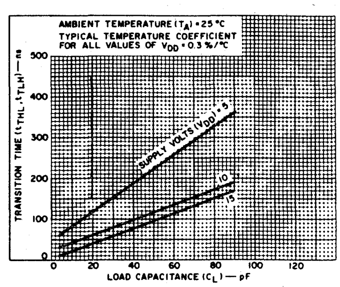


Fig. 3– Typical transition time vs. C_L for Q outputs.

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,H Packages Min.	Max.	E Package Min.	Max.	UNITS
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V
Setup Time, t_S*	5 10	650 230	– –	1300 460	– –	ns
Clock Pulse Width, t_W	5 10	340 170	– –	500 250	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1.5 3	dc dc	1 2	MHz
Clock Rise or Fall Time, t_rCL, t_fCL**	5 10	– –	15 15	– –	15 15	μs
Preset Enable Pulse Width, t_W	5 10	330 160	– –	660 320	– –	ns

*From Up/Down, Binary/Decode, Carry In, or Preset Enable Control Inputs to Clock Edge.
**If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) .... −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
  PACKAGE TYPES D,F,H .... −55 to +125°C
  PACKAGE TYPE E .... −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  (Voltages referenced to V_{SS} Terminal) .... −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
  FOR T_A=−40 to +60°C (PACKAGE TYPE E) .... 500 mW
  FOR T_A=+60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/°C to 200 mW
  FOR T_A=−55 to +100°C (PACKAGE TYPES D,F) .... 500 mW
  FOR T_A=+100 to +125°C (PACKAGE TYPES D,F) .... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
  FOR T_A=FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) .... 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, Input t_r,t_f=20 ns, C_L=15 pF, R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS D,F,H Packages Min.	Typ.	Max.	E Package Min.	Typ.	Max.	UNITS
Clocked Operation								
Propagation Delay Time: t_{PHL}, t_{PLH} Q Outputs	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Carry Output	5	–	425	850	–	425	1700	
	10	–	150	300	–	150	600	
Transition Time: t_{THL}, t_{TLH} Q Outputs	5	–	100	200	–	100	400	ns
	10	–	50	100	–	50	200	
Carry Output	5	–	200	400	–	200	800	
	10	–	100	200	–	100	400	
Minimum Clock Pulse Width, t_W	5	–	200	340	–	200	500	ns
	10	–	100	170	–	100	250	
Clock Rise & Fall Time, t_rCL, t_fCL**	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Minimum Setup Times, t_S*	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Maximum Clock Input Frequency, f_{CL}	5	1.5	2.5	–	1	2.5	–	MHz
	10	3	5	–	2	5	–	
Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF
Preset Enable								
Propagation Delay Time: t_{PHL}, t_{PLH} Q Outputs	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Carry Output	5	–	425	850	–	425	1700	
	10	–	150	300	–	150	600	
Minimum Preset Enable Pulse Width, t_W	5	–	115	330	–	115	660	ns
	10	–	80	160	–	80	320	
Minimum Preset Enable Removal Time	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Carry Input								
Propagation Delay Time: t_{PHL}, t_{PLH} Carry Output	5	–	175	350	–	175	700	ns
	10	–	50	100	–	50	200	

For footnotes, see Recommended Operating Conditions.

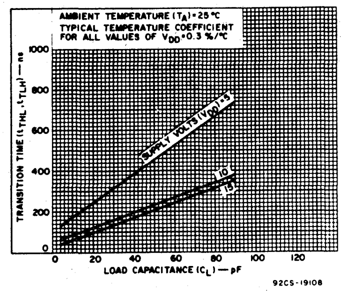


Fig. 4—Typical transition time vs. C_L for carry output.

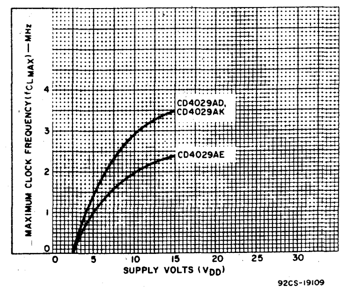


Fig. 5—Maximum clock input frequency vs. V_{DD}.

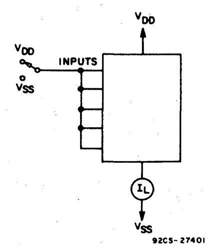


Fig. 6 – Quiescent-device-current test circuit.

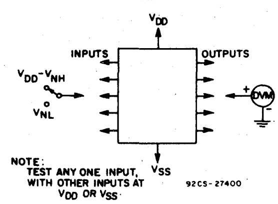


Fig. 7 – Noise-immunity test circuit.

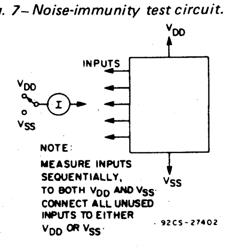


Fig. 8— Input-leakage-current test circuit.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	μA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High-Level, V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.												mA
Q Outputs	0.5	–	5	0.5	0.8	0.4	0.28	0.24	0.8	0.2	0.16	
	0.5	–	10	0.74	1.2	0.6	0.42	0.36	1.2	0.3	0.24	
Carry Output	0.5	–	5	0.1	0.16	0.08	0.06	0.05	0.16	0.04	0.03	
	0.5	–	10	0.4	0.64	0.32	0.22	0.19	0.64	0.16	0.13	
P-Channel (Source), I_DP Min.												
Q Outputs	4.5	–	5	−0.18	−0.24	−0.12	−0.08	−0.07	−0.24	−0.06	−0.05	
	9.5	–	10	−0.3	−0.4	−0.2	−0.14	−0.14	−0.4	−0.1	−0.08	
Carry Output	4.5	–	5	−0.09	−0.12	−0.06	−0.04	−0.04	−0.12	−0.03	−0.02	
	9.5	–	10	−0.15	−0.2	−0.1	−0.07	−0.07	−0.2	−0.05	−0.04	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm10^{-5}$ Typ., ±1 Max.								μA

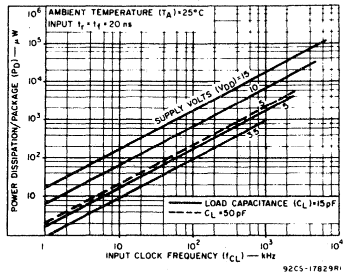


Fig. 9– Typical dissipation characteristics.

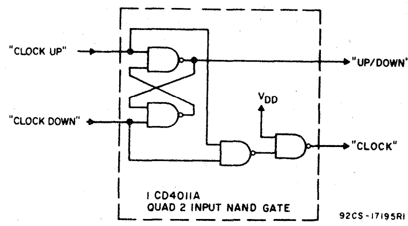
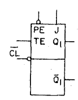


Fig. 10–Conversion of clock up, clock down input signals to clock and up/down input signals.

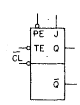
The CD4029A CLOCK and UP/DOWN inputs are used directly in most applications. In applications where CLOCK UP and CLOCK DOWN inputs are provided, conversion to the CD4029A CLOCK and UP/DOWN inputs can easily be realized by use of the circuit shown below.

CD4029A changes count on positive transitions of CLOCK UP or CLOCK DOWN inputs. For the gate configuration shown below, when counting up the CLOCK DOWN input must be maintained high and conversely when counting down the CLOCK UP input must be maintained high.



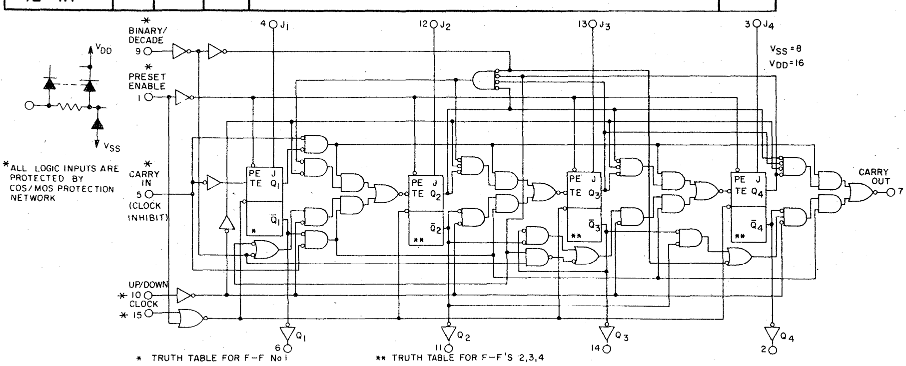
CLOCK	TE	PE	J	Q	$\bar{Q}$
X	X	0	0	0	1
⌐	1	1	X	$\bar{Q}$	Q
X	X	0	1	1	Q
⌐	0	1	X	Q	$\bar{Q}$ NC
⌐	X	1	X	Q	$\bar{Q}$ NC

NC - NO CHANGE TE - TOGGLE ENABLE



CLOCK	TE	PE	J	Q	$\bar{Q}$
X	X	0	0	0	1
⌐	0	1	X	$\bar{Q}$	Q
X	X	0	1	1	0
⌐	1	1	X	Q	$\bar{Q}$ NC
⌐	X	1	X	Q	$\bar{Q}$ NC

X - DON'T CARE



CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC (B/D)	1 0	BINARY COUNT DECADE COUNT
UP/DOWN (U/D)	1 0	UP COUNT DOWN COUNT
PRESET ENABLE (PE)	1 0	JAM IN NO JAM
CARRY IN (CI) (CLOCK INHIBIT)	1 0	NO COUNTER ADVANCE AT POS CLOCK TRANSITION ADVANCE COUNTER AT POS CLOCK TRANSITION

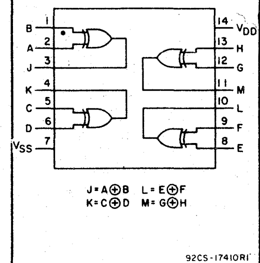
92CL-17191R3

Fig. 11–Logic diagram.

COS/MOS
Quad Exclusive-OR Gate

The RCA-CD4030A types consist of four independent Exclusive-OR gates integrated on a single monolithic silicon chip. Each Exclusive-OR gate consists of four n-channel and four p-channel enhancement-type transistors. All inputs and outputs are protected against electrostatic effects.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).



FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPES D, F, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)	
FOR T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = -55 to +100°C (PACKAGE TYPES D, F)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING) At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max	+265°C

Features:

- **Medium speed operation. . .**
  . . . t_{PHL} = t_{PLH} = 40 ns (typ.) @ C_L = 15 pF and $V_{DD}-V_{SS}$ = 10 V
- **Low output impedance. . .**
  . . . 500 Ω (typ.) @ $V_{DD}-V_{SS}$ = 10 V
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (Full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Even and odd-parity generators and checkers**
- **Logical comparators**
- **Adders/subtractors**
- **General logic functions**

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C,
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS D,F,H Packages Min.	Max.	E Package Min.	Max.	UNITS
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	12	3	12	V

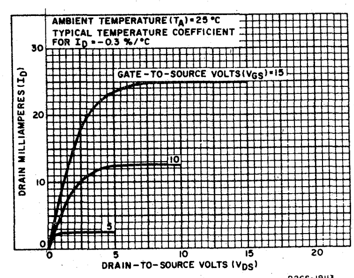
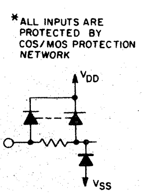
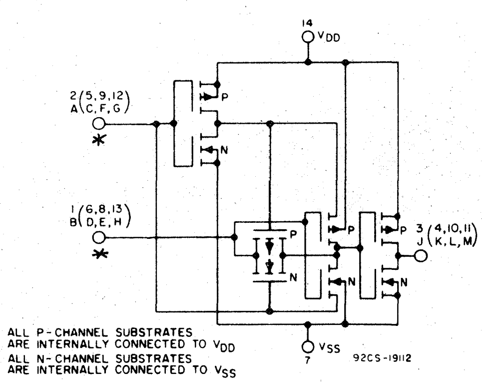


Fig.2 – Typical output n-channel drain characteristics.





TRUTH TABLE FOR ONE OF FOUR IDENTICAL GATES

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

WHERE "1" = HIGH LEVEL
"0" = LOW LEVEL

Fig.1 – Schematic diagram for 1 of 4 identical exclusive-OR gates.

For quiescent device current, noise immunity, and input leakage current test circuits see "Ratings and Characteristics" at the beginning of the COS/MOS section.

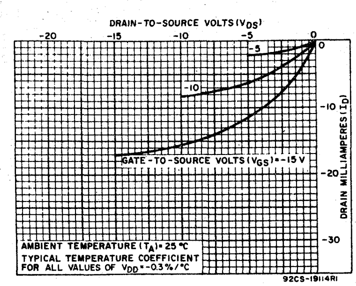


Fig.3 – Typical output p-channel drain characteristics.

CD4030A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	0.5	0.005	0.5	30	5	0.05	5	70	μA
	–	–	10	1	0.01	1	60	10	0.1	10	140	
	–	–	15	25	0.5	25	1000	250	2.5	250	2500	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N Channel (Sink) I_DN Min.	0.5	–	5	0.75	1.2	0.6	0.45	0.35	1.2	0.3	0.25	mA
	0.5	–	10	1.5	2.4	1.2	0.9	0.7	2.4	0.6	0.5	
P Channel (Source): I_DP Min.	4.5	–	5	−0.45	−0.6	−0.3	−0.21	−0.21	−0.6	−0.15	−0.12	
	9.5	–	10	−0.95	−1.3	−0.65	−0.45	−0.45	−1.3	−0.32	−0.25	
Input Leakage Current I_{IL}, I_{IH}	Any Input –	–	15		$\pm 10^{-5}$ Typ., ± 1 Max.							μA

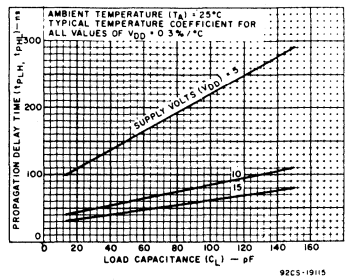


Fig.4 – Typical propagation-delay time vs. load capacitance.

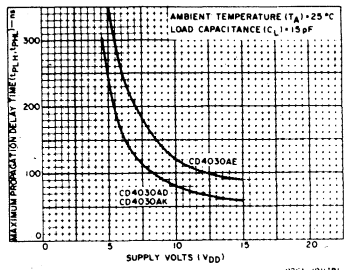


Fig.5 – Maximum propagation-delay time vs. supply voltage.

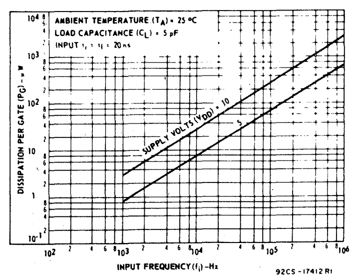


Fig.6 – Typical dynamic power dissipation characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

Characteristic	Test Conditions V_{DD} (V)	LIMITS D,F,H Packages Min.	Typ.	Max.	E Package Min.	Typ.	Max.	Units
Propagation Delay Time: t_{PLH}, t_{PHL}	5	–	100	200	–	100	300	ns
	10	–	40	100	–	40	150	
Transition Time: High-to-Low Level, t_{THL}	5	–	70	150	–	70	300	ns
	10	–	25	75	–	25	150	
Low-to-High Level, t_{TLH}	5	–	80	150	–	80	300	
	10	–	30	75	–	30	150	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

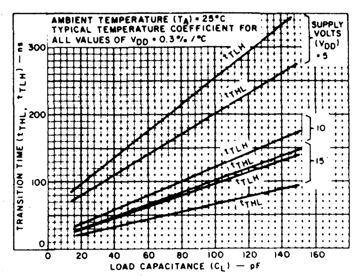


Fig.7 – Typical transition time vs. load capacitance.

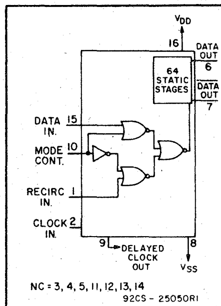
COS/MOS 64-Stage Static Shift Register

The RCA-CD4031A is a 64-stage static shift register in which each stage is a D-type, master-slave flip-flop.

The logic level present at the DATA input is transferred into the first stage and shifted one stage at each positive-going clock transition. Maximum clock frequencies up to 4 Megahertz (typical) can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the low or high state. The CD4031A has a MODE CONTROL input that, when in the high state, allows operation in the recirculating mode. Register packages can be cascaded and the clock lines driven directly for high speed operation. Alternatively, a delayed clock output (CL_D) is provided that enables cascading register packages while allowing reduced clock drive fan-out and rise- and fall-time requirements.

Data (Q) and $\overline{\text{Data}}$ ($\overline{Q}$) outputs are provided from the 64th register stage. The Data (Q) output is capable of drving one TTL or DTL load.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package, (K suffix), and in chip form (H suffix).



CD4031A
FUNCTIONAL DIAGRAM

Features:

- **Fully static operation: DC to 4 MHz typ. @ $V_{DD} - V_{SS}$ = 10 V**
- **Operation from a single 3 to 15 V positive or negative power supply**
- **High noise immunity**
- **Microwatt quiescent power dissipation: 10 μW (typ.) for ceramic packages; 100 μW (typ.) for plastic packages**
- **Single phase clocking requirements**
- **Recirculation capability**
- **Data compatible with TTL-DTL**
- **Two cascading modes:**
  Direct clocking for high-speed operation
  Delayed clocking for reduced clock drive requirements
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Serial shift registers**
- **Time delay circuits**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) .... -65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H .... -55 to +125°C
PACKAGE TYPE E .... -40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal): .... -0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = -55 to +100°C (PACKAGE TYPES D, F) .... 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) ... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS .... -0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Hold Time, t_H	5	100	–	100	–	ns
	10	200	–	200	–	
Clock Pulse Width, t_W	5	2.5	–	2.6	–	μs
	10	1	–	1.3	–	
Clock Input Frequency, f_{CL}	5	dc	0.8	dc	0.4	MHz
	10	dc	2	dc	1	
Clock Rise and Fall Time, t_rCL, t_fCL*	5	–	2	–	2	μs
	10	–	1	–	1	

* If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 15 pF and the transition time of the output driving stage.

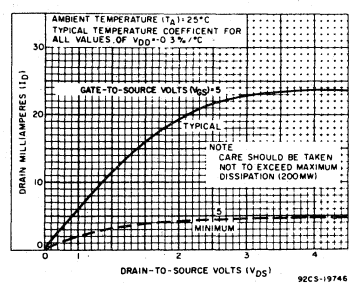


Fig. 1 — Typical and minimum output n-channel drain characteristics for Q output.

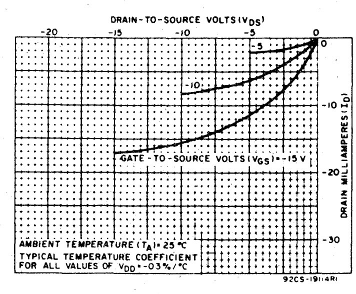
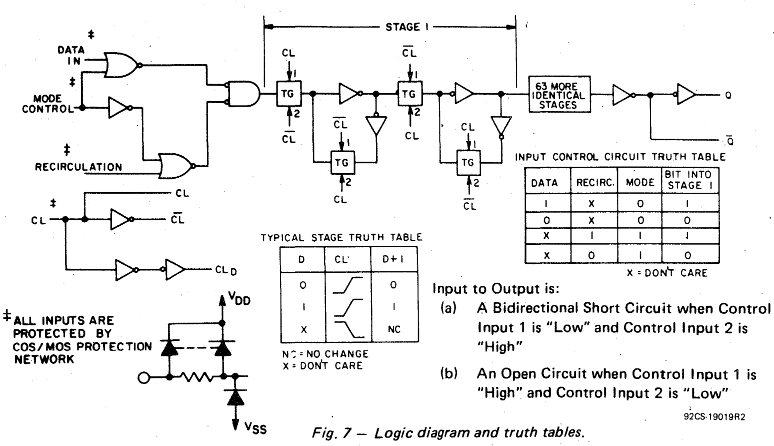


Fig. 2 — Typical output p-channel drain characteristics for Q output.

CD4031A Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) D, F, H PACKAGES -55	+25 TYP.	+25 LIMIT	+125	E PACKAGE -40	+25 TYP.	+25 LIMIT	+85	UNITS
Quiescent Device Current, I_L Max.	–	–	5	10	0.5	10	600	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max								V
	–	10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), $I_D N$ Min. Q	0.4	–	4.5	1.6	2.6	1.3	0.91	1.6	2.6	1.3	1.05	mA
Q	0.5	–	10	5	8	4	3.2	5	8	4	3.2	
Q̄	0.5	–	5	0.11	0.18	0.09	0.06	0.05	0.18	0.045	0.037	
Q̄	0.5	–	10	0.24	0.4	0.2	0.14	0.12	0.4	0.1	0.08	
CL_D	0.5	–	5	0.48	0.8	0.4	0.28	0.24	0.8	0.2	0.16	
CL_D	0.5	–	10	1.5	2.4	1.2	0.84	0.75	2.4	0.6	0.5	
P-Channel (Source): $I_D P$ Min. Q	4.5	–	5	-0.4	-0.64	-0.32	-0.22	-0.20	-0.64	-0.16	-0.13	
Q	9.5	–	10	-0.85	-1.4	-0.70	-0.49	-0.42	-1.4	-0.35	-0.29	
Q̄	4.5	–	5	-0.11	-0.18	-0.09	-0.06	-0.05	-0.18	-0.045	-0.037	
Q̄	9.5	–	10	-0.24	-0.4	-0.20	-0.14	-0.12	-0.4	-0.10	-0.08	
CL_D	4.5	–	5	-0.48	-0.8	-0.40	-0.28	-0.24	-0.8	-0.20	-0.16	
CL_D	9.5	–	10	-1	-1.6	-0.80	-0.56	-0.5	-1.6	-0.40	-0.32	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA



INPUT CONTROL CIRCUIT TRUTH TABLE

DATA	RECIRC.	MODE	BIT INTO STAGE 1
1	X	0	1
0	X	0	0
X	1	1	1
X	0	1	0

X = DON'T CARE

TYPICAL STAGE TRUTH TABLE

D	CL	D+1
0	⌐ (rising)	0
1	⌐ (rising)	1
X	¬ (falling)	NC

NC = NO CHANGE
X = DON'T CARE

‡ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

Input to Output is:
(a) A Bidirectional Short Circuit when Control Input 1 is "Low" and Control Input 2 is "High"
(b) An Open Circuit when Control Input 1 is "High" and Control Input 2 is "Low"

92CS-19019R2

Fig. 7 – Logic diagram and truth tables.

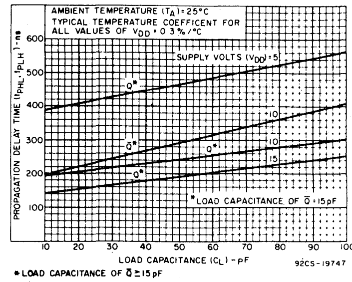


Fig. 3 – Typical propagation delay time vs. load capacitance for data outputs.

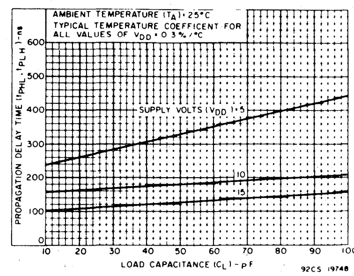


Fig. 4 – Typical propagation delay vs. load capacitance for delayed clock output.

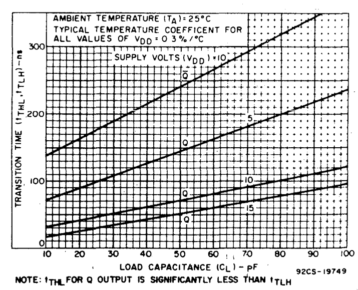


Fig. 5 – Typical transition time vs. load capacitance for data outputs.

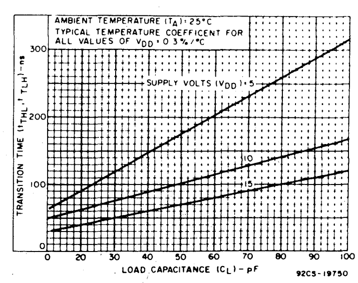


Fig. 6 – Typical transition time vs. load capacitance for delayed clock output.

DYNAMIC ELECTRICAL CHARACTERISTICS

at T_A=25°C, Input t_r,t_f=20 ns, C_L=15 pF (unless otherwise specified), R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS D, F, H MIN.	D, F, H TYP.	D, F, H MAX.	E MIN.	E TYP.	E MAX.	UNITS
Propagation Delay Time; t_{PLH}, t_{PHL} Clock to Data Output Q & $\overline{Q}$ *		5	–	400	800	–	400	1600	ns
		10	–	200	400	–	200	800	
Clock to CL_D	C_L = 60 pF	5	–	400	800	–	400	1600	
		10	–	200	400	–	200	800	
Transition Time; t_{THL}, t_{TLH} Q Output		5	–	75	150	–	75	300	ns
		10	–	30	60	–	30	120	
$\overline{Q}$ Output		5	–	300	600	–	300	1200	
		10	–	150	300	–	150	600	
CL_D Output	C_L = 60 pF	5	–	200	400	–	200	800	
		10	–	100	200	–	100	400	
Clock Rise and Fall Time; t_rCL, t_fCL**		5	–	–	2	–	–	2	μs
		10	–	–	1	–	–	1	
Minimum Data Set-Up Time, t_S		5	–	200	400	–	200	800	ns
		10	–	50	100	–	50	200	
Maximum Clock Input Frequency, f_{CL}***		5	0.8	2	–	0.4	2	–	MHz
		10	2	4	–	1	4	–	
Minimum Data Hold Time, t_H		5	–	50	100	–	50	100	ns
		10	–	100	200	–	100	250	
Minimum Clock Pulse Width, t_W		5	–	1.25	2.5	–	1.3	2.6	μs
		10	–	0.5	1	–	0.62	1.3	
Average Input Capacitance, C_I Clock			–	60	–	–	60	–	pF
All Others			–	5	–	–	5	–	

* Capacitive loading on $\overline{Q}$ output affects propagation delay of Q output. These limits apply for $\overline{Q}$ load $C_L \leq 15$ pF.

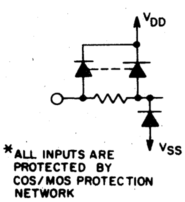
** If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 15 pF and the transition time of the output driving stage.

*** Maximum Clock Frequency for Cascaded Units;

a) Using Delayed Clock Feature –

$$f_{max} = \frac{1}{(n-1)\ CL_D \text{ prop. delay} + Q \text{ prop. delay} + \text{set-up time}}$$ where n = number of packages

b) Not Using Delayed Clock – $f_{max} = \frac{1}{\text{propagation delay} + \text{set-up time}}$



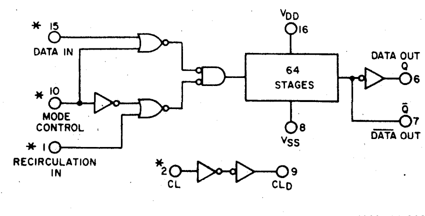


Fig. 12 – Functional diagram.

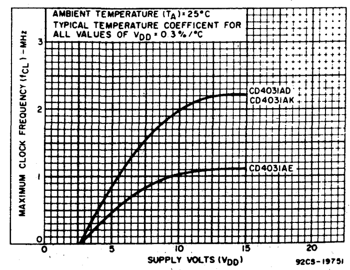


Fig. 8 – Maximum clock input frequency vs. supply voltage.

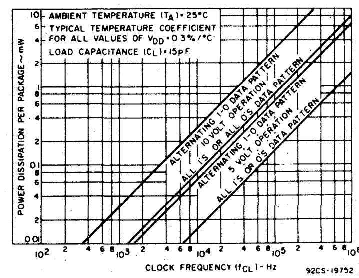


Fig. 9 – Typical power dissipation vs. frequency.

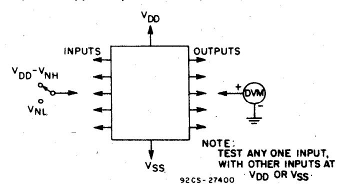


Fig. 10 – Noise-immunity test circuit.

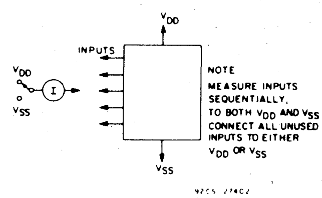
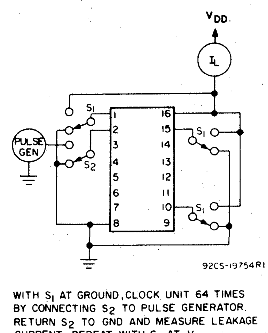


Fig. 11 – Input-leakage-current test circuit.



WITH S_1 AT GROUND, CLOCK UNIT 64 TIMES BY CONNECTING S_2 TO PULSE GENERATOR. RETURN S_2 TO GND AND MEASURE LEAKAGE CURRENT. REPEAT WITH S_1 AT V_{DD}.

Fig. 13 – Quiescent-device-current test circuit.

CD4032A, CD4038A Types

COS/MOS Triple Serial Adders

Positive Logic Adder – CD4032A

Negative Logic Adder – CD4038A

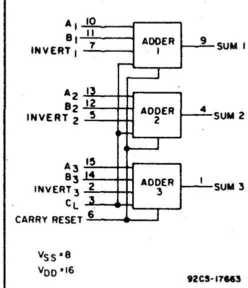
The RCA-CD4032A and CD4038A types consist of three serial adder circuits with common CLOCK and CARRY-RESET inputs. Each adder has two provisions for two serial DATA INPUT signals and an INVERT command signal. When the command signal is a logical "1", the sum is complemented. Data words enter the adder with the least significant bit first; the sign bit trails. The output is the MOD 2 sum of the input bits plus the carry from the previous bit position. The carry is only added at the positive-going clock transition for the CD4032A or at the negative-going clock for the CD4038A, thus, for spike free operation the input data transitions should occur as soon as possible after the triggering edge.

The CARRY is reset to a logical "0" at the end of each word by applying a logical "1" signal to a CARRY-RESET input one bit-position before the application of the first bit of the next word. Figs. 2 and 4 show definitive waveforms for all input and output signals.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Invert inputs on all adders for sum complementing applications**
- **Fully static operation. . . . . . dc to 5 MHz (typ.)**
- **Buffered outputs**
- **Single-phase clocking**
- **Microwatt quiescent power dissipation. . . . 5 μW (typ.)**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**



FUNCTIONAL DIAGRAM

Applications:

- **Serial arithmetic units**
- **Digital correlators**
- **Digital datalink computers**
- **Flight control computers**
- **Digital servo control systems**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
OPERATINT GEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . −55 to +125°C
PACKAGE TYPE E . . . . −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . 0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

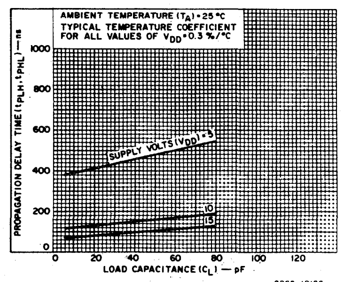


Fig. 1 – Typical propagation delay time vs. load capacitance for A, B, or INVERT inputs to sum outputs.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, H Packages		E Package		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Input Setup Time, t_S	5 10	t_rCL	–	t_rCL	–	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1.5 3	dc dc	2.5 5	MHz
Clock Rise or Fall Time, t_rCL, t_fCL	5 10	– –	15 15	– –	15 15	μs

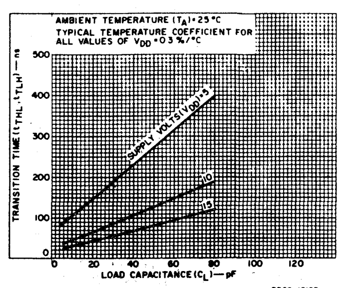


Fig. 2 – Typical transition time vs. load capacitance for sum outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS D, F, H Packages Min.	Typ.	Max.	E Package Min.	Typ.	Max.	UNITS
Propagation Delay Time; t_{PLH}, t_{PHL} A, B, or Invert Inputs to Sum Outputs	5	–	400	1100	–	400	1400	ns
	10	–	125	250	–	125	300	
Clock Input to Sum Outputs	5	–	800	2200	–	800	2400	
	10	–	250	500	–	250	600	
Transition Time; t_{THL}, t_{TLH} (Sum Outputs)	5	–	125	375	–	125	425	ns
	10	–	50	150	–	50	200	
Maximum Clock Input Frequency, f_{CL}	5	1.5	2.5	–	1	2.5	–	MHz
	10	3	5	–	2	5	–	
Clock Rise & Fall Time; t_rCL, t_fCL**	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Minimum Input Set Up Time, t_S*	5, 10	–	–	t_rCL	–	–	t_rCL	ns
Average Input Capacitance, C_I		–	5	–	–	5	–	pF

*This characteristic refers to the minimum time required for the A, B, or Reset Inputs to change state following a positive clock transition (CD4032A) or negative transition (CD4038A).

**If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

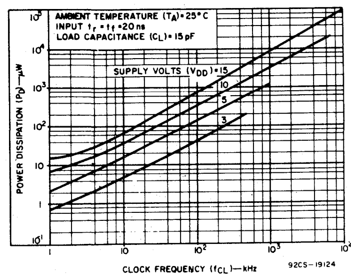


Fig. 3 – Typical dissipation characteristics.

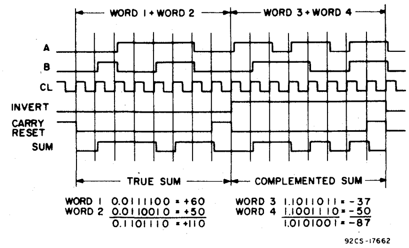


Fig. 4 – CD4032A timing diagram.

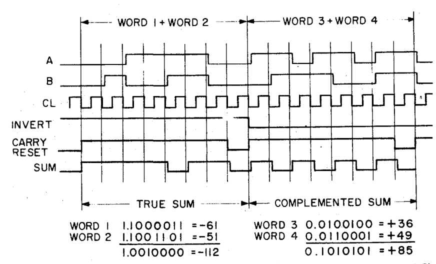


Fig. 5 – CD4038A timing diagram.

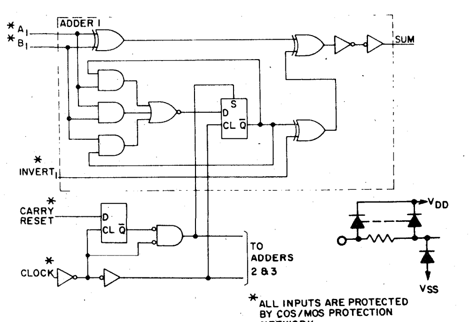


Fig. 6 – CD4032A logic diagram of one of three serial adders.

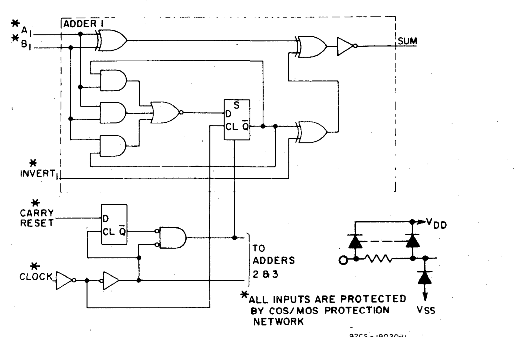


Fig. 7 – CD4038A logic diagram of one of three serial adders.

CD4032A, CD4038A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	μA
	–	–	10	10	0.5	10	600	100	1	100	1400	μA
	–	–	15	50	1	50	2000	500	5	500	5000	μA
Output Voltage: Low-Level V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								V
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								V
	–	0	10	9.95 Min.; 10 Typ.								V
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								V
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								V
	1	–	10	3 Min.; 4.5 Typ.								V
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								V
Inputs High, V_{NMH}	0.5	–	5	1 Min.								V
	1	–	10	1 Min.								V
Output Drive Current N-Channel (Sink), I_DN Min.	0.5	–	5	0.6	0.9	0.5	0.3	0.25	0.9	0.2	0.14	mA
	0.5	–	10	0.75	2.4	0.7	0.6	0.6	2.4	0.5	0.4	mA
P-Channel (Source), I_DP Min.	4.5	–	5	−0.21	−0.4	−0.15	−0.075	−0.14	−0.4	−0.1	−0.095	mA
	9.5	–	10	−0.7	−7.2	−0.55	−0.35	−0.3	−1.2	−0.27	−0.22	mA
Input Leakage Current, I_{IL}, I_{IH}	Any Input			$\pm10^{-5}$ Typ., ±1 Max.								μA
	–	–	15									

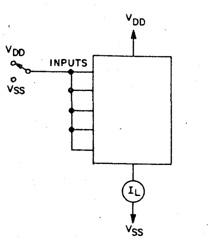


Fig. 8 – Quiescent-device-current test circuit.

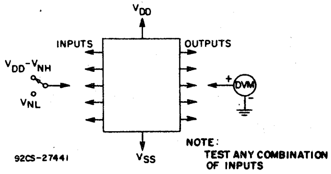


Fig. 9 – Noise-immunity test circuit.

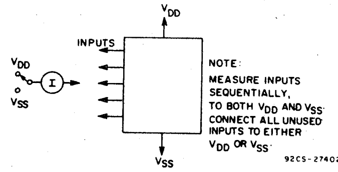


Fig. 10 – Input-leakage-current test circuit.

COS/MOS 8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register

The RCA-CD4034A is a static eight-stage parallel-or serial-input parallel-output register. It can be used to:

1) bidirectionally transfer parallel information between two buses, 2) convert serial data to parallel form and direct the parallel data to either of two buses, 3) store (recirculate) parallel data, or 4) accept parallel data from either of two buses and convert that data to serial form. Inputs that control the operations include a single-phase CLOCK (CL), A DATA ENABLE (AE), ASYNCHRONOUS/SYNCHRONOUS (A/S), A-BUS-TO-B-BUS/2B-BUS-TO-A-BUS (A/B), and PARALLEL/SERIAL (P/S).

Data inputs include 16 bidirectional parallel data lines of which the eight A data lines are inputs (outputs) and the B data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for SERIAL DATA is also provided.

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

PARALLEL OPERATION

A high P/S input signal allows data transfer into the register via the parallel data lines synchronously with the positive transition of the clock provided the A/S input is low. If the A/S input is high the transfer is independent of the clock. The direction of data flow is controlled by the A/B input. When this signal is high the A data lines are inputs (and B data lines are outputs); a low A/B signal reverses the direction of data flow.

The AE input is an additional feature which allows many registers to feed data to a common bus. The A DATA lines are enabled only when this signal is high.

Data storage through recirculation of data in each register stage is accomplished by making the A/B signal high and the AE signal low.

SERIAL OPERATION

A low P/S signal allows serial data to transfer into the register synchronously with the positive transition of the clock. The A/S input is internally disabled when the register is in the serial mode (asynchronous serial operation is not allowed).

The serial data appears as output data on either the B lines (when A/B is high) or the A lines (when A/B is low and the AE signal is high).

Register expansion can be accomplished by simply cascading CD4034A packages.

The CD4034A-Series types are supplied in 24-lead hermetic dual-in-line ceramic packages (D suffix), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

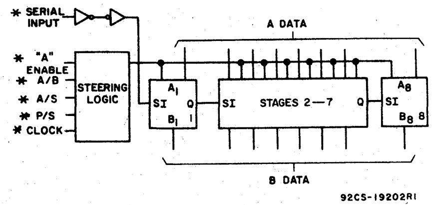
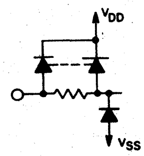


Fig. 1 – Functional diagram.



*ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to + 150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, H . . . . . -55 to +125°C
PACKAGE TYPE E. . . . . -40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal). . . . . -0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = -40 to +60°C (PACKAGE TYPE E). . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E). . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = -55 to +100°C (PACKAGE TYPES D) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES). . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:*

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5 10	500 200	– –	500 200	– –	ns
Clock Pulse Width, t_W	5 10	400 175	– –	400 175	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1.5 3	dc dc	1.5 3	MHz
Clock Rise and Fall Time, t_rCL, t_fCL*	5,10	–	15	–	15	μs

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

Table I — Truth Table for Register Input-Levels and the Resulting Register Operation (L = Low Level, H = High Level, X = Don't Care)

"A" Enable	P/S	A/B	A/S	Operation*
L	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Outputs Disabled
L	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
L	H	L	L	Parallel Mode; "B" Synch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	H	L	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Synch. Data Recirculation
L	H	H	H	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Asynch. Data Recirculation
H	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Output
H	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
H	H	L	L	Parallel Mode; "B" Synch. Parallel Data Input, "A" Parallel Data Output
H	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Input, "A" Parallel Data Output
H	H	H	L	Parallel Mode; "A" Synch. Parallel Data Input, "B" Parallel Data Output
H	H	H	H	Parallel Mode; "A" Asynch. Parallel Data Input, "B" Parallel Data Output

*Outputs change at positive transition of clock in the serial mode and when the A/S control input is "low" in the parallel mode.

Features:

- Bidirectional parallel data input
- Parallel or serial inputs/parallel outputs
- Asynchronous or synchronous parallel data loading
- Parallel data-input enable on "A" data lines
- Data recirculation for register expansion
- Multipackage register expansion
- Fully static operation DC-to-5 MHz (typ.) At $V_{DD}-V_{SS}$ = 10 V
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 µA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Parallel Input/Parallel Output, Parallel Input/Serial Output, Serial Input/Parallel Output, Serial Input/Serial Output Register
- Shift right/shift left register
- Shift right/shift left with parallel loading
- Address register
- Buffer register
- Bus system register with enable parallel lines at bus side
- Double bus register system
- Up-Down Johnson or ring counter
- Pseudo-random code generators
- Sample and hold register (storage, counting, display)
- Frequency and phase comparator

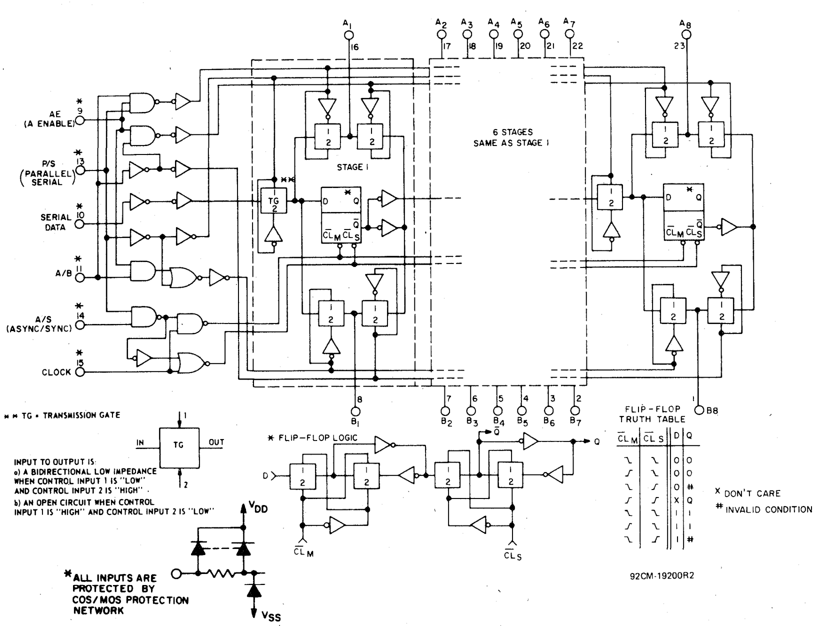


Fig. 2 — Logic diagram.

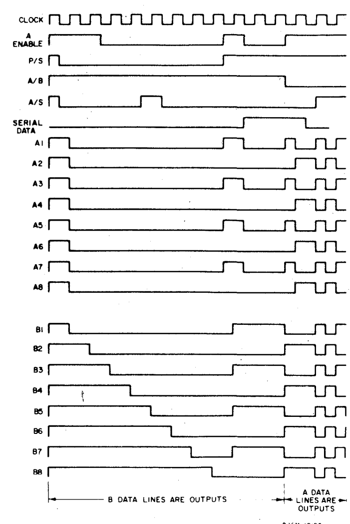


Fig. 3 — Timing diagram.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	μA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max								V
	–	10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.5	–	5	0.124	0.2	0.1	0.07	0.124	0.2	0.1	0.07	mA
	0.5	–	10	0.31	0.5	0.25	0.175	0.31	0.5	0.25	0.175	
P-Channel (Source): I_DP Min.	4.5	–	5	-0.075	-0.1	-0.05	-0.035	-0.075	-0.1	-0.05	-0.035	
	9.5	–	10	-0.188	-0.25	-0.125	-0.088	-0.188	-0.25	-0.125	-0.088	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm10^{-5}$ Typ., ±1 Max.								μA

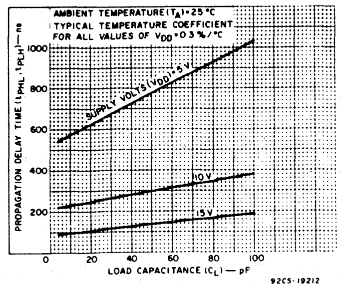


Fig. 4 – Typical propagation delay time vs. load capacitance.

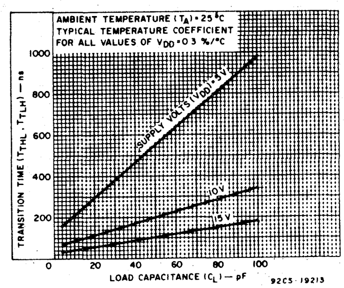


Fig. 5 – Typical transition time vs. load capacitance.

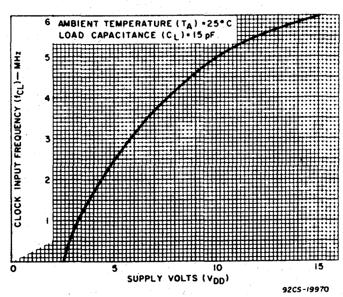


Fig. 6 – Typical clock input frequency vs. supply voltage.

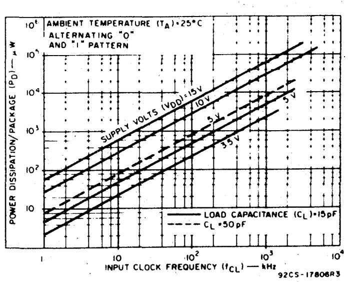


Fig. 7 – Typical dissipation characteristics.

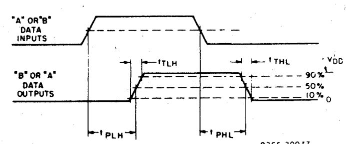


Fig. 8 – Asynchronous operation propagation delay time and transition time.

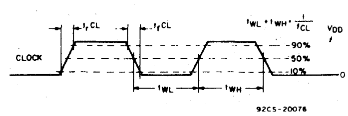


Fig. 9 – Clock pulse rise and fall times.

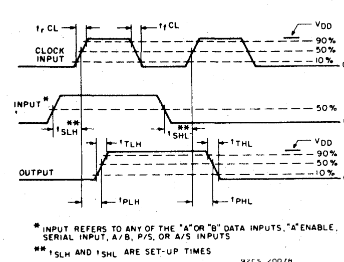


Fig. 10 – Synchronous operation propagation delay times, transition times, and set-up times.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ C$, Input t_r, $t_f = 20 ns$, $C_L = 15 pF$, $RL = 200 k\Omega$

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNIT
		V_{DD} (V)	D, H PACKAGES MIN.	D, H PACKAGES TYP.	D, H PACKAGES MAX.	E PACKAGE MIN.	E PACKAGE TYP.	E PACKAGE MAX.	
Propagation Delay Time; t_{PLH}, t_{PHL}		5	–	600	1200	–	600	1200	ns
		10	–	240	480	–	240	480	
Transition Time; t_{THL}, t_{TLH}		5	–	250	750	–	250	750	ns
		10	–	100	300	–	100	300	
Maximum Clock Input Frequency, f_{CL}		5	1.5	2.5	–	1.5	2.5	–	MHz
		10	3	5	–	3	5	–	
Clock Pulse Width, t_W		5	–	200	400	–	200	400	ns
		10	–	100	175	–	100	175	
Min. High-Level AE, P/S, A/S Pulse Width		5	–	240	480	–	240	480	ns
		10	–	85	195	–	85	195	
Clock Rise & Fall Time t_rCL, t_fCL*		5	–	–	15	–	–	15	μs
		10	–	–	15	–	–	15	
Data Set-Up Time, t_S		5	–	250	500	–	250	500	ns
		10	–	100	200	–	100	200	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

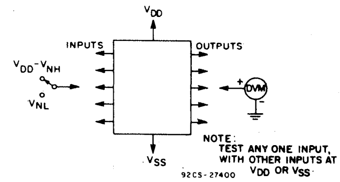


Fig. 11 – Noise-immunity test circuit.

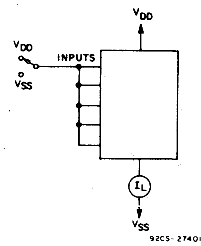


Fig. 12 – Quiescent-device-current test circuit.

APPLICATIONS

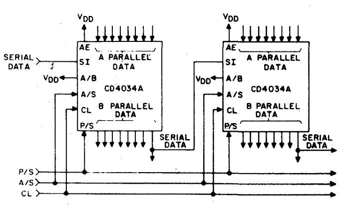


Fig. 14 – 16-Bit parallel in/parallel out, parallel in/serial out, serial in/parallel out, serial in/serial out register.

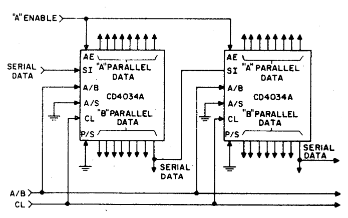


Fig. 15 – 16-Bit serial in/gated parallel out register.

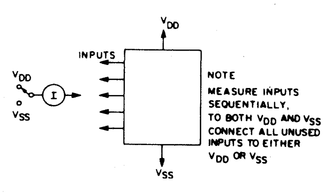


Fig. 13 – Input-leakage-current test circuit.

COS/MOS 4-Stage Parallel In/Parallel Out Shift Register

with J-$\overline{K}$ Serial Inputs and True/ Complement Outputs

Features:

- 4-Stage clocked shift operation
- Synchronous parallel entry on all 4 stages
- J$\overline{K}$ inputs on first stage
- Asynchronous True/Complement control on all outputs
- Static flip-flop operation; Master-slave configuration
- Reset control
- Buffered outputs
- Low power dissipation — 5μW typ. (ceramic)
- High speed — to 5 MHz
- Quiescent current specified to 15 V
- Maximum input leakage current of 1μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

The RCA-CD4035A is a four-stage clocked signal serial register with provision for SYNCHRONOUS PARALLEL inputs to each stage and SERIAL inputs to the first stage via J$\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low).

Parallel entry via the D line of each register stage is permitted only when the PARALLEL/SERIAL control is high.

In the parallel or serial mode information is transferred on positive clock transitions.

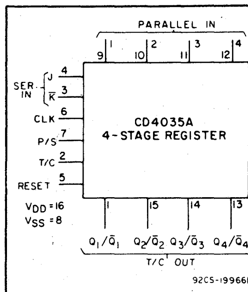
When the TRUE/COMPLEMENT control is high, the TRUE contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with repect to the CLOCK signal.

J$\overline{K}$ input logic is provided on the first stage SERIAL input to minimize logic requirements particularly in counting and sequence-generation applications. With J$\overline{K}$ inputs connected together, the first stage becomes a D flip-flop. An asynchronous common RESET is also provided.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications

- Counters, Registers
  Arithmetic-unit registers
  Shift left — shift right registers
  Serial-to-parallel/parallel-to-serial conversions
- Sequence generation
- Control circuits
- Code conversion



CD4035A
FUNCTIONAL DIAGRAM

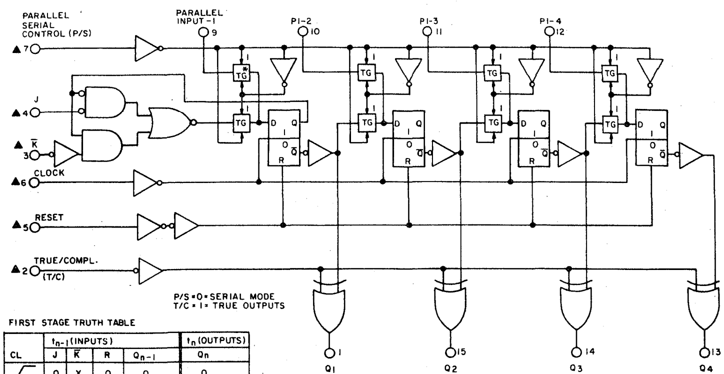
MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . −66 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . −55 to +125°C
PACKAGE TYPE E . . . −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . −0.5 to +15V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . Derate Linearly at 12mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES). . . . 100mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . −0.5 to V_{DD} +0.5V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, except as noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

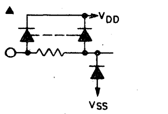
CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			D, F, H PACKAGES		E PACKAGE		
			MIN.	MAX.	MIN.	MAX.	
Supply Voltage Range (For T_A = Full Package-Temperature Range			3	12	3	12	V
Data Setup Time, t_S:	J/$\overline{K}$ Lines	5	500	–	750	–	ns
		10	200	–	250	–	
	Parallel-In Lines	5	350	–	500	–	
		10	80	–	100	–	
Clock Pulse Width, t_W		5	335	–	500	–	ns
		10	165	–	250	–	
Clock Rise and Fall Time, t_rCL, t_fCL		5	–	15	–	15	μs
		10	–	5	–	5	
Reset Pulse Duration, t_W		5	400	–	500	–	ns
		10	175	–	200	–	

CD4035A Types



FIRST STAGE TRUTH TABLE

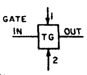
CL	J	K̄	R	Q_{n-1}	Q_n
	t_{n-1} (INPUTS)				t_n (OUTPUTS)
⟋	0	X	0	0	0
⟋	1	X	0	0	1
⟋	X	0	0	1	0
⟋	1	0	0	Q_{n-1}	$\overline{Q_{n-1}}$ TOGGLE MODE
⟋	X	1	0	1	1
⟍	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0



ALL INPUTS PROTECTED BY COS/MOS PROTECTION NETWORK

TERMINAL No. 16 = V_{DD}
TERMINAL No. 8 = GND

*TG = TRANSMISSION GATE



INPUT TO OUTPUT IS:
a) A BIDIRECTIONAL LOW IMPEDANCE WHEN CONTROL INPUT 1 IS LOW AND CONTROL INPUT 2 IS HIGH
b) AN OPEN CIRCUIT WHEN CONTROL INPUT 1 IS HIGH AND CONTROL INPUT 2 IS LOW

Fig. 1 – Logic block diagram.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, F, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	μA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max								V
	–	10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.5	–	5	0.62	1	0.5	0.35	0.43	1	0.35	0.24	mA
	0.5	–	10	1.55	2.5	1.25	0.87	1.05	2.5	0.85	0.59	
P-Channel (Source): I_DP Min.	4.5	–	5	-0.31	-0.5	-0.25	-0.17	-0.2	-0.5	-0.18	-0.12	
	9.5	–	10	-0.81	-1.3	-0.65	-0.45	-0.56	-0.31	-0.45	-0.31	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

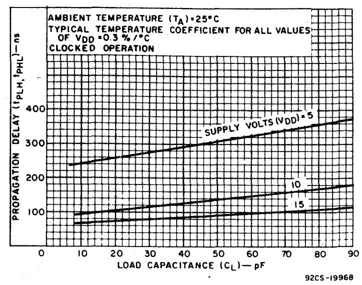


Fig. 2 – Typical propagation delay time vs. load capacitance.

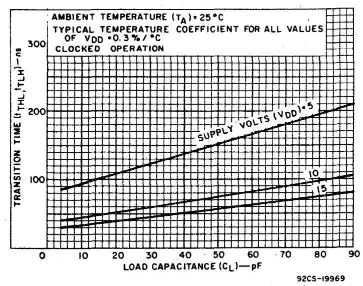


Fig. 3 – Typical transition time vs. load capacitance.

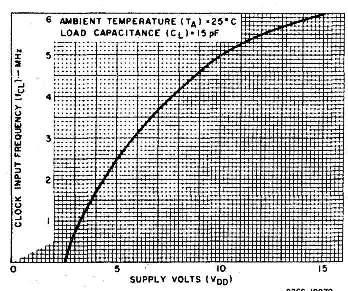


Fig. 4 – Typical clock input frequency vs. supply voltage.

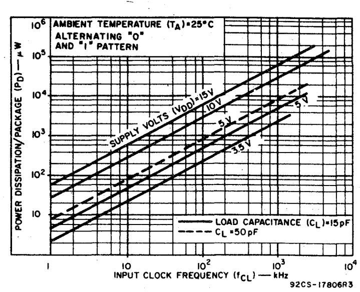


Fig. 5 – Typical dynamic power dissipation characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS
At T_A = 25°C, Input t_r,t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTICS	TEST CONDITIONS		LIMITS						UNITS
			D, F, H PACKAGES			E PACKAGE			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLOCKED OPERATION									
Propagation Delay Time: t_{PLH}, t_{PHL}		5	–	250	500	–	250	700	ns
		10	–	100	200	–	100	300	
Transition Time: t_{THL}, t_{TLH}		5	–	100	200	–	100	300	ns
		10	–	50	100	–	50	150	
Minimum Clock Pulse Width, t_W		5	–	200	335	–	200	500	ns
		10	–	100	165	–	100	250	
Maximum Clock Rise & Fall Time t_{rCL}, t_{fCL}*		5	–	–	15	–	–	15	μs
		10	–	–	5	–	–	5	
Minimum Setup Time: J/$\overline{K}$ Lines		5	–	250	500	–	250	750	ns
		10	–	100	200	–	100	250	
Parallel-In Lines		5	–	100	350	–	100	500	
		10	–	50	80	–	50	100	
Maximum Clock Frequency, f_{CL}		5	1.5	2.5	–	1	2.5	–	MHz
		10	3	5	–	2	5	–	
Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
RESET OPERATION									
Propagation Delay Time: t_{PHL}, t_{PLH}		5	–	250	500	–	250	700	ns
		10	–	100	200	–	100	300	
Minimum Reset Pulse Width, t_W		5	–	200	400	–	200	500	ns
		10	–	100	175	–	100	200	

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

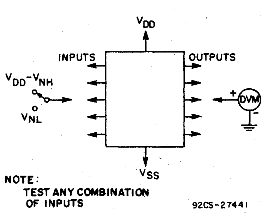


Fig. 6 – Noise-immunity test circuit.

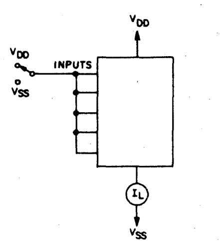


Fig. 7 – Quiescent-device-current test circuit.

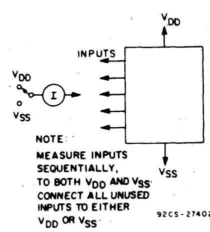


Fig. 8 – Input-leakage-current test circuit.

CD4037A Types

COS/MOS Triple AND/OR Bi-Phase Pairs

The RCA-CD4037A consists of three AND/OR pairs driven by common control signals A and B.

Each circuit has a data input (C), and two output terminals (D and E) that provide outputs in accordance with the truth table shown in Fig. 1. The circuit is useful for coding or decoding signals for split-phase (Bi-phase) communication systems, magnetic recording, and plated wire and core memory systems. A separate V_{CC} terminal is provided to allow level conversion to any voltage from 3 volts to V_{DD}. These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

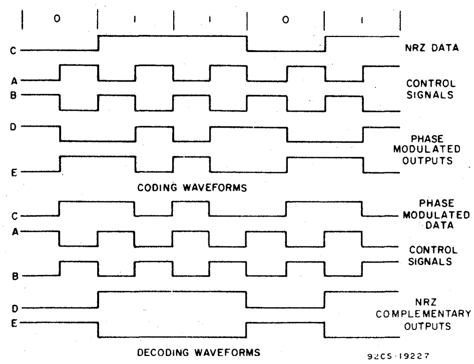
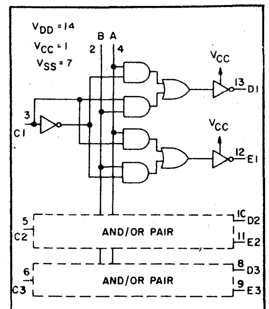


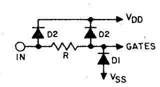
Fig. 1 – Coding and decoding waveforms.



CD 4037A
FUNCTIONAL DIAGRAM

TRUTH TABLE

INPUT A	INPUT B	OUTPUT D	OUTPUT E
0	0	1	1
1	0	C	$\overline{C}$
0	1	$\overline{C}$	C
1	1	0	0



ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

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RECOMMENDED OPERATING CONDITIONS. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS D, F, H PACKAGES MIN.	LIMITS D, F, H PACKAGES MAX.	LIMITS E PACKAGE MIN.	LIMITS E PACKAGE MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V

CAUTION: V_{CC} VOLTAGE LEVEL MUST BE EQUAL TO OR LESS POSITIVE THAN V_{DD}

DYNAMIC ELECTRICAL CHARACTERISTICS
at $T_A = 25^\circ C$, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	D, F, H MIN.	D, F, H TYP.	D, F, H MAX.	E MIN.	E TYP.	E MAX.	UNITS
Propagation Delay Time: A and B Inputs t_{PHL}, t_{PLH}		5	–	225	450	–	325	650	ns
		10	–	75	150	–	100	200	
C Inputs t_{PHL}		5	–	250	500	–	350	700	ns
		10	–	75	150	–	100	200	
t_{PLH}		5	–	225	450	–	325	650	
		10	–	90	180	–	125	250	
Transition Time: High-to-Low Level, t_{THL}		5	–	40	80	–	60	120	ns
		10	–	15	30	–	20	40	
Low-to-High Level, t_{TLH}		5	–	75	150	–	100	200	ns
		10	–	60	120	–	90	180	
Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF

Features:

- **Outputs compatible with low-power TTL systems.**
- **High sink and source current (1.6 mA typ.) capability at $V_{DD} = V_{CC}$ = 10V and V_{DS} = 0.5 V.**
- **Microwatt quiescent power dissipation: P_D = 0.5 µW/ceramic pkg. (typ.), P_D = 2 µW/plastic pkg. (typ.) at V_{DD} = 10 V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 µA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Split-phase (Bi-Phase) communication systems.**
- **Disc, drum, and tape digital recording systems.**
- **Plated wire and core memory systems.**
- **High-to-low logic level converter.**

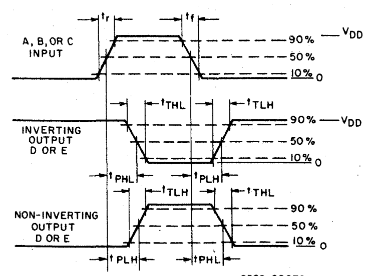


Fig. 2 – Waveforms for measurement of dynamic characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . -65 to +150° C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . -55 to +125° C
PACKAGE TYPE E . . . . -40 to +85° C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . -0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = -40 to +60° C (PACKAGE TYPE E) . . . . 500 mW
FOR T_A = +60 to +85° C (PACKAGE TYPE E) . . Derate Linearly at 12 mW/° C to 200 mW
FOR T_A = -55 to +100° C (PACKAGE TYPES D, F) . . . . 500 mW
FOR T_A = +100 to +125° C (PACKAGE TYPES D, F) Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . -0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . +265° C

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, F, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.03	5	300	50	0.1	50	700	μA
	–	–	10	10	0.05	10	600	100	0.2	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max								V
	–	10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.5	–	5	0.85	0.7	1.2	0.45	0.4	0.35	0.7	0.3	mA
	0.5	–	10	1.3	1.1	2	0.7	0.65	0.55	1.1	0.45	
P-Channel (Source): I_DP Min.	4.5	–	5	-0.65	-0.55	-1	-0.35	-0.35	-0.3	-0.55	-0.2	
	9.5	–	10	-0.9	-0.75	-1.6	-0.45	-0.5	-0.4	-0.75	-0.3	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm10^{-5}$ Typ., ±1 Max.								μA

For quiescent device current, noise immunity, and input leakage current test circuits see "Ratings and Characteristics" at the beginning of the COS/MOS section.

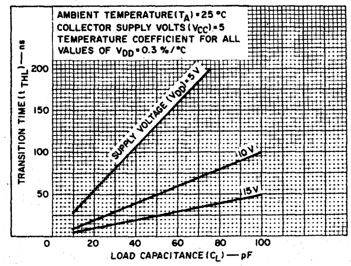


Fig. 3 — Typical transition time vs. load capacitance.

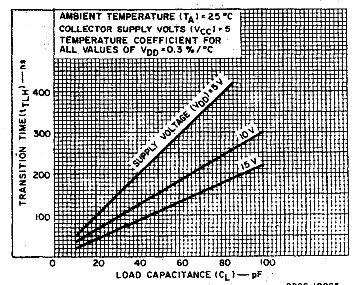


Fig. 4 — Typical transition time vs. load capacitance.

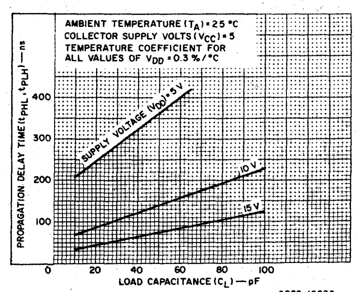


Fig. 5 — Typical propagation delay time vs. load capacitance.

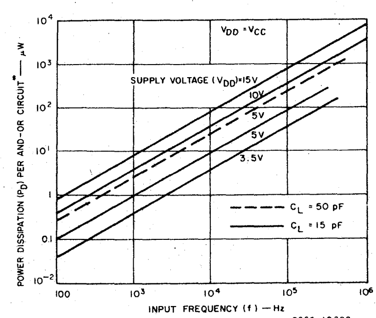


Fig. 6 — Typical dissipation characteristics.

COS/MOS 12-Stage Ripple-Carry Binary Counter/Divider

The RCA-CD4040A consists of an input-pulse-shaping circuit and 12 ripple-carry binary counter stages. Resetting the counter to the all-O's state is accomplished by a high-level on the reset line. A master-slave flip-flop configuration is utilized for each counter stage. The state of the counter is advanced one step in binary order on the negative-going transition of the input pulse. All inputs and outputs are fully buffered.

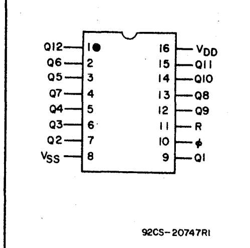
These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **Medium-speed operation . . . 5 MHz (typ.) input pulse rate at $V_{DD} - V_{SS}$ = 10 V**
- **Low output impedance . . . 750 Ω (typ.) at $V_{DD} - V_{SS}$ = 10 V and V_{DS} = 0.5 V**
- **Common reset**
- **Fully static operation**
- **All 12 buffered outputs available**
- **Low-power TTL compatible**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Frequency-dividing circuits**
- **Time-delay circuits**
- **Control counters**



CD4040A
TERMINAL DIAGRAM

RECOMMENDED OPERATING CONDITONS at T_A = 25°C, Except as Noted:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges :

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,H Packages Min.	D,F,H Packages Max.	E Package Min.	E Package Max.	UNITS
Supply Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Input Pulse Width, t_W	5 10	400 110	– –	500 125	– –	ns
Input-Pulse Frequency, f_ϕ	5 10	dc dc	1.5 4	dc dc	1.5 4	MHz
Input-Pulse Rise or Fall Time, $t_{r\phi}, t_{f\phi}$	5 10	15 15	– –	15 15	– –	μs
Reset Pulse Width, t_W	5 10	1000 500	– –	1250 600	– –	ns

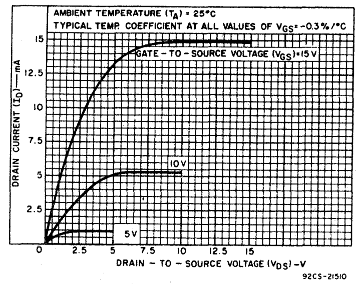


Fig.2 – Typical output n-channel drain characteristics.

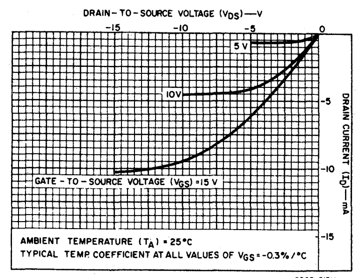


Fig.3 – Typical output p-channel drain characteristics.

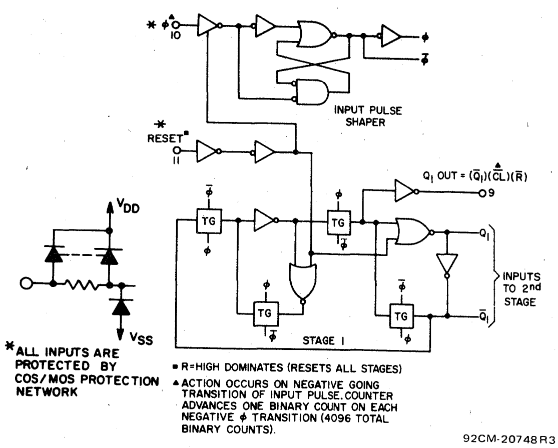


Fig.1 – Logic diagram of CD4040A input pulse shaper and 1 of 12 stages.

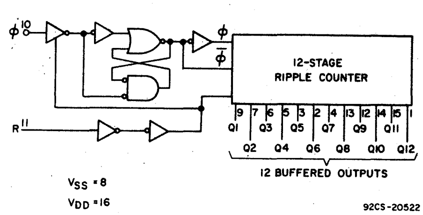


Fig.4 – Functional diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) .... −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
  PACKAGE TYPES D, F, H .... −55 to +125°C
  PACKAGE TYPE E .... −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  (Voltages referenced to V_{SS} Terminal) .... −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
  FOR T_A = −40 to +60°C (PACKAGE TYPE E) .... 500 mW
  FOR T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/°C to 200 mW
  FOR T_A = −55 to +100°C (PACKAGE TYPES D, F) .... 500 mW
  FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) .... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) .... 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C

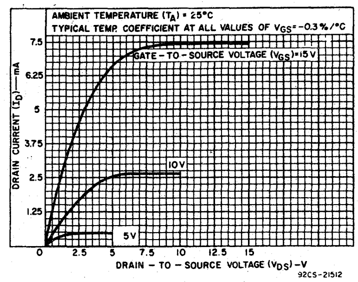


Fig.5 – Minimum output n-channel drain characteristics.

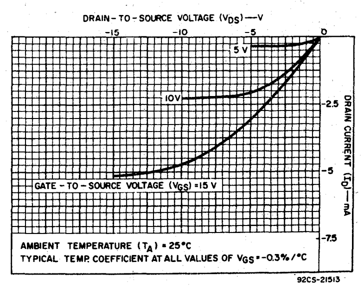


Fig.6 – Minimum output p-channel drain characteristics.

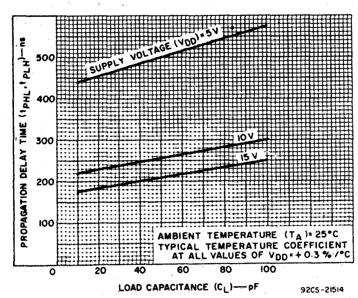


Fig.7 – Typical propagation delay time vs. load capacitance (per stage).

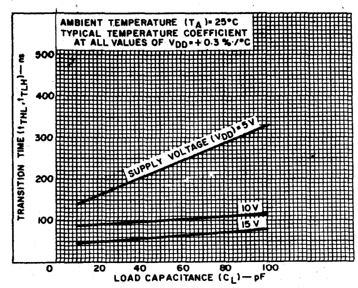


Fig.8 – Typical transition time vs. load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	15	0.5	15	900	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	2.5	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High-Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), $I_D N$ Min.	0.5	–	5	0.22	0.36	0.145	0.102	0.21	0.36	0.08	0.056	mA
	0.5	–	10	0.44	0.75	0.4	0.250	0.42	0.75	0.2	0.14	
P-Channel (Source): $I_D P$ Min.	4.5	–	5	−0.15	−0.25	−0.1	−0.07	−0.15	−0.25	−0.06	−0.04	
	9.5	–	10	−0.03	−0.5	−0.25	−0.175	−0.29	−0.5	−0.15	−0.1	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm10^{-5}$ Typ., ±1 Max.								μA

CD4040A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

Characteristic	Test Conditions	V_{DD} (V)	LIMITS D,F,H Packages Min.	Typ.	Max.	E Package Min.	Typ.	Max.	Units
Input-Pulse Operation									
Propagation Delay Time, t_{PLH}, t_{PHL}●		5	–	450	900	–	450	950	ns
		10	–	225	450	–	225	475	
Transition Time, t_{THL}, t_{TLH}		5	–	150	300	–	150	350	ns
		10	–	75	150	–	75	175	
Maximum Input-Pulse Frequency, f_ϕ		5	1.5	2.5	–	1.5	2.5	–	MHz
		10	4	6	–	4	6	–	
Minimum Input-Pulse Width, t_W	f=100 kHZ	5	–	200	400	–	200	500	ns
		10	–	75	110	–	75	125	
Input-Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$▲		5	–	–	15	–	–	15	µs
		10	–	–	7.5	–	–	7.5	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
Reset Operation									
Propagation Delay Time, t_{PHL}*		5	–	500	1000	–	500	1250	ns
		10	–	250	500	–	250	600	
Minimum Reset Pulse Width, t_W		5	–	500	1000	–	500	1250	ns
		10	–	250	500	–	250	600	

● Measured from the 50% level of the negative input pulse edge to the 50% level of either the positive or negative edge of the Q1 output (pin 9); or measured from the negative edge of Q1 through Q11 outputs to the positive or negative edge of the next higher output.

▲ Maximum input rise or fall time for functional operation.

* Measured from the positive edge of the reset pulse to the negative edge of any output (Q1 to Q12).

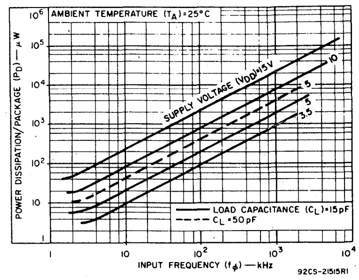


Fig.9 – Typical dissipation characteristics.

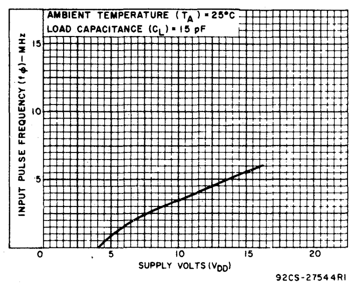


Fig.10 – Typical input-pulse frequency vs. supply voltage.

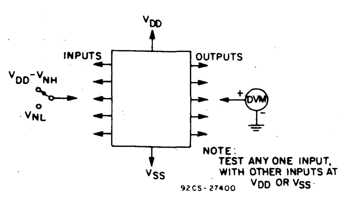


Fig. 11– Noise-immunity test circuit.

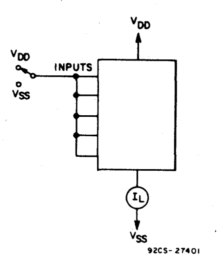


Fig.12 – Quiescent-device-current test circuit.

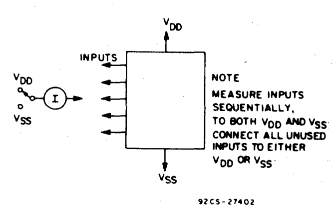
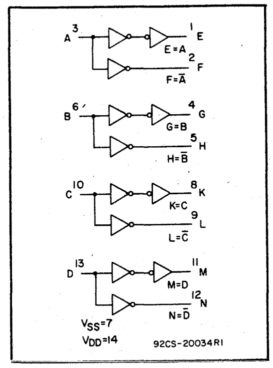


Fig.13 – Input-leakage-current test circuit.

COS/MOS Quad True/Complement Buffer

The RCA-CD4041A types are quad true/complement buffers consisting of n- and p-channel units having low channel resistance and high current (sourcing and sinking) capability. The CD4041A is intended for use as a buffer, line driver, or COS/MOS-to-TTL driver. It can be used as an ultra-low power resistor-network driver for A/D and D/A conversion, as a transmission-line driver, and in other applications where high noise immunity and low-power dissipation are primary design requirements.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).



MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) .... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

- PACKAGE TYPES D, F, H .... −55 to +125°C
- PACKAGE TYPE E .... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) .... −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

- FOR T_A = −40 to +60°C (PACKAGE TYPE E) .... 500 mW
- FOR T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/°C to 200 mW
- FOR T_A = −55 to +100°C (PACKAGE TYPES D, F) .... 500 mW
- FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) .... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) .... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C

Features:

True Output

- **High current source and sink capability**
  8 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 10 V
  3.2 mA (typ.) @ V_{DS} = 0.4 V, V_{DD} = 5 V
  (two TTL loads)

Complement Output

- **Medium current source and sink capability**
  3.6 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 10 V
  1.6 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 5 V
- **Quiescent current specified to 15 V**
- **Maximum input peakage of 1 µA at 15 V (full package-temperature range)**
- **1-V noise margin (full package temperature range)**

Applications:

- **High current source/sink driver**
- **COS/MOS-to-DTL/TTL converter**
- **Display driver**
- **MOS clock driver**
- **Resistor network driver (Ladder or weighted R)**
- **Buffer**
- **Transmission line driver**

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	12	V

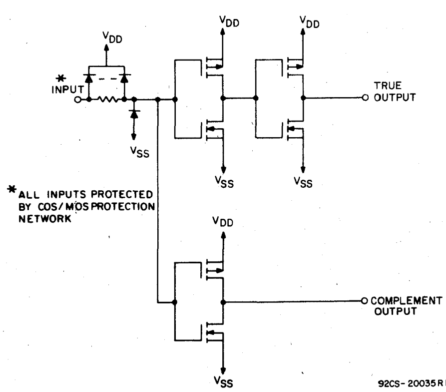


Fig.1 – CD4041A schematic diagram.

CD4041A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C and C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS				UNITS
		V_{DD} (Volts)	D,F,H Packages TYP.	D,F,H Packages MAX.	E Package TYP.	E Package MAX.	
Propagation Delay Time: High-to-Low Level t_{PHL}	True Output	5	65	115	65	140	ns
		10	40	75	40	100	
	Comp. Output	5	55	100	55	125	ns
		10	30	45	30	65	
Low-to-High Level t_{PLH}	True Output	5	75	125	75	150	ns
		10	45	75	45	100	
	Comp. Output	5	45	100	45	125	ns
		10	25	40	25	60	
Transition Time: High-to-Low Level t_{THL}	True Output	5	20	40	20	60	ns
		10	13	25	13	40	
	Comp. Output	5	40	60	40	80	ns
		10	25	40	25	50	
Low-to-High Level t_{TLH}	True Output	5	20	40	20	60	ns
		10	13	25	13	40	
	Comp. Output	5	35	55	35	75	ns
		10	25	40	25	50	
Input Capacitance C_I	Any Input		5	–	5	–	pF

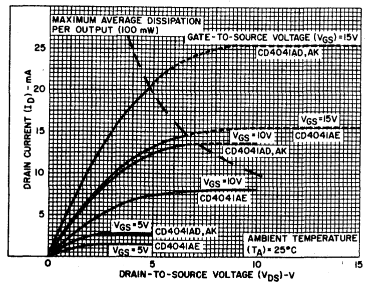


Fig.8 – Minimum output n-channel drain characteristics –complement output.

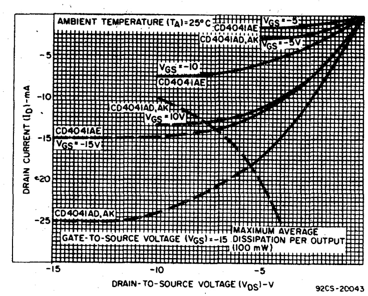


Fig.9 – Minimum output p-channel drain characteristics – complement output.

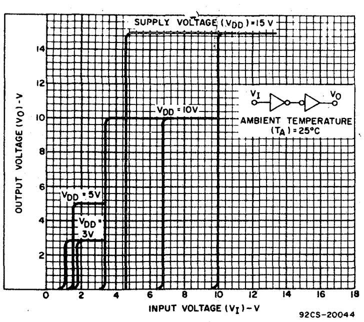


Fig.10 – Minimum and maximum transfer characteristics – true output.

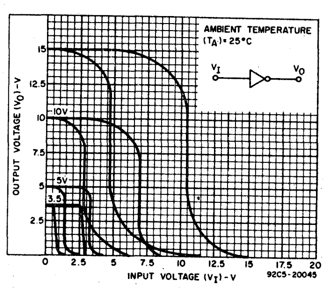


Fig.11 – Minimum and maximum transfer characteristics – complement output.

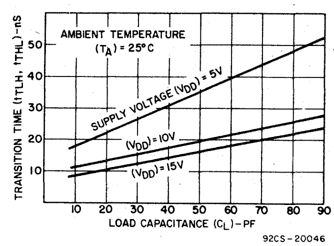


Fig.12 – Typical transition time vs. C_L – true output.

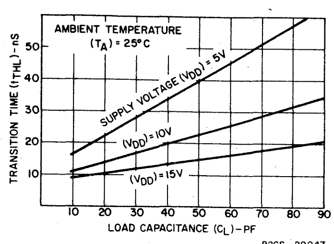


Fig.13 – Typical high-to-low level transition time vs. C_L – complement output.

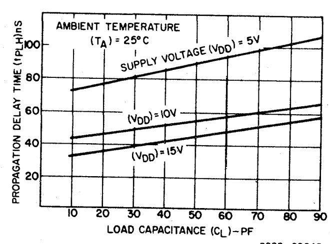


Fig.14 – Typical low-to-high level propagation delay time vs. C_L – true output.

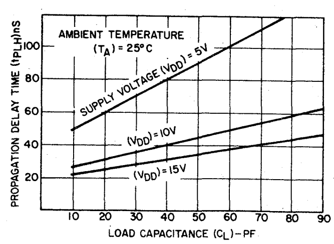


Fig.15 – Typical low-to-high level propagation delay time vs. C_L – complement output.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	1	0.005	1	60	10	0.01	10	140	µA
	–	–	10	2	0.005	2	120	20	0.02	20	280	
	–	–	15	25	0.25	25	1000	250	2.5	250	2500	
Output Voltage: Low-Level, V_{OL}	–	0.5	5	0 Typ.; 0.05 Max.								V
	–	0.10	10	0 Typ.; 0.05 Max.								
High-Level, V_{OH}	–	0.5	5	4.95 Min.; 5 Typ.								
	–	0.10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_{DN} Min.	0.4	True	5	2.1	3.2	1.6	1.2	1	3.2	0.8	0.7	mA
	0.5	True	10	6.25	10	5	3.5	3	10	2.5	2.2	
	0.5	Comp.	5	1	1.6	0.8	0.55	0.5	1.6	0.4	0.35	
	0.5	Comp.	10	2.5	4	2	1.4	1.2	4	1	0.9	
P-Channel (Source) I_{DP} Min.	4.5	True	5	−1.75	−2.8	−1.4	−1	−0.85	−2.8	−0.7	−0.6	
	9.5	True	10	−5	−8	−4	−2.8	−2.4	−8	−2	−1.8	
	4.5	Comp.	5	−0.75	−1.2	−0.6	−0.4	−0.35	−1.2	−0.3	−0.27	
	9.5	Comp.	10	−2.25	−3.6	−1.8	−1.25	−1.1	−3.6	−0.9	−0.8	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ.; 1 Max.								µA

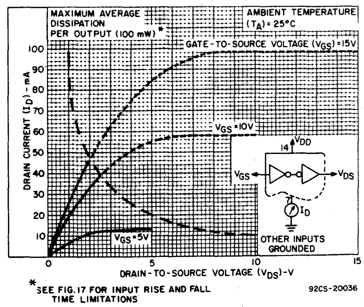


Fig.2 – Typical output n-channel drain characteristics – true output.

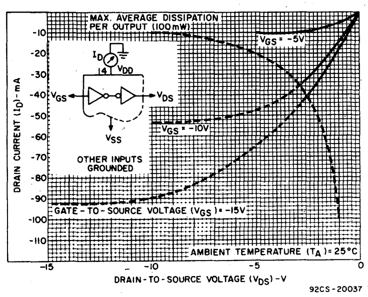


Fig.3 – Typical output p-channel drain characteristics – true output.

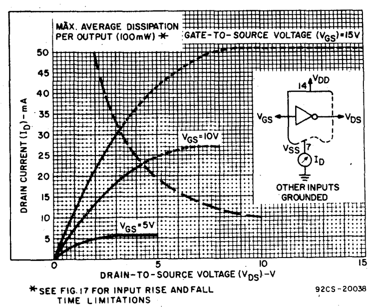


Fig.4 – Typical output n-channel drain characteristics – complement output.

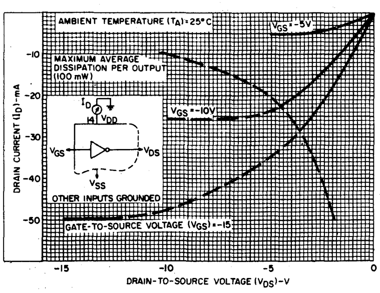


Fig.5 – Typical output p-channel drain characteristics – complement output.

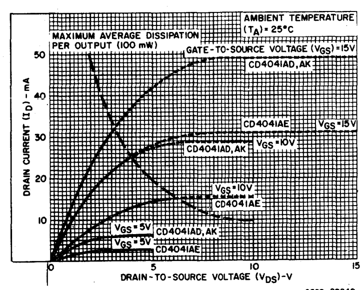


Fig.6 – Minimum output n-channel drain characteristics – true output.

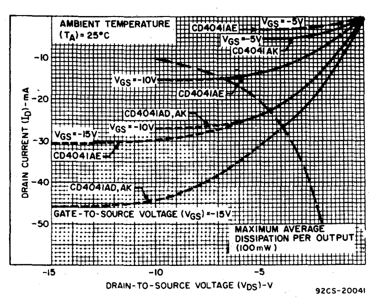


Fig.7 – Minimum output p-channel drain characteristics – true output.

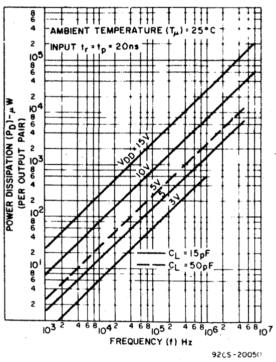


Fig.16 – Typical power dissipation vs. frequency per output pair.

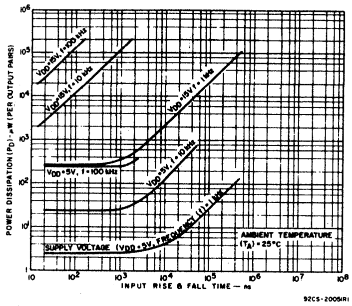


Fig.17 – Typical power dissipation vs. input rise & fall time per output pair.

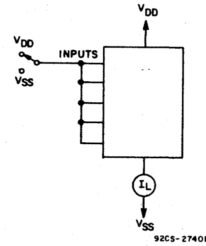


Fig.18 – Quiescent device current test circuit.

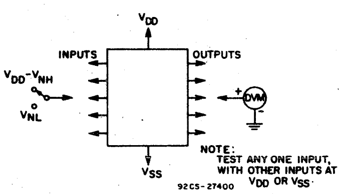


Fig.19 – Noise immunity test circuit.

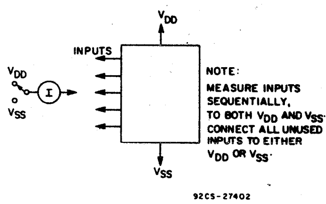
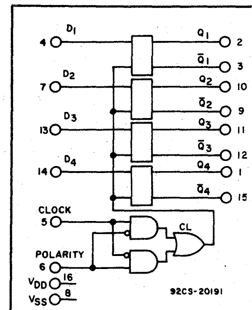


Fig.20 – Input leakage current test circuit.

COS/MOS Quad Clocked "D" Latch

The RCA-CD4042A types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the n- and p-channel output devices is balanced and all outputs are electrically identical. Information present at the data input is transferred to outputs Q and $\bar{Q}$ during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4042A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . –55 to +125°C
PACKAGE TYPE E . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = –40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . +265°C

Features:

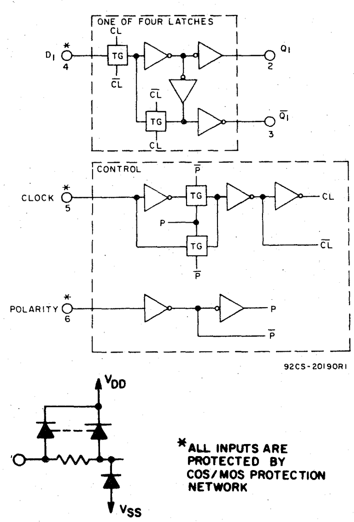
- **Clock polarity control**
- **Q and $\bar{Q}$ outputs**
- **Common clock**
- **Low power TTL compatible**
- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 µA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Buffer storage**
- **Holding register**
- **General digital logic**

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 KΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,H Packages Typ.	LIMITS D,F,H Packages Max.	LIMITS E Package Typ.	LIMITS E Package Max.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} Data In to Q	5 10	150 75	300 150	150 75	400 200	ns
Data In to $\bar{Q}$	5 10	250 100	500 200	250 100	600 250	ns
Clock to Q	5 10	300 125	600 250	300 125	750 300	ns
Clock to $\bar{Q}$	5 10	400 175	800 350	400 175	1000 400	ns
Transition Time: t_{THL}, t_{TLH}	5 10	100 50	200 100	100 50	300 150	ns
Minimum Clock Pulse Width, t_W	5 10	175 60	250 120	175 60	350 175	ns
Minimum Hold Time, t_H	5 10	150 60	300 120	150 60	350 150	ns
Minimum Setup Time, t_S	5 10	0 0	50 30	0 0	50 30	ns
Minimum Clock Rise or Fall Time: t_r, t_f	5 10	Not rise or fall time sensitive.				µs
Input Capacitance, C_I (Any Input)	–	5	–	5	–	pF



CLOCK	POLARITY	Q
0	0	D
⟋ (rising)	0	LATCH
1	1	D
⟍ (falling)	1	LATCH

Fig. 1 – Logic block diagram & truth table.

CD4042A Types

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,H Packages Min.	Max.	E Package Min.	Max.	UNITS
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	12	3	12	V
Clock Pulse Width, t_W	5 10	350 175	– –	250 120	– –	ns
Setup Time, t_S	5 10	50 30	– –	50 30	– –	ns
Hold Time, t_H	5 10	350 150	– –	300 120	– –	ns
Clock Rise or Fall Time: t_r, t_f	5 10	Not rise or fall time sensitive.				μs

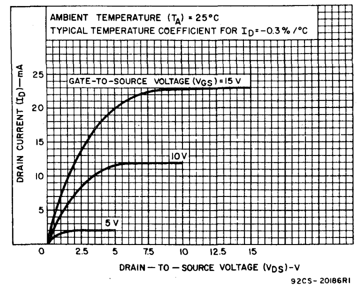


Fig. 2 – Typical output n-channel drain characteristics.

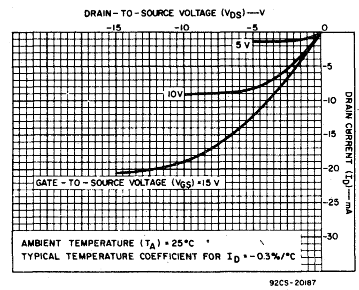


Fig. 3 – Typical output p-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions V_O (V)	V_{IN} (V)	V_{DD} (V)	Limits at Indicated Temperatures (°C) D,F,H Packages –55	+25 Typ.	+25 Limit	+125	E Package –40	+25 Typ.	+25 Limit	+85	Units
Quiescent Device Current, I_L Max.	–	–	5	1	0.005	1	60	10	0.01	10	140	μA
	–	–	10	2	0.005	2	120	20	0.02	20	280	
	–	–	15	25	0.25	25	1000	250	2.5	250	2500	
Output Voltage: Low-Level, V_{OL}	–	0,5	5	0 Typ.; 0.05 Max.								V
	–	0,10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}	–	0,5	5	4.95 Min.; 5 Typ.								
	–	0,10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink), I_DN Min.	0.5	–	5	0.5	1	0.4	0.27	0.24	1	0.2	0.18	mA
	0.5	–	10	1.25	2	1	0.7	0.6	2	0.5	0.45	
p-Channel (Source), I_DP Min.	4.5	–	5	-0.45	-1	-0.35	-0.25	-0.2	-1	-0.175	-0.15	
	9.5	–	10	-1.15	-2	-0.9	-0.6	-0.34	-2	-0.45	-0.4	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		15	$\pm10^{-5}$ Typ.; 1 Max.								μA

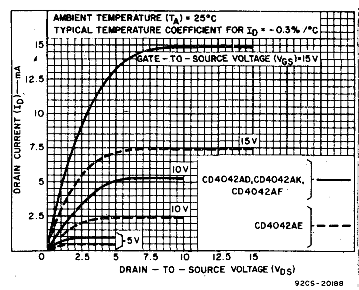


Fig. 4 – Minimum n-channel drain characteristics.

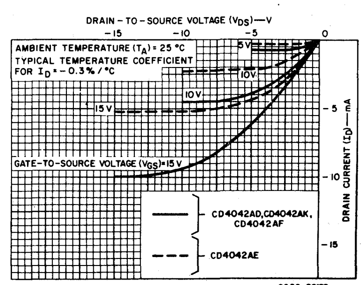
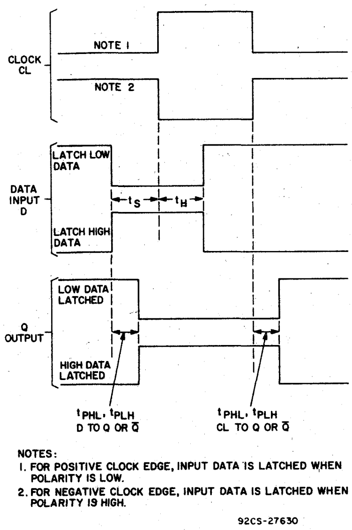


Fig. 5 – Minimum p-channel drain characteristics.



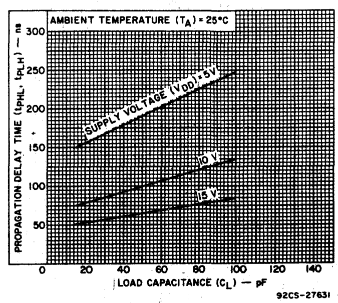


Fig. 7 – *Typical propagation delay time vs. load capacitance— data to Q.*

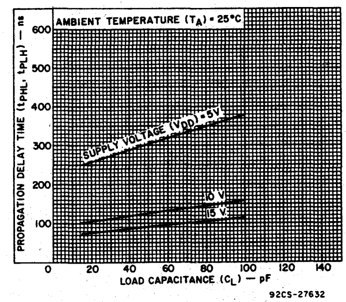


Fig. 8 – *Typical propagation delay time vs. load capacitance – data to $\bar{Q}$.*

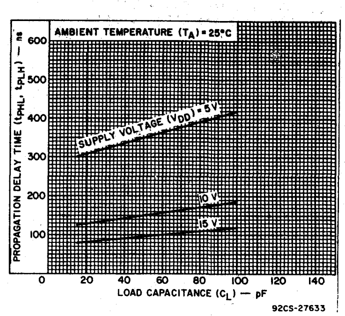


Fig. 9 – *Typical propagation delay time vs. load capacitance – clock to Q.*

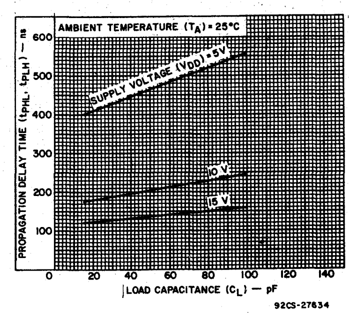


Fig. 10 – *Typical propagation delay time vs. load capacitance – clock to $\bar{Q}$.*

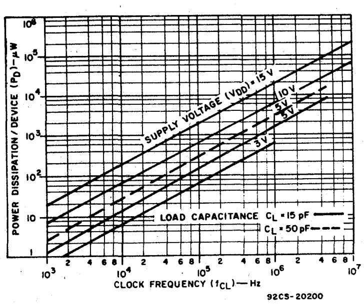


Fig. 11 – *Typical dissipation characteristics.*

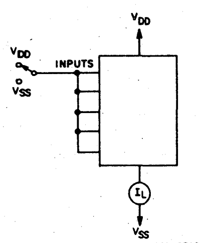


Fig. 12 – *Quiescent device current test circuit.*

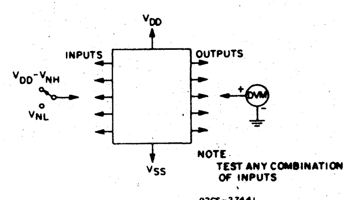


Fig. 13 – *Noise immunity test circuit.*

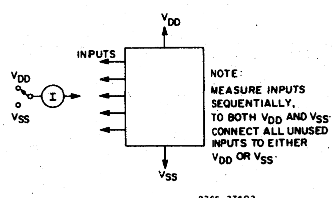


Fig. 14 – *Input leakage current test circuit.*

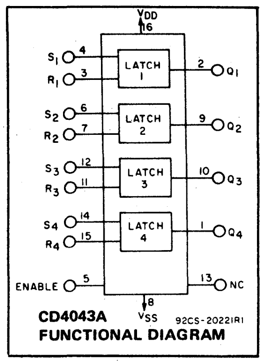
CD4043A, CD4044A Types

COS/MOS Quad 3-State R/S Latches

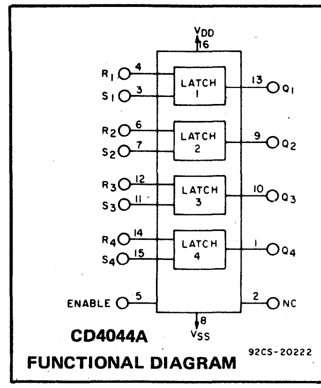
Quad NOR R/S Latch – CD4043A
Quad NAND R/S Latch – CD4044A

The RCA-CD4043A types are quad cross-coupled 3-state COS/MOS NOR latches and the CD4044A types are quad cross-coupled 3-state COS/MOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or high on the ENABLE input connects the latch states to the Q outputs. A logic "0" or low on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common busing of the outputs. The logic operation of the latches is summarized in the truth table shown in Fig. 1.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4043A FUNCTIONAL DIAGRAM



CD4044A FUNCTIONAL DIAGRAM

Applications:

- **Holding register in multi-register system**
- **Four bits of independent storage with output ENABLE**
- **Strobed register**
- **General digital logic**

Features:

- **3-Level outputs with common output ENABLE**
- **Separate SET and RESET inputs for each latch**
- **NOR and NAND configurations**
- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

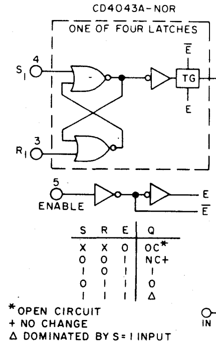
MAXIMUM RATINGS, *Absolute-Maximum Values:*

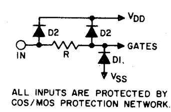
STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
 PACKAGE TYPES D, F, H . . . . –55 to +125°C
 PACKAGE TYPE E . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
 (Voltages referenced to V_{SS} Terminal): . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
 FOR T_A = –40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
 FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
 FOR T_A = –55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
 FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
 FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
 At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	VDD (V)	LIMITS D,F,H Packages Min.	Max.	E Package Min.	Max.	UNITS
Supply-Voltage Range (For T_A = Full Package Temperature Range	–	3	12	3	12	V
Set or Reset Pulse Width, t_W	5 10	200 100	– –	225 110	– –	ns

CD4043A-NOR





CD4044A-NAND

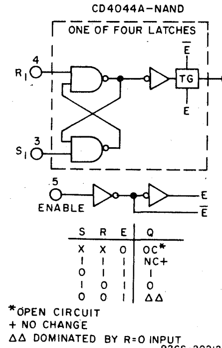


Fig. 1 — Logic diagrams and truth tables.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	1	0.005	1	60	10	0.01	10	140	μA
	–	–	10	2	0.005	2	120	20	0.02	20	280	μA
	–	–	15	25	0.25	25	1000	250	2.5	250	2500	μA
Output Voltage: Low-Level, V_{OL}	–	0,5	5	0 Typ.; 0.05 Max.								V
	–	0,10	10	0 Typ.; 0.05 Max.								V
High Level, V_{OH}	–	0,5	5	4.95 Min.; 5 Typ.								V
	–	0,10	10	9.95 Min.; 10 Typ.								V
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								V
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.;								V
	1	–	10	3 Min.; 4.5 Typ.								V
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								V
Inputs High, V_{NMH}	0.5	–	5	1 Min.								V
	1	–	10	1 Min.								V
Output Drive Current: n-Channel (Sink), I_DN Min.	0.5	–	5	0.25	0.5	0.2	0.19	0.12	0.5	0.1	0.09	mA
	0.5	–	10	0.61	1	0.5	0.35	0.3	1	0.25	0.22	mA
p-Channel (Source), I_DP Min.	4.5	–	5	-0.22	-0.5	-0.175	-0.12	-0.11	-0.5	-0.09	-0.08	mA
	9.5	–	10	-0.5	-1	-0.4	-0.28	-0.24	-1	-0.2	-0.18	mA
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm10^{-5}$ Typ.; ±1 Max.								μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,H Packages Typ.	D,F,H Max.	E Package Typ.	E Max.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} SET or RESET to Q	5 10	175 75	350 175	175 75	400 200	ns
3-State Propagation Delay Time: ENABLE to Q t_{PHZ}, t_{PZH}	5 10	100 50	200 100	100 50	200 100	ns
t_{PLZ}, t_{PZL}	5 10	80 40	160 80	80 40	160 80	ns
Transition Time: t_{THL}, t_{PLH}	5 10	100 50	200 100	100 50	250 125	ns
Minimum SET or RESET Pulse Width, t_W	5 10	80 40	200 100	80 40	225 110	ns
Average Input Capacitance, C_I (Any Input)	–	5	–	5	–	pF

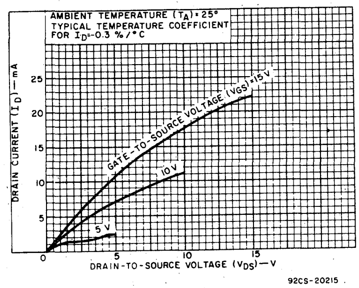


Fig.2 – Typical output n-channel drain characteristics.

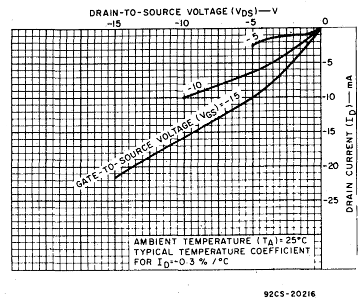


Fig. 3 – Typical output p-channel drain characteristics.

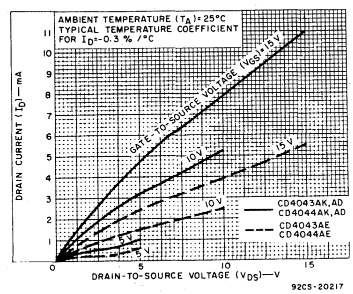


Fig. 4 – Minimum n-channel drain characteristics.

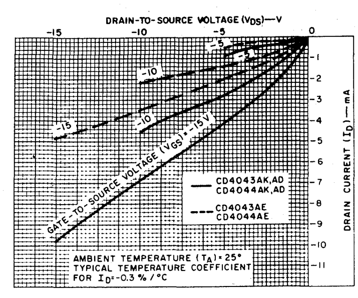


Fig. 5 – Minimum p-channel drain characteristics.

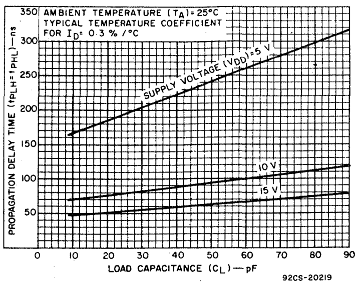


Fig. 6 — Typical propagation delay time vs. C_L.

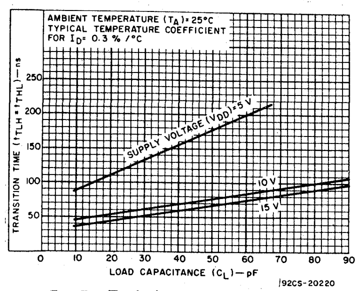


Fig. 7 — Typical transition time vs. C_L.

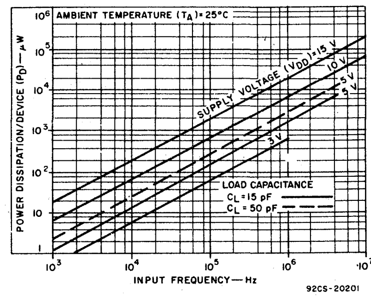


Fig. 8 — Typical dissipation characteristics.

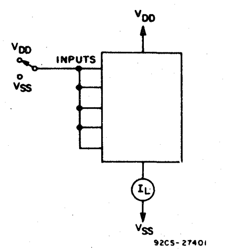


Fig. 9 — Quiescent device current test circuit.

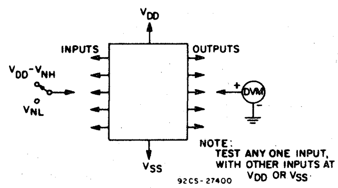


Fig. 10 — Noise immunity test circuit.

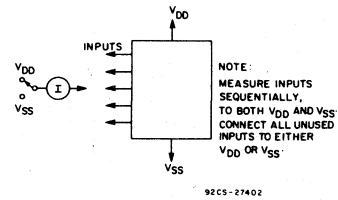
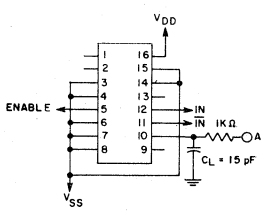


Fig. 11 — Input leakage current test circuit.



TEST	IN	$\overline{IN}$	A
t_{PHZ}	V_{DD}	V_{SS}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}	V_{DD}
t_{PZH}	V_{DD}	V_{SS}	V_{SS}
t_{PZL}	V_{SS}	V_{DD}	V_{DD}

Z = HIGH IMPEDANCE

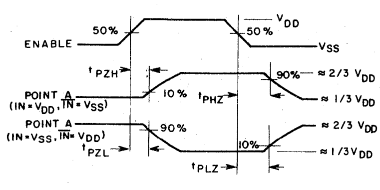


Fig. 12 — ENABLE propagation delay time test circuit and waveforms.

APPLICATIONS

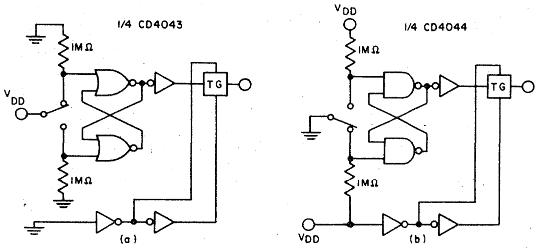


Fig. 13 — Switch bounce eliminator.

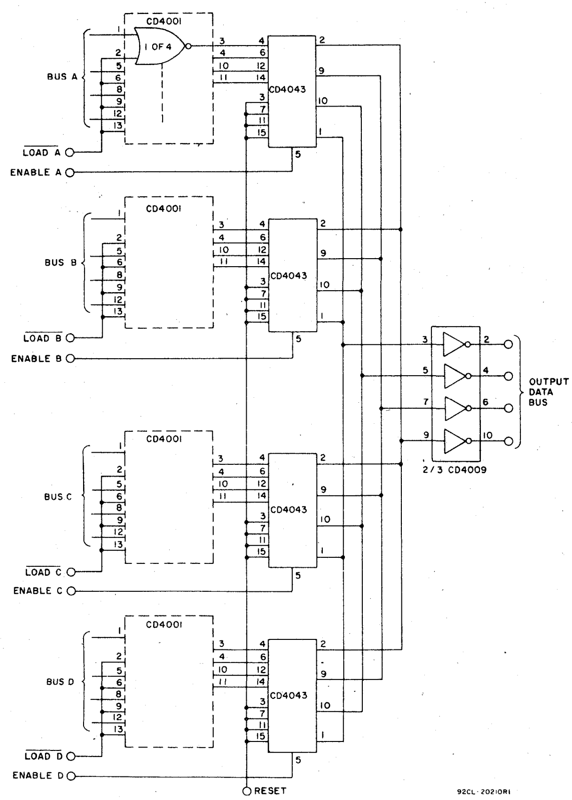


Fig. 14 — Multiple bus storage.

COS/MOS 21-Stage Counter

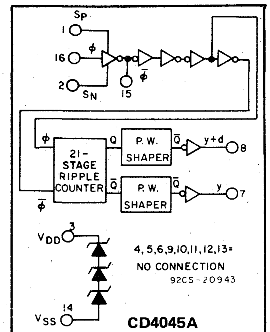
The RCA-CD4045A is a timing circuit consisting of 21 counter stages, two output-shaping flip-flops, two inverter output drivers, three 5.5-V zener diodes (providing transient protection at 16.5 V), and input inverters for use in a crystal oscillator. The CD4045A configuration provides 21 flip-flop counting stages, and two flip-flops for shaping the output waveform for a 3.125% duty cycle. Push-pull operation is provided by the inverter output drivers.

The first inverter is intended for use as a crystal oscillator/amplifier. However, it may be used as a normal logic inverter if desired. A crystal oscillator circuit can be made less sensitive to voltage-supply variations by the use of source resistors. In this device, the sources of the p and n transistors have been brought out to package terminals. If external resistors are not required, the sources must be shorted to their respective substrates (S_p to V_{DD}, S_n to V_{SS}). See Fig. 3.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

- **Digital equipment in which ultra-low dissipation and/or operation using a battery source are primary design requirements.**
- **Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs at various intervals in the counting sequence.**
- **Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.**



CD4045A FUNCTIONAL DIAGRAM

Features:

- **Microwatt quiescent dissipation . . . . . .**
  2.5 µW (typ.) @ V_{DD} = 5 V;
  10 µW (typ.) @ V_{DD} = 10 V
- **Very low operating dissipation . . . . . .**
  1 mW (typ.); @ V_{DD} = 5 V, fφ = 1 MHz
- **Output drivers with sink or source capability . . . . . .**
  7 mA (typ.) @ V_O = 0.5 V, V_{DD} = 5 V (sink)
  5 mA (typ.) @ V_O = 4.5 V, V_{DD} = 5 V (source)
- **Medium speed (typ.) . . . . .**
  fφ = 5 MHz @ V_{DD} = 5 V
  fφ = 10 MHz @ V_{DD} = 10 V
- **16.5 V zener diode transient protection on chip for automotive use**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 µA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . –65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, H . . . . –55 to +125°C

PACKAGE TYPE E . . . . –40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . –0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = –40 to +60°C (PACKAGE TYPE E) . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = –55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . –0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	VDD (V)	LIMITS D,F,H Packages Min.	Max.	E Package Min.	Max.	UNITS
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V
Input-Pulse Width, t_W	5 10	115 60	– –	140 75	– –	ns
Input-Pulse Frequency, fφ	5 10	dc dc	4.4 8.5	dc dc	3.5 6.5	MHz
Input-Pulse Rise or Fall Time, $t_{r\phi}$, $t_{f\phi}$	5 10	– –	15 10	– –	15 10	µs

NOTE 1: To minimize power dissipation in the zener diodes, and to ensure device dissipation less than 200 mW, a 150 Ω current-limiting resistor must be placed in series with the power supply for V_{DD} > 13 V.

NOTE 2: Observe power-supply terminal connections, V_{DD} is terminal No. 3 and V_{SS} is terminal No. 14 (not 16 and 8 respectively, as in all other CD4000A Series 16-lead devices).

CD4045A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		D,F,H Packages			E Package			
	V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time: ϕ to y or y+d out t_{PLH}, t_{PHL}	5	–	2.2	4.4	–	2.2	5.5	μs
	10	–	1.2	2.4	–	1.2	3.3	
Transition Time: t_{THL}, t_{TLH}	5	–	450	800	–	450	900	ns
	10	–	375	650	–	375	750	
Maximum Input-Pulse Frequency, $f_{m\phi}$	5	4.4	5	–	3.5	5	–	MHz
	10	8.5	10	–	6.5	10	–	
Minimum Input-Pulse Width, t_W	5	–	100	115	–	100	140	ns
	10	–	50	60	–	50	75	
Input-Pulse Rise & Fall Time; $t_r\phi$, $t_f\phi$	5 10	– –	– –	15 10	– –	– –	15 10	μs
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

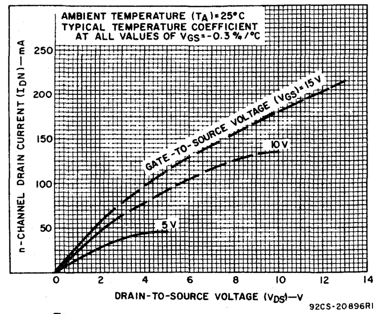


Fig. 1 – Typical output n-channel drain characteristics.

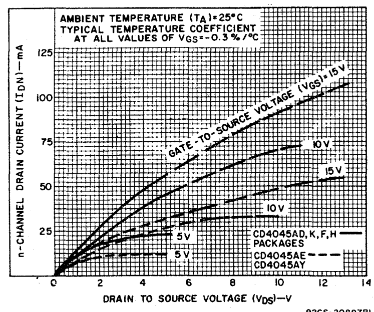


Fig. 2 – Minimum output n-channel drain characteristcs.

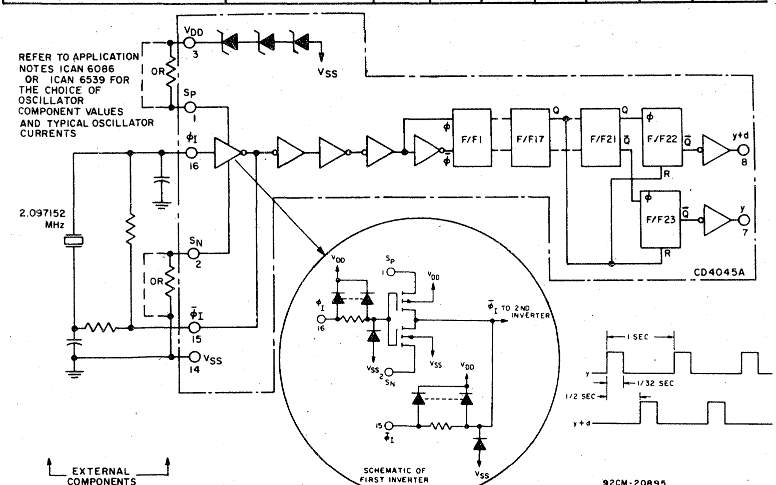


Fig. 3 – CD4045A and outboard components in a typical 21-stage counter application.

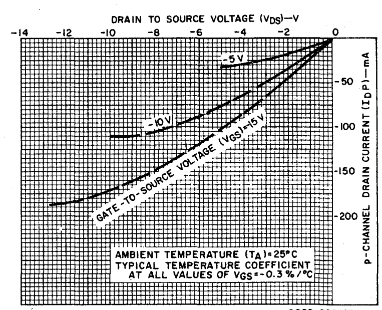


Fig. 4 – Typical output p-channel drain characteristics.

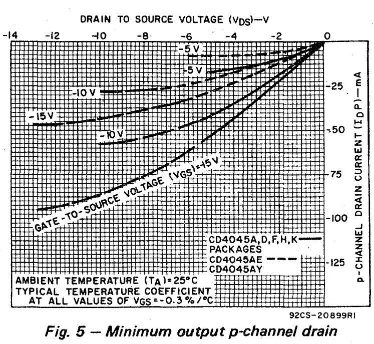


Fig. 5 – Minimum output p-channel drain characteristics.

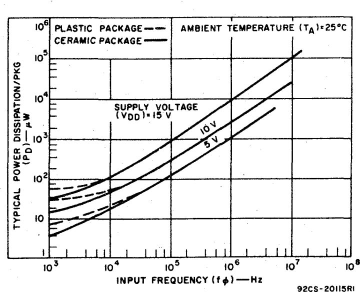


Fig. 6 – Typical dissipation vs input frequency (21 counting stages).

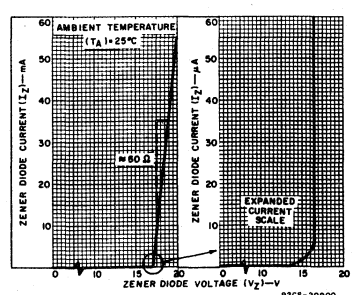


Fig. 7 – Typical zener diode characteristics.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,F,H Packages				*E Package*				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	+25 Typ.	+25 Limit	+125	–40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	15	0.5	15	900	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) I_DN Min.	0.5	–	5	4.4	7	3.5	2.5	2.2	7	1.8	1.3	mA
	0.5	–	10	6.9	11	5.5	3.9	3.5	11	2.8	2	
p-Channel (Source): I_DP Min.	4.5	–	5	–3.1	–5	–2.5	–1.8	–1.6	–5	–1.3	–0.9	
	9.5	–	10	–5.6	–9	–4.5	–3.2	–2.8	–9	–2.3	–1.6	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm10^{-5}$ Typ., ±1 Max.								μA
Zener Breakdown Voltage, $V_{(BR)Z}$	1–100 μA		Min.	13.3	–	13.5	13.7	13.3	–	13.5	13.6	V
			Typ.	–	16.5	–	–	–	16.5	–	–	
			Max.	17.8	–	18	18.2	17.8	–	18	18.1	

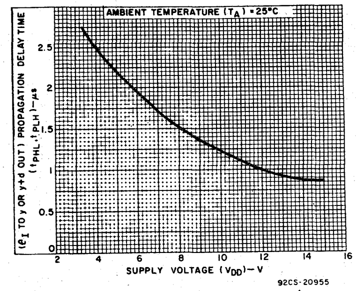


Fig. 8 – Typical propagation delay (ϕ_1 to y or y+d out) vs V_{DD}.

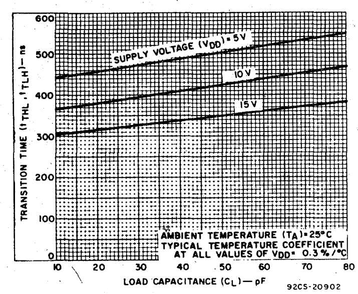


Fig. 9 – Typical transition time vs C_L.

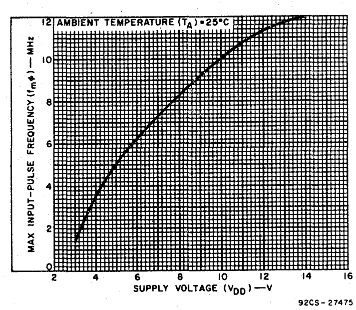


Fig. 10 – Typical maximum input-pulse frequency.

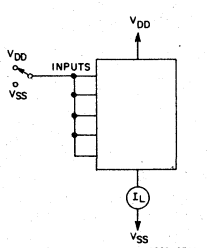


Fig. 11 – Quiescent-device-current test circuit.

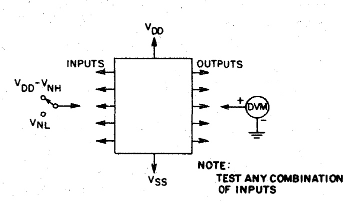


Fig. 12 – Noise-immunity test circuit.

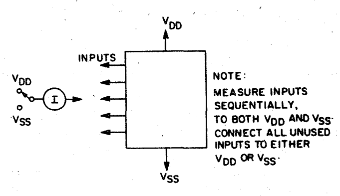


Fig. 13 – Input-leakage-current test circuit.

CD4046A Types

COS/MOS Micropower Phase-Locked Loop

The RCA-CD4046A COS/MOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2-V zener diode is provided for supply regulation if necessary.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\Omega$) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R_S) of 10 kΩ or more should be connected from this terminal to V_{SS}. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full COS/MOS logic swing is available at the output of the VCO and allows direct coupling to COS/MOS frequency dividers such as the RCA-CD4024, CD4018, CD4020, CD4022, CD4029, and CD4059. One or more CD4018 (Presettable Divide-by-N Counter) or CD4029 (Presettable Up/Down Counter), or CD4059A (Programmable Divide-by-"N" Counter), together with the CD4046A (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within COS/MOS logic levels [logic "0" ≤30% ($V_{DD}-V_{SS}$), logic "1" ≥ 70% ($V_{DD}-V_{SS}$)]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase comparator I is an exclusive-OR network; it operates analagously to an over-driven balanced mixer. To maximize the lock range, the signal- and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_o).

The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ($2f_c$).

The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2f_L$). The capture range is ≤ the lock range.

With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. 2 shows the typical, triangular, phase-to-output response characteristic

Features:

- **Very low power consumption: 70 μW (typ.) at VCO f_o = 10 kHz, V_{DD} = 5 V**
- **Operating frequency range up to 1.2 MHz (typ.) at V_{DD} = 10 V**
- **Wide supply-voltage range: $V_{DD} - V_{SS}$ = 5 to 15 V**
- **Low frequency drift: 0.06%/°C (typ.) at V_{DD} = 10 V**
- **Choice of two phase comparators:**
  1. **Exclusive-OR network**
  2. **Edge-controlled memory network with phase-pulse output for lock indication**
- **High VCO linearity: 1% (typ.)**
- **VCO inhibit control for ON-OFF keying and ultra-low standby power consumption**
- **Source-follower output of VCO control input (Demod. output)**
- **Zener diode to assist supply regulation**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**

Applications:

- **FM demodulator and modulator**
- **Frequency synthesis and multiplication**
- **Frequency discriminator**
- **Data synchronization**
- **Voltage-to-frequency conversion**
- **Tone decoding**
- **FSK – Modems**
- **Signal conditioning**
- **(See ICAN-6101) "RCA COS/MOS Phase-Locked Loop – A Versatile Building Block for Micropower Digital and Analog Applications"**

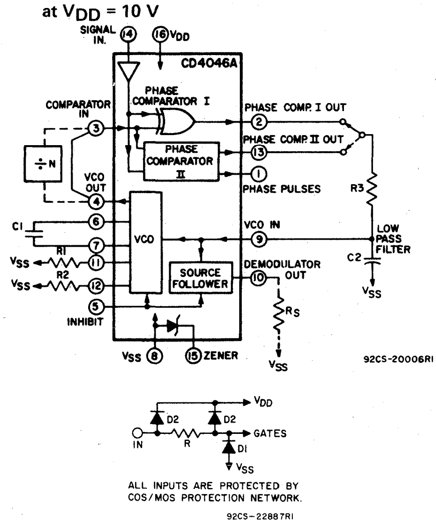


Fig.1 – COS/MOS phase-locked loop block diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

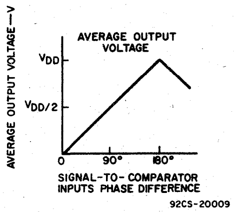


Fig.2 — Phase-comparator I characteristics at low-pass filter output.

of phase-comparator I. Typical waveforms for a COS/MOS phase-locked-loop employing phase comparator I in locked condition of f_o is shown in Fig. 3.

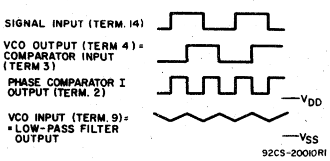


Fig.3 — Typical waveforms for COS/MOS phase-locked loop employing phase comparator I in locked condition of f_o.

Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal- and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS Min.	LIMITS Max.	UNITS
Supply Voltage Range (For T_A = Full Package Temperature Range	3	12	V

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristic	Test Conditions	V_O Volts	V_{DD} Volts	Limits All Package Types D,E,F,H Min.	Typ.	Max.	Units
Phase Comparator Section							
Operating Supply Voltage, $V_{DD}-V_{SS}$	VCO Operation		–	5	–	15	V
	Comparators only		–	3	–	15	
Total Quiescent Device Current, I_L: Term. 14 Open	Term. 15 open, Term. 5 at V_{DD}, Terms. 3 & 9 at V_{SS}		5	–	25	55	µA
			10	–	200	410	
Term. 14 at V_{SS} or V_{DD}			5	–	5	15	
			10	–	25	60	
			15	–	50	500	
Term. 14 (SIGNAL IN) Input Impedance, Z_{14}			5	1	2	–	MΩ
			10	0.2	0.4	–	
			15	–	0.2	–	
AC-Coupled Signal Input Voltage Sensitivity* (peak-to-peak)	See Fig.7		5	–	200	400	mV
			10	–	400	800	
			15	–	700	–	
DC-Coupled Signal Input and Comparator Input Voltage Sensitivity Low Level			5	1.5	2.25	–	V
			10	3	4.5	–	
			15	4.5	6.75	–	
High Level		V_O Volts	5	–	2.75	3.5	
			10	–	5.5	7	
			15	–	8.25	–	
Output Drive Current: n-Channel (Sink), I_{DN}	Phase Comparator I & II Term. 2 & 13	0.5	5	0.43	0.86	–	mA
		0.5	10	1.3	2.5	–	
	Phase Pulses	0.5	5	0.23	0.47	–	
		0.5	10	0.7	1.4	–	
p-Channel (Source), I_{DP}	Phase Comparator I & II Term. 2 & 13	4.5	5	−0.3	−0.6	–	
		9.5	10	−0.9	−1.8	–	
	Phase Pulses	4.5	5	−0.08	−0.16	–	
		9.5	10	−0.25	−0.5	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		15	–	$\pm10^{-5}$	±1	µA

* For sine wave, the frequency must be greater than 1 kHz for Phase Comparator II.

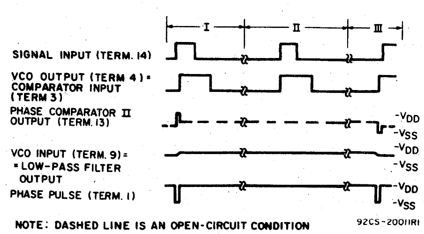


Fig.4 — Typical waveforms for COS/MOS phase-locked loop employing phase comparator II in locked condition.

CD4046A Types

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

Characteristic	Test Conditions	V_O Volts	V_{DD} Volts	Limits – All Package Types D,E,F,H – Min.	Typ.	Max.	Units
VCO Section							
Operating Supply Voltage $V_{DD}-V_{SS}$	As fixed oscillator only			3	–	15	V
	Phase-lock-loop operation			5	–	15	
Operating Power Dissipation, P_D	$f_o = 10$ kHz, $R_1 = 1$ MΩ, $R_2 = \infty$, $VCO_{IN} = \frac{V_{DD}}{2}$		5	–	70	–	μW
			10	–	600	–	
			15	–	2400	–	
Maximum Operating Frequency, f_{max}	R1 = 10 kΩ, $R_2 = \infty$, $VCO_{IN} = V_{DD}$, C1 = 100 pF		5	0.25	0.5	–	MHz
	C1 = 50 pF		10	0.6	1.2	–	
			15	–	1.5	–	
Center Frequency (f_o) and Frequency Range, $f_{max}-f_{min}$	Programmable with external components R1, R2, and C1 *See Design Information*						
Linearity	VCO_{IN} = 2.5 V ± 0.3 V, R1 > 10 kΩ		5	–	1	–	%
	= 5 V ± 2.5 V, R1 > 400 kΩ		10	–	1	–	
	= 7.5 V ± 5 V, R1 = 1 MΩ		15	–	1	–	
Temperature-Frequency Stability•: No Frequency Offset $f_{MIN} = 0$	$\%/^oC \propto \frac{1}{f \cdot V_{DD}}$, $R_2 = \infty$		5	–	0.12–0.24	–	%/°C
			10	–	0.04–0.08	–	
			15	–	0.015–0.03	–	
Frequency Offset $f_{MIN} \neq 0$	$\%/^oC \propto \frac{1}{f.V_{DD}}$		5	–	0.06–0.12	–	
			10	–	0.05–0.1	–	
			15	–	0.03–0.06	–	
Input Resistance of VCO_{IN} (Term 9), R_I			5,10,15	–	10^{12}	–	Ω
VCO Output Voltage (Term 4) Low Level, V_{OL}	Driving COS/MOS-Type Load (e.g. Term 3 Phase Comparator Input)		5,10,15	–	–	0.01	V
High Level, V_{OH}			5	4.99	–	–	
			10	9.99	–	–	
			15	14.99	–	–	
VCO Output Duty Cycle			5,10,15	–	50	–	%
VCO Output Transition Times, t_{THL}, t_{TLH}			5	–	75	150	ns
			10	–	50	100	
			15	–	40	–	
VCO Output Drive Current: n-Channel (Sink), I_{DN}		0.5	5	0.43	0.86	–	mA
		0.5	10	1.3	2.6	–	
p-Channel (Source), I_{DP}		4.5	5	–0.3	–0.6	–	
		9.5	10	–0.9	–1.8	–	
Source-Follower Output (Demodulated Output): Offset Voltage ($VCO_{IN}-V_{DEM}$)	$R_S > 10$ kΩ		5,10	–	1.5	2.2	V
			15	–	1.5	–	
Linearity	$R_S > 50$kΩ, VCO_{IN} = 2.5±0.3 V		5	–	0.1	–	%
	= 5±2.5 V		10	–	0.6	–	
	= 7.5±5 V		15	–	0.8	–	
Zener Diode Voltage (V_Z)	$I_Z = 50$ μA			4.5	5.2	6.1	V
Zener Dynamic Resistance, R_Z	$I_Z = 1$ mA			–	100	–	Ω

• Positive coefficient.

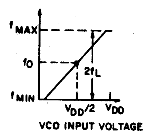
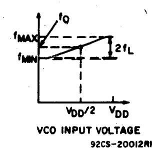
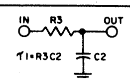
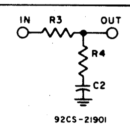
Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. 4 shows typical waveforms for a COS/MOS PLL employing phase comparator II in a locked condition.

DESIGN INFORMATION

This information is a guide for approximating the values of external components for the CD4046A in a Phase-Locked-Loop system. The selected external components must be within the following ranges:

$10\ k\Omega \leq R1, R2, R_S \leq 1\ M\Omega$
$C1 \geq 100$ pF at $V_{DD} \geq 5$ V;
$C1 \geq 50$ pF at $V_{DD} \geq 10$ V

In addition to the given design information refer to Fig.5 for R1, R2, and C1 component selections.

Characteristics	Phase Comparator Used	Design Information: VCO WITHOUT OFFSET $R_2 = \infty$	Design Information: VCO WITH OFFSET
VCO Frequency	1		
	2	Same as for No.1	
For No Signal Input	1	VCO will adjust to center frequency, f_o	
	2	VCO will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2\ f_L$	1	$2\ f_L$ = full VCO frequency range	
		$2\ f_L = f_{max} - f_{min}$	
	2	Same as for No.1	
Frequency Capture Range, $2\ f_C$	1		(1), (2) $2\,f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau 1}}$
Loop Filter Component Selection			For $2\ f_C$, see Ref. (2)
	2	$f_C = f_L$	
Phase Angle Between Signal and Comparator	1	90° at center frequency (f_o) approximating 0° and 180° at ends of lock range ($2\ f_L$)	
	2	Always 0° in lock	

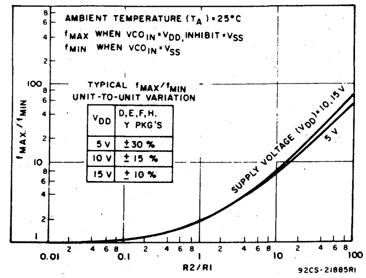


Fig.5(c) — Typical f_{max}/f_{min} vs R2/R1.

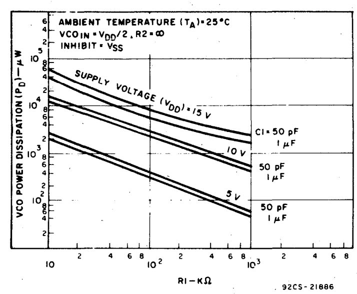


Fig.6(a) — Typical VCO power dissipation at center frequency vs R1.

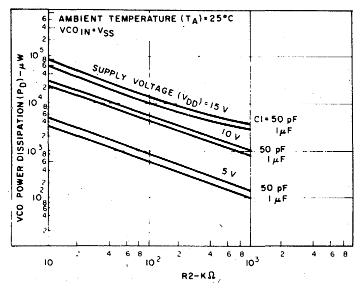


Fig.6(b) — Typical VCO power dissipation at f_{min} vs R2.

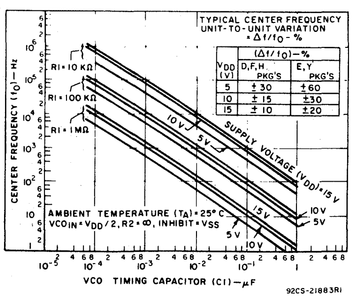


Fig.5(a) — Typical center frequency vs C1 for R1 = 10 kΩ, and 1 MΩ and f_o ~ 1/R1 C1.

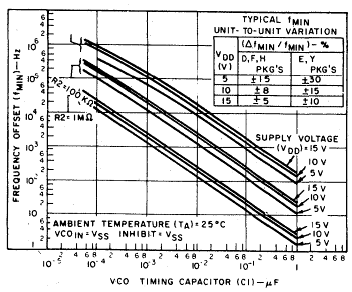


Fig.5(b) — Typical frequency offset vs C1 for R2 = 10 kΩ, 100 kΩ, and 1 MΩ.

NOTE: Lower frequency values are obtainable if larger values of C1 than shown in Figs. 5(a) and 5(b) are used.

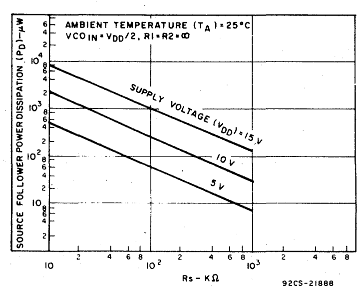


Fig.6(c) — Typical source follower power dissipation vs R_S.

NOTE: To obtain approximate total power dissipation of PLL system for no-signal input

P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S) — Phase Comparator I

P_D (Total) = P_D (f_{MIN}) — Phase Comparator II

DESIGN INFORMATION (Cont'd):

Characteristics	Phase Comparator Used	Design Information	
Locks On Harmonic of Center Frequency	1	Yes	
	2	No	
Signal Input Noise Rejection	1	High	
	2	Low	
		VCO WITHOUT OFFSET $R_2 = \infty$	**VCO WITH OFFSET**
VCO Component Selection	1	– Given: f_o – Use f_o with Fig.5a to determine R1 and C1	– Given: f_o and f_L – Calculate f_{min} from the equation $f_{min} = f_o - f_L$ – Use f_{min} with Fig.5b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1
	2	– Given: f_{max} – Calculate f_o from the equation $f_o = \frac{f_{max}}{2}$ –Use f_o with Fig.5a to determine R1 and C1	– Given: f_{min} & f_{max} – Use f_{min} with Fig.5b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1

For further information, see

(1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York, 1966

(2) G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

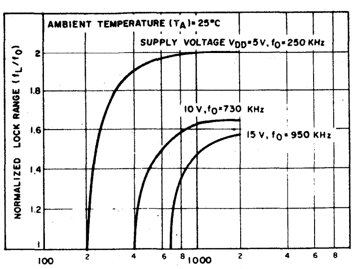


Fig.7 – Typical lock range vs signal input amplitude.

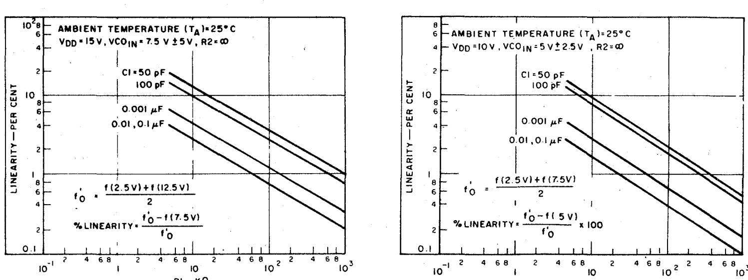


Fig.8(a) and (b) – Typical VCO linearity vs R1 and C1.

COS/MOS Low-Power Monostable/Astable Multivibrator

The RCA-CD4047A consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options.

Inputs include +TRIGGER, −TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER, and EXTERNAL RESET. Buffered outputs are Q, $\overline{\text{Q}}$, and OSCILLATOR. In all modes of operation an external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.

Astable operation is enabled by a high level on the ASTABLE input. The period of the square wave at the Q and $\overline{\text{Q}}$ Outputs in this mode of operation is a function of the external components employed. "True" input pulses on the ASTABLE input or "Complement" pulses on the $\overline{\text{ASTABLE}}$ input allow the circuit to be used as a gatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output.

In the monostable mode, positive-edge triggering is accomplished by application of a leading-edge pulse to the +TRIGGER input and a low level to the −TRIGGER input. For negative-edge triggering, a trailing-edge pulse is applied to the −TRIGGER and a high level is applied to the +TRIGGER. Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading edge only) by applying a common pulse to both the RETRIGGER and +TRIGGER inputs. In this mode the output pulse remains high as long as the input pulse period is shorter than the period determined by the RC components.

An external countdown option can be implemented by coupling "Q" to an external "N" counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator.

A high level on the EXTERNAL RESET input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time. In the monostable mode, a high-level or power-on reset pulse, must be applied to the EXTERNAL RESET whenever V_{DD} is applied.

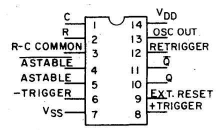
These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **Low power consumption: special COS/MOS oscillator configuration**
- **Monostable (one-shot) or astable (free-running) operation**
- **True and complemented buffered outputs**
- **Only one external R and C required**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Monostable Multivibrator Features:

- **Positive- or negative-edge trigger**
- **Output pulse width independent of trigger pulse duration**
- **Retriggerable option for pulse width expansion**
- **Long pulse widths possible using small RC components by means of external counter provision**
- **Fast recovery time essentially independent of pulse width**
- **Pulse-width accuracy maintained at duty cycles approaching 100%**



CD4047A
Terminal Diagram

Astable Multivibrator Features:

- **Free-running or gatable operating modes**
- **50% duty cycle**
- **Oscillator output available**
- **Good astable frequency stability:**
  Frequency deviation:
  =±2% + 0.03%/°C @ 100 kHz
  =±0.5% + 0.015%/°C @ 10 kHz
  (circuits "trimmed" to frequency V_{DD} = 10 V ± 10%)

Applications :

Digital equipment where low-power dissipation and/or high noise immunity are primary design requirements:

- **Envelope detection**
- **Frequency multiplication**
- **Frequency division**
- **Frequency discriminators**
- **Timing circuits**
- **Time-delay applications**

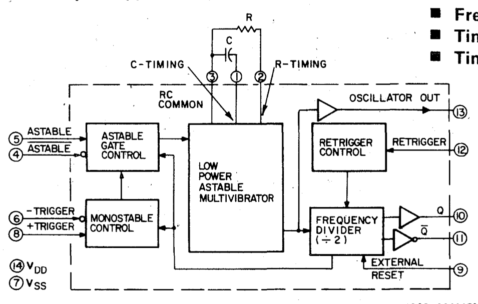


Fig. 1 – CD4047A logic block diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A= −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
FOR T_A= +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A= −55 to +100°C (PACKAGE TYPES D, F) . . . . . 500 mW
FOR T_A= +100 to +125°C (PACKAGE TYPES D, F) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A= FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

CD4047A Types

RECOMMENDED OPERATING CONDITIONS at T_A= 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD}	LIMITS D,F,H Packages Min.	D,F,H Packages Max.	E Package Min.	E Package Max.	UNITS
Supply-Voltage Range (For T_A=Full Package- Temperature Range)		3	12	3	12	V
Input Pulse Width, t_W (Any Input)	5 10	1000 400	– –	1300 600	– –	ns
Trigger, Retrigger Rise or Fall Time, t_r , t_f	5 10	– –	15 5	– –	15 5	μs

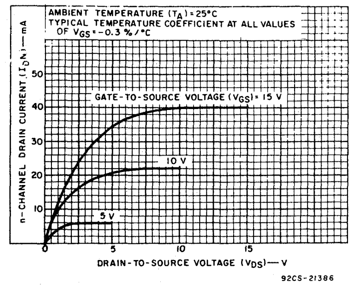


Fig. 2 – Typical output n-channel drain characteristics for Q and $\bar{Q}$ buffers.

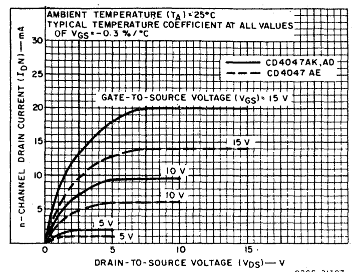


Fig. 3 – Minimum output n-channel drain characteristics for Q and $\bar{Q}$ buffers.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics	Conditions V_O (V)	V_{IN} (V)	V_{DD} (V)	D,F,H Packages –55	+25 Typ.	+25 Limit	+125	E Package - 40	+25 Typ.	+25 Limit	+85	Units
Quiescent Device Current I_L Max.	–	–	5	5	0.03	5	300	50	0.1	50	700	μA
	–	–	10	10	0.05	10	600	100	0.2	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min., 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5		5	1 Min.								V
	9		10	1 Min.								
Inputs High, V_{NMH}	0.5		5	1 Min.								
	1		10	1 Min.								
Output Drive Current: (Q,$\bar{Q}$ Outputs) n-channel (Sink), I_DN Min.	0.5	–	5	0.5	0.8	0.4	0.28	0.34	0.8	0.28	0.23	mA
	0.5	–	10	1.25	2	1	0.7	0.85	2	0.7	0.6	
p-Channel (Source): I_DP Min.	4.5	–	5	-0.5	-0.8	-0.4	-0.28	-0.34	-0.8	-0.28	-0.23	
	9.5	–	10	-1.25	-2	-1	-0.7	-0.85	-2	-0.7	-0.6	
Input Leakage Current, I_{IL},I_{IH}	Any Input –	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

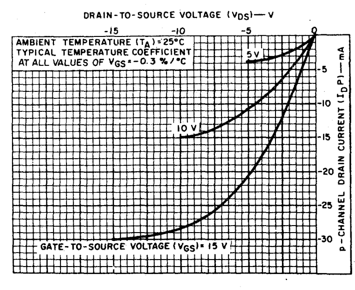


Fig. 4. – Typical output p-channel drain characteristics for Q and $\bar{Q}$ buffers.

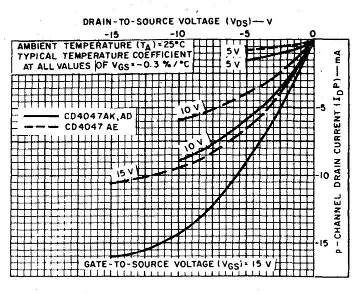


Fig. 5 – Minimum output p-channel drain characteristics for Q and $\bar{Q}$ buffers.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$, Input t_r, t_f = 20 ns, C_L = 15 pF, $R_L = 200\ k\Omega$

CHARACTERISTICS	TEST CONDITIONS V_{DD} (Volts)	LIMITS D,F,H Packages Min.	TYP.	MAX.	LIMITS E Package MIN.	TYP.	MAX.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} Astable, $\overline{Astable}$ to Osc. Out	5	–	200	400	–	200	550	ns
	10	–	100	200	–	100	275	
Astable, $\overline{Astable}$ to Q, $\overline{Q}$	5	–	550	900	–	550	1200	
	10	–	250	500	–	250	650	
+Trigger, −Trigger to Q, $\overline{Q}$	5	–	700	1200	–	700	1600	
	10	–	300	600	–	300	800	
+Trigger, Retrigger to Q, $\overline{Q}$	5	–	300	600	–	300	800	
	10	–	175	300	–	175	400	
External Reset to Q, $\overline{Q}$	5	–	300	600	–	300	800	
	10	–	125	250	–	125	350	
Transition Time: t_{THL}, t_{TLH} Q, $\overline{Q}$	5	–	75	125	–	75	150	ns
	10	–	45	75	–	45	100	
Osc. Out	5	–	75	150	–	75	180	
	10	–	45	100	–	45	130	
Minimum Input Pulse Width (any input), t_W*	5	–	500	1000	–	500	1300	ns
	10	–	200	400	–	200	600	
+Trigger, Retrigger Rise & Fall Time, t_r, t_f	5	–	–	15	–	–	15	μs
	10	–	–	5	–	–	5	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

* Input pulse widths below the minimum specified may cause malfunction of the unit. See Application Note ICAN - 6230

CD4047A FUNCTIONAL TERMINAL CONNECTIONS
NOTE: IN ALL CASES EXTERNAL RESISTOR BETWEEN TERMINALS 2 AND 3▲
EXTERNAL CAPACITOR BETWEEN TERMINALS 1 AND 3▲

FUNCTION	TERMINAL CONNECTIONS TO V_{DD}	TO V_{SS}	INPUT PULSE TO	OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
Astable Multivibrator:					
Free Running	4,5,6,14	7,8,9,12	–	10,11,13	t_A(10,11)=4.40 RC
True Gating	4,6,14	7,8,9,12	5	10,11,13	t_A(13)=2.20 RC
Complement Gating	6,14	5,7,8,9,12	4	10,11,13	
Monostable Multivibrator:					
Positive-Edge Trigger	4,14	5,6,7,9,12	8	10,11	t_M(10,11)=2.48 RC
Negative-Edge Trigger	4,8,14	5,7,9,12	6	10,11	
Retriggerable	4,14	5,6,7,9	8,12	10,11	
External Countdown*	14	5,6,7,8,9,12	–	10,11	

* Input Pulse to Reset of External Counting Chip External Counting Chip Output To Terminal 4 ▲ See Text.

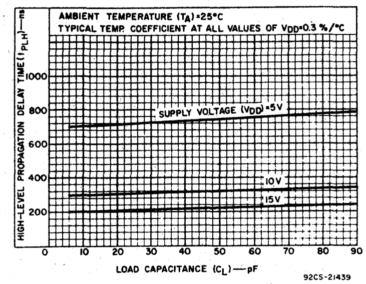


Fig. 6 – Typical low-to-high level propagation delay time vs load capacitance for Q and $\overline{Q}$ buffers.

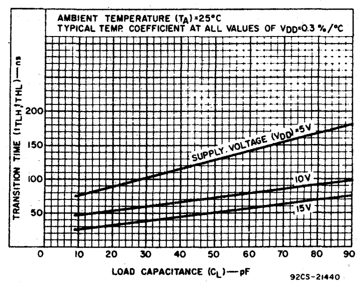


Fig. 7 – Typical transition time vs load capacitance for Q and $\overline{Q}$ buffers.

I. Astable Mode Design Information

A. Unit-to-Unit Transfer-Voltage Variations.

The following analysis presents worst-case variations from unit to unit as a function of transfer-voltage (V_{TR}) shift (33%–67% V_{DD}) for free-running (astable) operation.

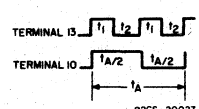


Fig. 8 – Astable mode waveforms.

$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

$$t_A = 2(t_1 + t_2)$$

$$= -2\ RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})}$$

Typ: $V_{TR} = 0.5\ V_{DD}$ $t_A = 4.40\ RC$
Min: $V_{TR} = 0.33\ V_{DD}$ $t_A = 4.62\ RC$
Max: $V_{TR} = 0.67\ V_{DD}$ $t_A = 4.62\ RC$

thus if $\boxed{t_A = 4.40\ RC}$ is used, the maximum variation will be (+5.0%,–0.0%).

CD4047A Types

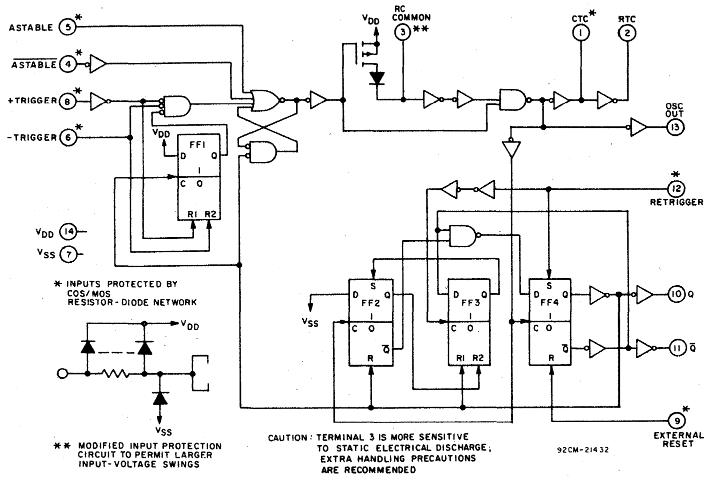


Fig. 9 – CD4047A logic diagram.

B. Variations Due to V_{DD} and Temperature Changes

In addition to variations from unit to unit, the astable period may vary as a function of frequency with respect to V_{DD} and temperature. Typical variations are presented in graphical form in Figs. 10 to 20 with 10 V as reference for voltage variation curves and 25°C as reference for temperature variation curves.

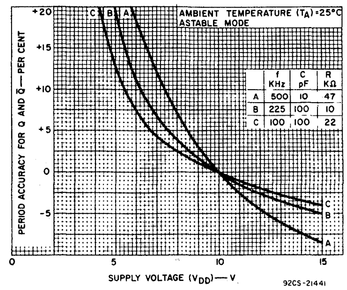


Fig. 10 – Typical Q-and-Q̄-period accuracy vs supply voltage (high frequency).

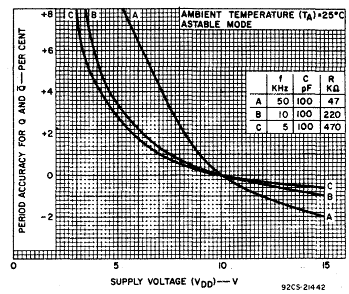


Fig. 11 – Typical Q-and-Q̄-period accuracy vs supply voltage (medium frequency)

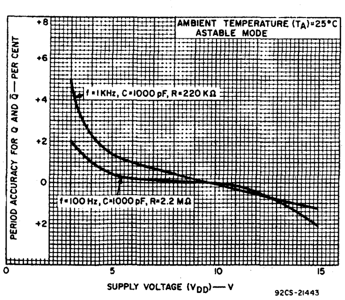


Fig. 12 – Typical Q-and-Q̄-period accuracy vs supply voltage (low frequency).

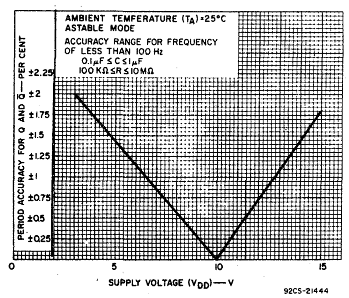


Fig. 13 – Typical Q-and-Q̄- period accuracy vs supply voltage (very low frequency).

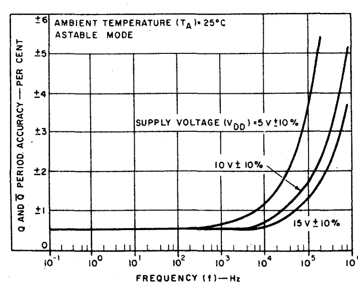


Fig. 14 – Typical Q-and Q̄-period accuracy vs frequency for V_{DD} variation of ±10% from value indicated.

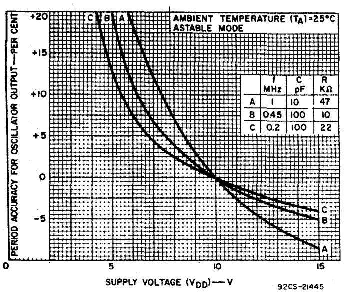


Fig. 15 – Typical oscillator-output-period accuracy vs supply voltage (high frequency).

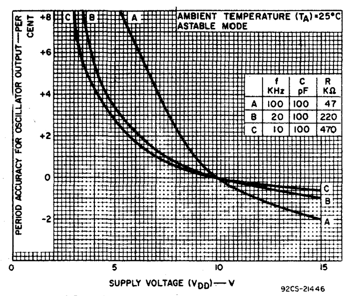


Fig. 16 – Typical oscillator-output-period accuracy vs supply voltage (medium frequency).

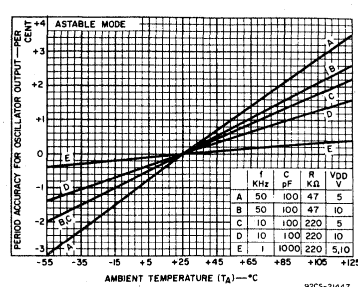


Fig. 17 – Typical Q- and Q̄-period accuracy vs temperature (medium frequency).

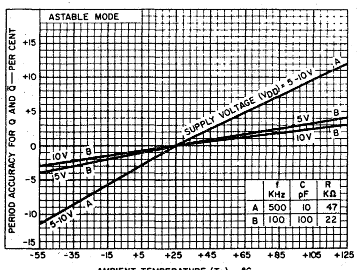


Fig. 18 – Typical Q- and Q̄-period accuracy vs temperature (high frequency).

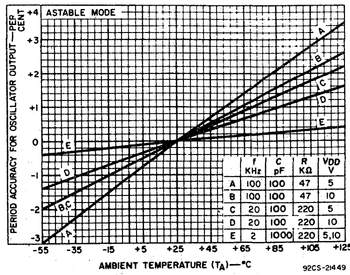


Fig. 19 – Typical oscillator-period accuracy vs temperature (medium frequency).

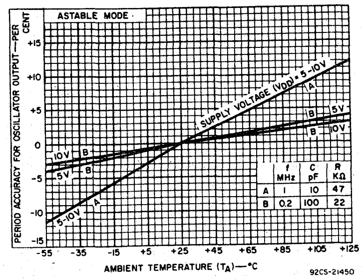


Fig. 20 – Typical oscillator-period accuracy vs temperature (high frequency).

II. Monostable Mode Design Information

The following analysis presents worst-case variations from unit to unit as a function of transfer-voltage (V_{TR}) shift (33% – 67% V_{DD}) for one-shot (monostable) operation.

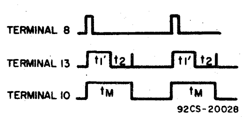


Fig. 21 – Monostable waveforms.

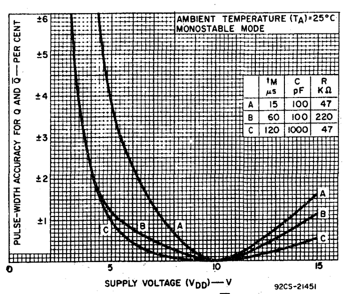


Fig. 22 – Typical Q- and Q̄-pulse-width accuracy vs supply voltage (t_M = 15, 60, 120 µs).

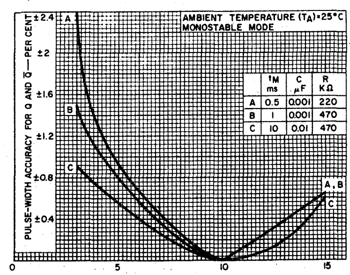


Fig. 23 – Typical Q- and Q̄-pulse-width accuracy vs supply voltage (t_M = 0.5, 1, 10 ms).

$$t_1' = -RC \ln \frac{V_{TR}}{2V_{DD}}$$

$$t_M = (t_1' + t_2)$$

$$t_M = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})(2V_{DD})}$$

where t_M = Monostable mode pulse width. Values for t_M are as follows:

Typ:	$V_{TR} = 0.5\ V_{DD}$	$t_M = 2.48\ RC$
Min:	$V_{TR} = 0.33\ V_{DD}$	$t_M = 2.71\ RC$
Max.	$V_{TR} = 0.67\ V_{DD}$	$t_M = 2.48\ RC$

Thus if $\boxed{t_M = 2.48\ RC}$ is used, the maximum variation will be (+9.3%, –0.0%).

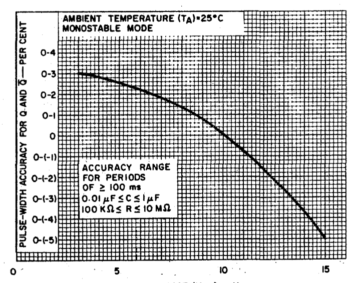


Fig. 24 – Typical Q- and Q̄-pulse-width accuracy vs supply voltage ($t_M \geqslant$ 100 ms).

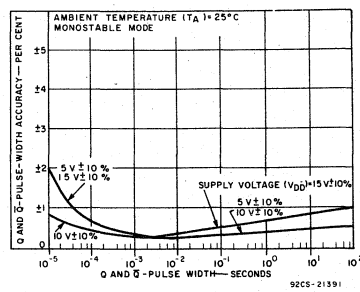


Fig. 25 – Typical Q- and Q̄ pulse-width accuracy vs Q and Q̄ pulse width for a variation of ±10% from value indicated.

Note:

In the astable mode, the first positive half cycle has a duration of T_M; succeeding durations are $t_A/2$.

In addition to variations from unit to unit, the monostable pulse width may vary as a function of frequency with respect to V_{DD} and temperature. These variations are presented in graphical form in Fig. 22 to 27 with 10 V as reference for voltage-variation curves and 25°C as reference for temperature-variation curves.

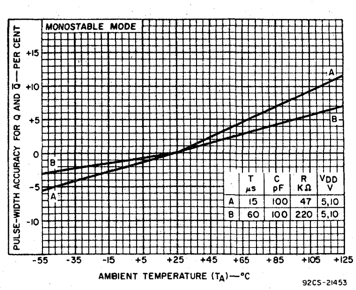


Fig. 26 – Typical Q and Q̄ pulse-width accuracy vs temperature (high frequency).

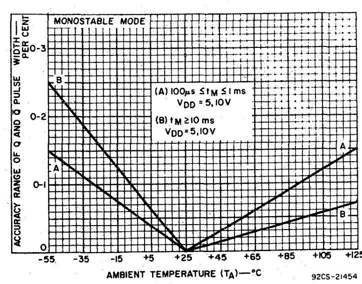


Fig. 27 – Typical Q and Q̄ pulse-width accuracy range vs temperature.

III. Retrigger Mode Operation

The CD4047A can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminals 8 and 12, and the output is taken from terminal 10 or 11. As shown in Fig. 28, normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied. For two input pulses, $t_{RE}=t_1' + t_1 + 2t_2$. For more than two pulses, t_{RE} (Q OUTPUT), terminates at some variable time, t_D, after the termination of the last retrigger pulse, t_D is variable because t_{RE} (Q OUTPUT) terminates after the second positive edge of the oscillator output appears at flip-flop 4 (see Fig. 8).

IV. External Counter Option

Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Fig. 29. The pulse duration at the output is

$$t_{ext} = (N-1)(t_A) + (t_M + t_A/2)$$

where t_{ext}= pulse duration of the circuitry, and N is the number of counts used.

V. Timing-Component Limitations

The capacitor used in the circuit should be non-polarized and have low leakage(i.e. the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used). There is no upper or lower limit for either R or C value to maintain oscillation.

However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the COS/MOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted.

The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be:

$C \geqslant 100$ pF, up to any practical value, for astable modes;

$C \geqslant 1000$ pF, up to any practical value for monostable modes.

$10\ k\Omega \leqslant R \leqslant 1\ M\Omega$

VI. Power Consumption

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formulae:

Astable Mode: $P = 2CV^2f$. (Output at terminal No. 13)
$P = 4CV^2f$. (Output at terminal Nos. 10 and 11)

Monostable Mode:

$$P = \frac{(2.9CV^2)\ (\text{Duty Cycle})}{T}$$

(Output at terminal Nos. 10 and 11)

The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.

Because the power dissipation does not depend on R, a design for minimum power dissipation would be a small value of C. The value of R would depend on the desired period (within the limitations discussed above). See Figs. 30–32 for typical power consumption in astable mode.

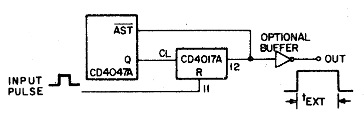


Fig. 28 – Implementation of external counter option.

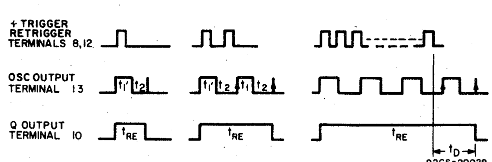


Fig. 29 – Retrigger-mode waveforms.

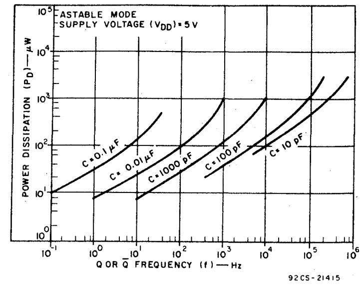


Fig. 30 – Power dissipation vs output frequency (V_{DD} = 5 V).

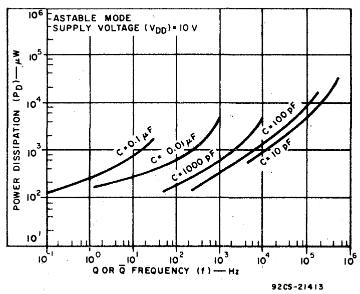


Fig. 31 – Power dissipation vs output frequency (V_{DD} = 10 V).

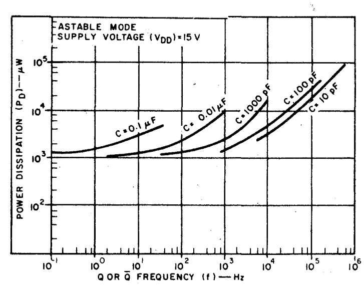


Fig. 32 – Power dissipation vs output frequency (V_{DD} = 15 V).

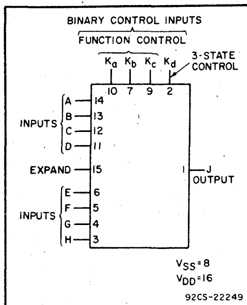
COS/MOS Multi-Function Expandable 8-Input Gate

The RCA-CD4048A is an 8-input gate having four control inputs. Three binary control inputs – Ka, Kb, and Kc – provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR, and AND/NOR.

A fourth control input –Kd – provides the user with 3-state outputs. When control input Kd is high the output is either a logic 1 or a logic 0 depending on the input states. When control input Kd is low, the output is an open circuit. This feature enables the user to connect this device to a common bus line.

In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs to one CD4048A, (see Fig. 6). For example, two CD4048A's can be cascaded to provide a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to V_{SS}.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4048A Functional Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A= –40 to +60°C (PACKAGE TYPE E) . . . . . . 500 mW
FOR T_A= +60 to +85°C (PACKAGE TYPE E) . . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A= –55 to +100°C (PACKAGE TYPES D, F) . . . . . . 500 mW
FOR T_A= +100 to +125°C (PACKAGE TYPES D, F) . . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A= FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . . +265°C

Features:

- **Medium-power TTL drive capability**
- **Three-state output**
- **High current source and sink capability 9 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 10 V**
- **Many logic functions available in one package**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 µA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

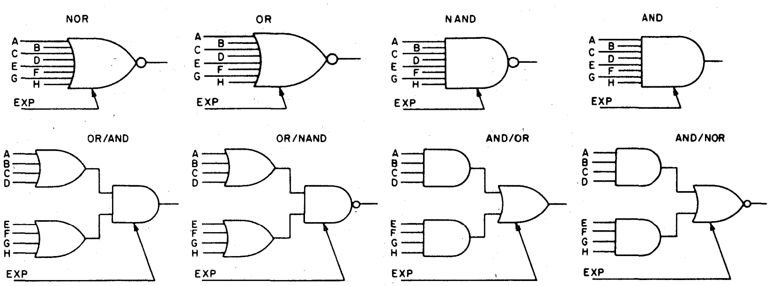


Fig. 1 – Basic logic configurations.

Applications:

- **Selection of up to 8 logic functions**
- **Digital control of logic**
- **General-purpose gating logic**
  - **Decoding**
  - **Encoding**

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,H Packages Min.	LIMITS D,F,H Packages Max.	LIMITS E Package Min.	LIMITS E Package Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V

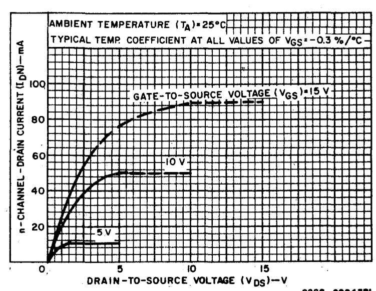


Fig. 2– Typical output n-channel drain characteristics.

CD4048A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	1	0.005	1	60	10	0.01	10	140	μA
	–	–	10	2	0.01	2	120	20	0.02	20	280	
	–	–	15	25	0.5	25	1000	250	2.5	250	2500	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) I_DN Min.	0.4	–	4.5	2	3.2	1.6	1.1	1.9	3.2	1.6	1.3	mA
	0.5	–	10	5.6	9	4.5	3.1	5.4	9	4.5	3.7	
p-channel (Source), I_DP Min.	4.6	–	5	−2	−3.2	−1.6	−1.1	−1.9	−3.2	−1.6	−1.3	
	9.5	–	10	−5.6	−9	−4.5	−3.1	−3.8	−9	−3.15	−2.6	
Input Leakage Current, I_{IL}, I_{IH}	Any Input											
	–	–	15	± 10^{-5} Typ., ± 1 Max.								μA
3-State Output Leakage Current I_{OL}, I_{OH}	Forced (Output Disabled)											μA
	–	–	15	±10^{-4} Typ., ±2 Max.								

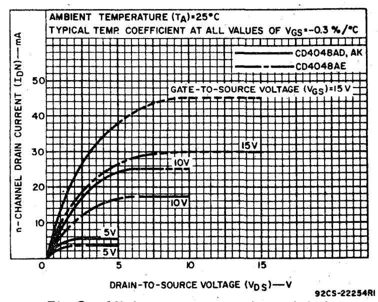


Fig. 3— Minimum output n-channel drain characteristics

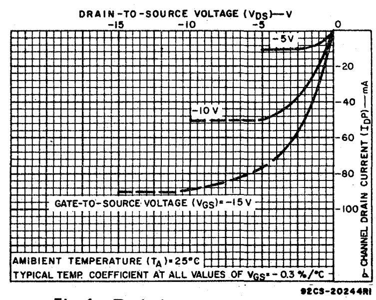


Fig. 4— Typical output p-channel drain characteristics.

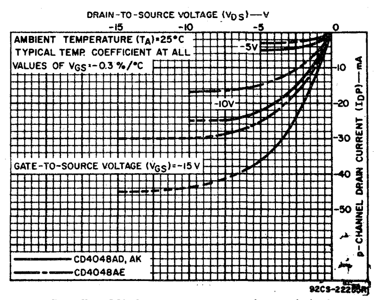


Fig. 5— Minimum output p-channel drain characteristics.

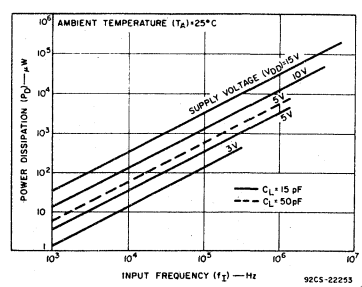


Fig. 6— Typical power dissipation as a function of input frequency.

DYNAMIC ELECTRICAL CHARACTERISTCS at T_A = 25°C and C_L = 15 pF and 50 pF,
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS				UNITS
			D,F,H Packages		E Package		
		V_{DD} (Volts)	TYP.	MAX.*	TYP.	MAX.*	
C_L = 15 pF							
Propagation Delay Time t_{PHL}		5	750	1300	750	1600	ns
		10	225	400	225	500	
Transition Time: High-to-Low Level t_{THL}		5	90	140	90	170	ns
		10	30	50	30	65	
Low-to-High Level t_{TLH}		5	130	250	130	300	ns
		10	40	60	40	75	
Input Capacitance C_I	Any Input		5	–	5	–	pF
C_L = 50 pF							
Propagation Delay Time t_{PLH}, t_{PHL}		5	775	1350	775	1650	ns
		10	240	430	240	530	
Transition Time: High-to-Low Level t_{THL}		5	105	170	105	200	ns
		10	40	70	40	85	
Low-to-High Level t_{TLH}		5	145	280	145	330	ns
		10	50	80	50	95	
Input Capacitance C_I	Any Input		5	–	5	–	pF

* Max. Limits represent worst-case limits for worst-case modes of operation shown in Figs. 15, 16, and 17.

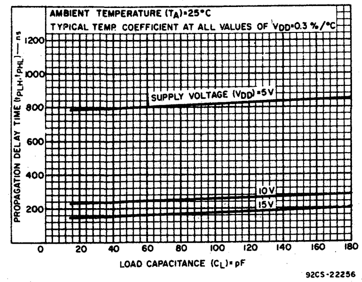


Fig. 7– Typical propagation delay time as a function of load capacitance.

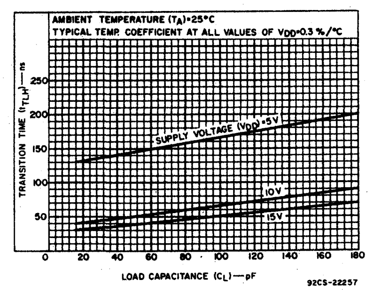


Fig. 8– Typical low-to-high level transition time as a function of load capacitance.

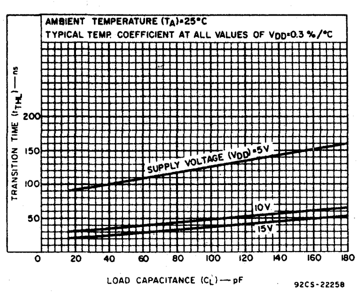


Fig. 9– Typical high-to-low level transition time as a function of load capacitance.

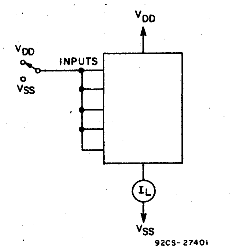


Fig. 10– Quiescent-device-current test circuit.

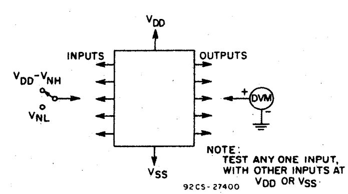


Fig. 11– Noise-immunity test circuit.

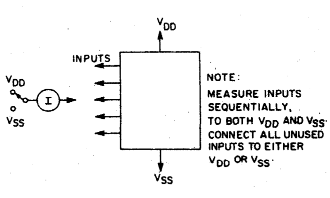


Fig. 12– Input-leakage-current test circuit.

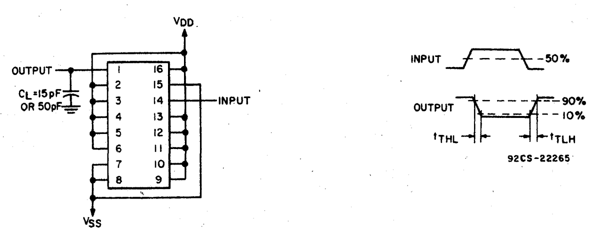


Fig. 13– t_{THL}, t_{TLH} – AND/NOR.

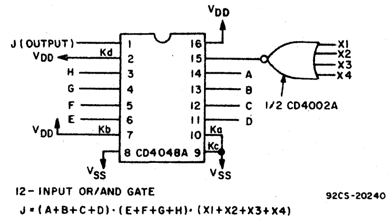
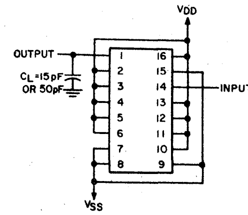


Fig. 14(a) · 12-input OR/AND gate.



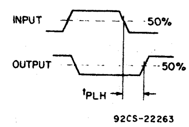


Fig. 15– t_{PLH} – NAND.

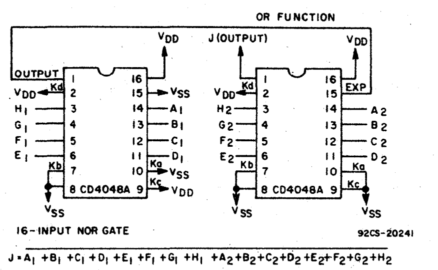
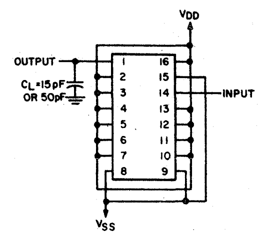


Fig. 14(b) 16-input NOR gate.
Applications of Expand Input



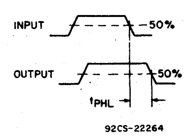
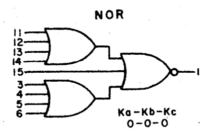


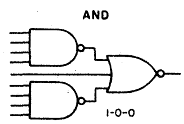
Fig. 16– t_{PHL} – AND.

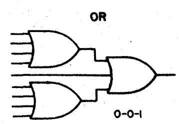
IMPLEMENTATION OF EXPAND INPUT FOR 9 OR MORE INPUTS

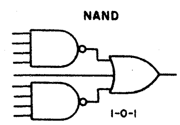
OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	$J=\overline{(A+B+C+D+E+F+G+H)+(EXP)}$
OR	OR	$J=(A+B+C+D+E+F+G+H)+(EXP)$
AND	NAND	$J=(ABCDEFGH)\cdot(\overline{EXP})$
NAND	NAND	$J=\overline{(ABCDEFGH)\cdot(\overline{EXP})}$
OR/AND	NOR	$J=(A+B+C+D)\cdot(E+F+G+H)\cdot(\overline{EXP})$
OR/NAND	NOR	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)\cdot(\overline{EXP})}$
AND/NOR	AND	$J=\overline{(ABCD)+(EFGH)+(EXP)}$
AND/OR	AND	$J=(ABCD)+(EFGH)+(EXP)$

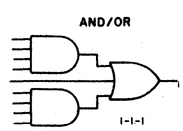
Note: (EXP) designates the EXPAND function (i.e., $X_1+X_2+\ldots X_N$).











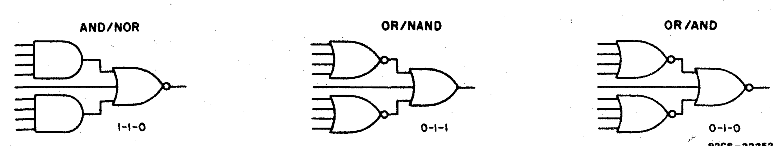
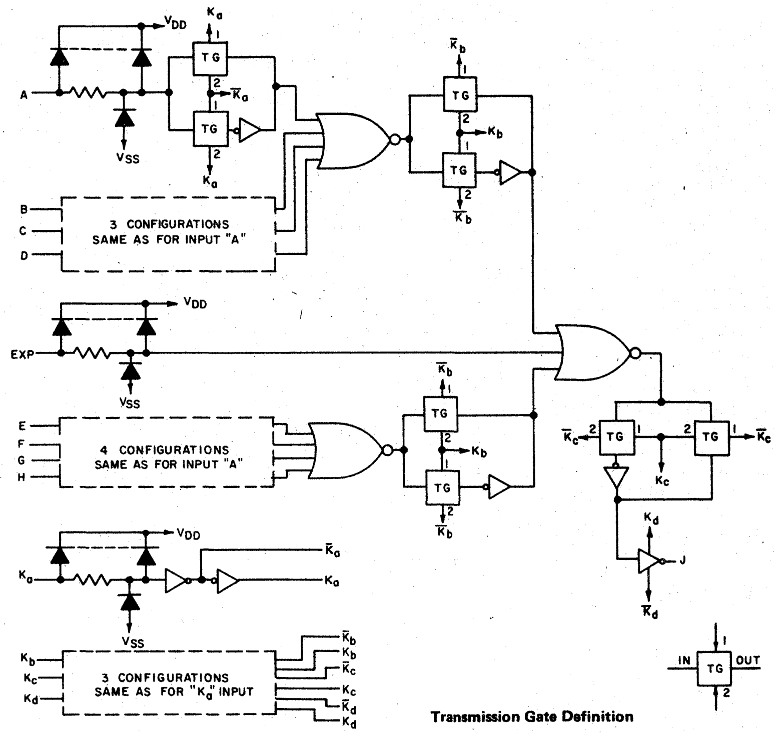


Fig. 14(c) · Actual-circuit logic configurations.

Fig. 14– Expansion logic and truth table.



Transmission Gate Definition

TG = Transmission Gate
Input to Output is:

a) A bidirectional low impedance when control input 1 is low and control 2 is high.
b) An open circuit when control input 1 is high and control input 2 is low.

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FUNCTION TRUTH TABLE

OUTPUT FUNCTION	BOOLEAN EXPRESSION	K_a	K_b	K_c	UNUSED INPUT*
NOR	$J=\overline{A+B+C+D+E+F+G+H}$	0	0	0	V_{SS}
OR	$J=A+B+C+D+E+F+G+H$	0	0	1	V_{SS}
OR/AND	$J=(A+B+C+D)\cdot(E+F+G+H)$	0	1	0	V_{SS}
OR/NAND	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)}$	0	1	1	V_{SS}
AND	$J=ABCDEFGH$	1	0	0	V_{DD}
NAND	$J=\overline{ABCDEFGH}$	1	0	1	V_{DD}
AND/NOR	$J=\overline{ABCD+EFGH}$	1	1	0	V_{DD}
AND/OR	$J=ABCD+EFGH$	1	1	1	V_{DD}
K_d=1 Normal Inverter Action					
K_d=0 High Impedance Output					

EXPAND Input=0 *See Figs. 1 and 7.

Fig. 17– Logic diagram and truth table.

CD4049A, CD4050A Types

COS/MOS Hex Buffer/Converters

CD4049A—Inverting Type
CD4050A—Non-Inverting Type

The CD4049A and CD4050A are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC}=5 V, $V_{OL} \geq 0.4$ V, and $I_DN \geq 3.2$ mA.)

The CD4049A and CD4050A are designated as replacements for CD4009A and CD4010A, respectively. Because the CD4049A and CD4050A require only one power supply, they are preferred over the CD4009A and CD4010A and should be used in place of the CD4009A and CD4010A in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049A and CD4050A are pin compatible with the CD4009A and CD4010A respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049A or CD4050A, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069 Hex Inverter is recommended.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **High sink current for driving 2 TTL loads**
- **High-to-low level logic conversion**
- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**

Applications:

- **COS/MOS to DTL/TTL hex converter**
- **COS/MOS current "sink" or "source" driver**
- **COS/MOS high-to-low logic-level converter**

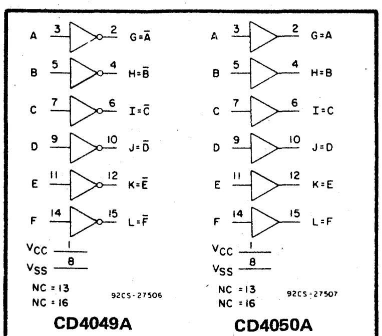


Fig.1 — Functional diagrams.

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (V_{CC}) (For T_A=Full Package-Temperature Range)	3	12	V
Input Voltage Range (V_I)	V_{CC}*	12	V

*The CD4049 and CD4050 have high-to-low-level voltage conversion capability but not low-to-high-level; therefore it is recommended that $V_I \geq V_{CC}$.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions V_O (V)	V_{IN} (V)	V_{CC} (V)	Limits at Indicated Temperatures (°C) D,F,H Packages −55	+25 Typ.	+25 Limit	+125	E Package −40	+25 Typ.	+25 Limit	+85	Units
Quiescent Device Current, I_L Max.	–	–	5	0.3	0.01	0.3	20	3	0.03	3	42	μA
	–	–	10	0.5	0.01	0.5	30	5	0.05	5	70	
	–	–	15	10	0.02	10	100	50	0.05	50	500	
Output Voltage: Low-Level, V_{OL}	–	0, 5	5	0 Typ.; 0.05 Max.								V
	–	0, 10	10	0 Typ.; 0.05 Max.								
High-Level, V_{OH}	–	0, 5	5	4.95 Min.; 5 Typ.								
	–	0, 10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL} CD4050A	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH} All Types	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Inputs Low, V_{NL} CD4049A	3.6	–	5	1 Min.; 1.5 Typ.								
	7.2	–	10	2 Min.; 3 Typ.								
Noise Margin: Inputs Low, V_{NML} Min. CD4050A	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH} Min. CD4050A	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	4.5	3.3	5.2	2.6	1.8	3.1	5.2	2.6	2.1	mA
	0.4	–	5	3.75	6	3	2.1	3.6	6	3	2.5	
	0.5	–	10	10	16	8	5.6	9.6	16	8	6.6	
P-Channel (Source), I_DP Min.	4.5	–	5	−0.62	−1	−0.5	−0.35	−0.6	−1	−0.5	−0.4	
	2.5	–	5	−1.85	−2.5	−1.25	−0.9	−1.5	−2.5	−1.25	−1	
	9.5	–	10	−1.85	−2.5	−1.25	−0.9	−1.5	−2.5	−1.25	−1	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{CC}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

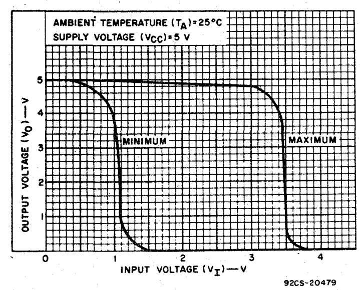


Fig. 2—Minimum and maximum voltage transfer characteristics for CD4049A.

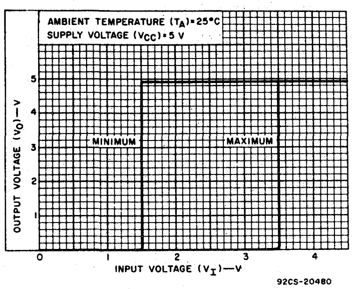


Fig. 3—Minimum and maximum voltage transfer characteristics for CD4050A.

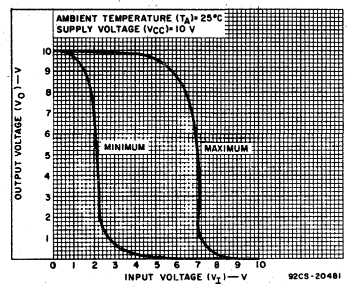


Fig. 4—Minimum and maximum voltage transfer characteristics for CD4049A.

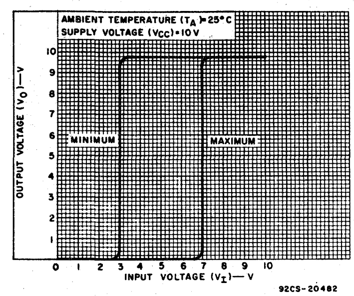


Fig. 5—Minimum and maximum voltage transfer characteristics for CD4050A.

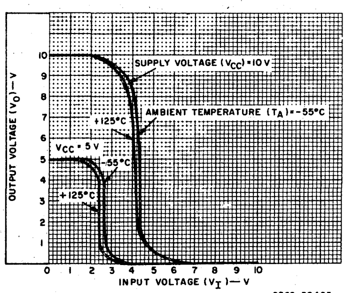


Fig. 6—Typical voltage transfer characteristics as a function of temperature for CD4049A.

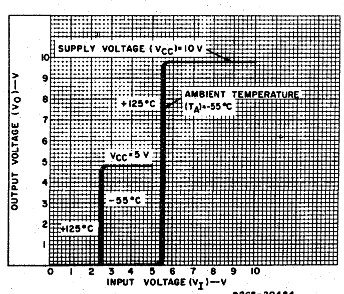


Fig. 7—Typical voltage transfer characteristics as a function of temperature for CD4050A.

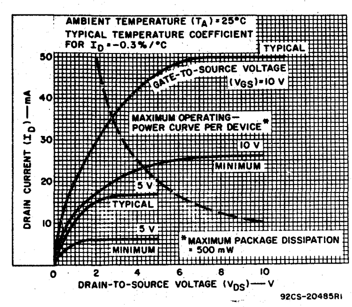


Fig. 8—Typical and minimum n-channel drain characteristics as a function of gate-to-source voltage (V_{GS}) for CD4049A, CD4050A.

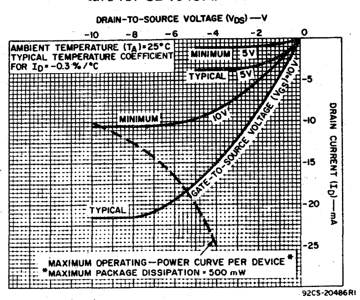


Fig. 9—Typical and minimum p-channel drain characteristics as a function of gate-to-source voltage (V_{GS}) for CD4049A, CD4050A.

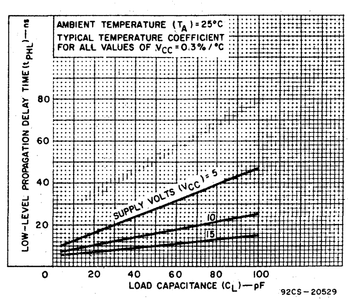


Fig. 10—Typical high-to-low level propagation delay time vs. C_L for CD4049A.

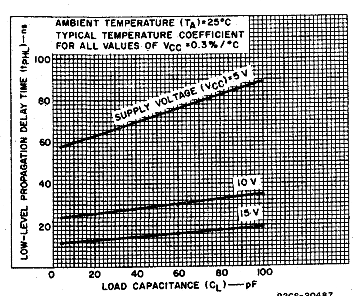


Fig. 11—Typical high-to-low level propagation delay time vs. C_L for CD4050A.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; Input t_r,t_f=20 ns, C_L=15 pF, R_L=200 kΩ

CHARACTERISTIC		CONDITIONS V_I	CONDITIONS V_{CC}	LIMITS ALL PKGS. Typ.	LIMITS ALL PKGS. Max.	UNITS
Propagation Delay Time: Low-to-High, t_{PLH}	CD4049A	5	5	50	80	ns
		10	10	25	55	
	CD4050A	5	5	75	140	
		10	10	35	85	
High-to-Low, t_{PHL}	CD4049A	5	5	15	55	ns
		10	10	10	30	
	CD4050A	5	5	55	110	
		10	10	25	55	
Transition Time: Low-to-High, t_{TLH}		5	5	50	100	ns
		10	10	30	60	
High-to-Low, t_{THL}		5	5	20	45	
		10	10	16	40	
Input Capacitance, C_I	CD4049A	–	–	15	–	pF
	CD4050A	–	–	5	–	

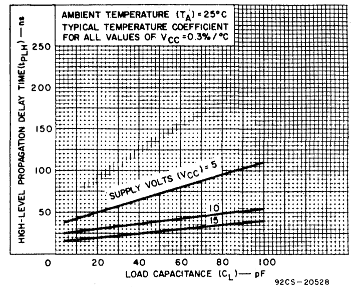


Fig. 12—Typical low-to-high level propagation delay time vs. C_L for CD4049A.

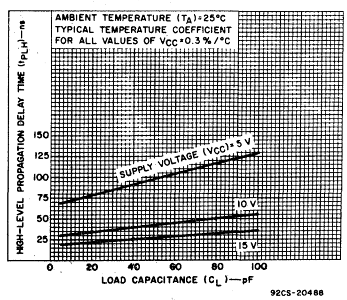


Fig. 13—Typical low-to-high level propagation delay time vs. C_L for CD4050A.

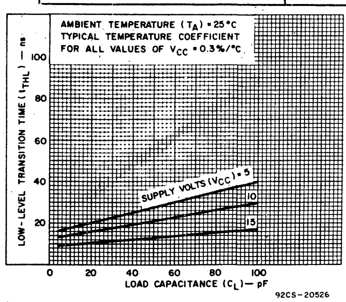


Fig. 14—Typical high-to-low level transition time vs. C_L for CD4049A, CD4050A.

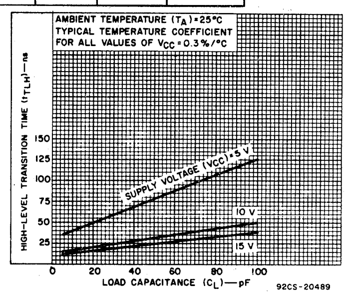


Fig. 15—Typical low-to-high level transition time vs. C_L for CD4049A, CD4050A.

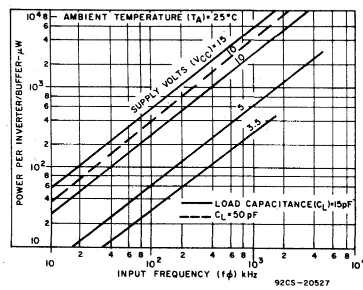


Fig. 16—Typical dissipation characteristics for CD4049A, CD4050A.

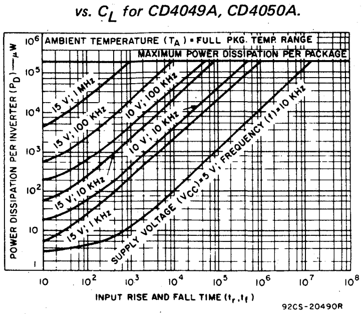


Fig. 17—Typical power dissipation vs. transition time per inverter CD4049A.

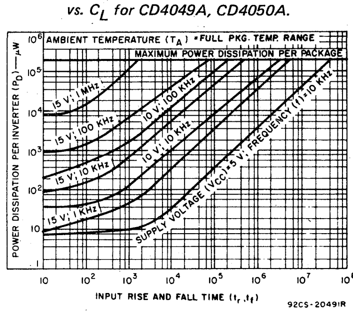


Fig. 18—Typical power dissipation vs. transition time per inverter CD4050A.

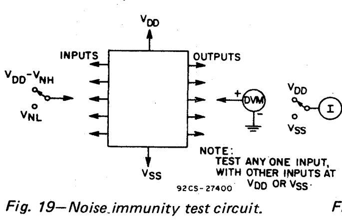


Fig. 19—Noise immunity test circuit.

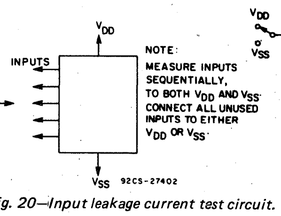


Fig. 20—Input leakage current test circuit.

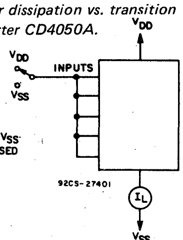


Fig. 21—Quiescent device current test circuit.

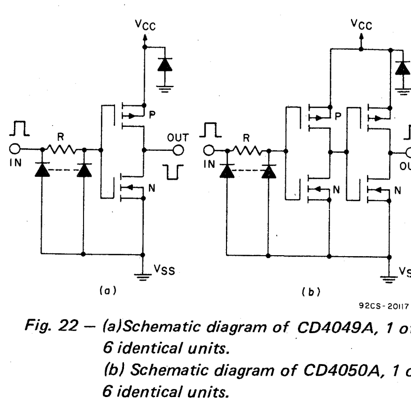


Fig. 22 — (a)Schematic diagram of CD4049A, 1 of 6 identical units. (b) Schematic diagram of CD4050A, 1 of 6 identical units.

COS/MOS LSI 4-Bit Arithmetic Logic Unit

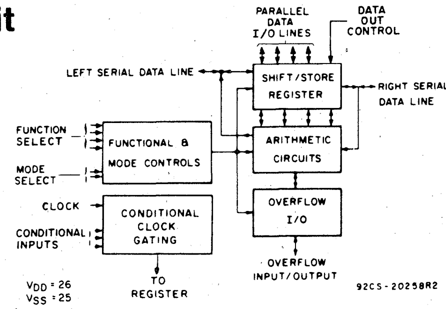


Fig. 1 – Block diagram – CD4057A.

The RCA-CD4057A is a low-power arithmetic logic unit (ALU) designed for use in LSI computers. An arithmetic system of virtually any size can be constructed by wiring together a number of CD4057A ALU's. The CD4057A provides 4-bit arithmetic operations, time sharing of data terminals, and full functional decoding for all control lines. The distributed control system of this device provides great flexibility in system designs by allowing hard-wired connection of N units in 4^N unique combinations. Four control lines provide 16 instructions which include Addition, Subtraction, Bidirectional and Cycle Shifts, Up-Down Counting, AND, OR, and Exclusive-OR logic operations.

Two mode control lines allow the CD4057A to function as any 4-bit section of a larger arithmetic unit by controlling the bidirectional serial transfer of data to adjacent arithmetic arrays. By means of three "Conditional Control" lines Overflow, All Zeros, and Negative State conditions may be detected and used to establish a conditional operation. Predetermined operation of the CD4057A on a conditional basis allows greater ALU flexibility. Although especially applicable as a parallel arithmetic unit, the CD4057A also finds use in virtually any application requiring one or more of its 16 basic instructions. The CD4057A is supplied in a hermetically sealed 28-lead dual-in-line ceramic package (CD4057AD), 28-lead ceramic flat package (CD4057AK), and in chip form (CD4057AH).

Applications:

- **Parallel Arithmetic Units**
- **Process Controllers**
- **Remote Data Sets**
- **Graphic Display Terminals**

Features:

- **LSI Complexity on a Single Chip**
- **16-Instruction Capability**
  - **-Add, Subtract, Count**
  - **-AND, OR, Exclusive-OR**
  - **-Right, Left, or Cyclic Shifts**
- **Bidirectional Data Busses**
- **Instruction Decoding on Chip**
- **Fully Static Operation**
- **Single-Phase Clocking**
- **Easily Expandable to 8, 12, 16,. . . . Bit Operation**
- **Low Quiescent Device Dissipation . . . . . . 10 μW (typ.)**
- **Conditional-Operation Controls on Chip**
- **Add Time (Data In-To Sum Out) =375 ns (typ) at 10V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, H . . . . −55 to +125°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = −55 to +100°C (PACKAGE TYPES D) . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D) . . . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	V
Setup Time, t_S DATA	5	40	–	ns
	10	20	–	ns
OP CODE	5	4590	–	ns
	10	1320	–	ns
Clock Pulse Width, t_W	5	1200	–	ns
	10	375	–	ns
Clock Input Frequency, f_{CL} Count Mode	5	0.13	–	MHz
	10	0.46	–	MHz
Shift Mode	5	0.33	–	MHz
	10	1.4	–	MHz
Clock Rise or Fall Time, t_rCL, t_fCL	5	–	15	μs
	10	–	15	μs

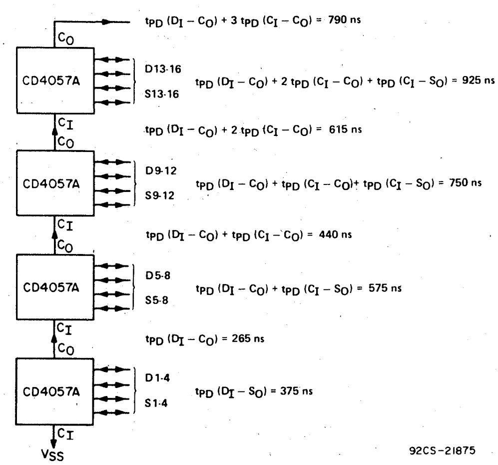


Fig. 2 – Typical speed characteristics of a 16-bit ALU at V_{DD} = 10 V.

CD4057A Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	Limits at Indicated Temperatures (°C) CD4057AD, CD4057AH −55°C Min.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNITS
Quiescent Device Current I_L	–	–	5	–	5	–	0.5	5	–	150	μA
	–	–	10	–	10	–	1	10	–	300	
	–	–	15	–	50	–	1	50	–	2000	
Output Voltage; Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.							V
	–	10	10	0 Typ.; 0.05 Max.							
High Level, V_{OH}	–	0	5	4.95 Min.; 5 Typ.							V
	–	0	10	9.95 Min.; 10 Typ.							
Noise Immunity (All Inputs) V_{NL}, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.							V
	1	–	10	3 Min.; 4.5 Typ.							
	4.2	–	5	1.5 Min.; 2.25 Typ.							
	9	–	10	3 Min.; 4.5 Typ.							
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.							V
	9	–	10	1 Min.							
Inputs High, V_{NMH}	0.5	–	5	1 Min.							
	1	–	10	1 Min.							
Output Drive Current: I_DN, I_DP Zero Indicator	0.5	–	5	0.11	–	0.09	0.16	–	0.06	–	mA
n-channel	0.5	–	10	0.12	–	0.10	0.16	–	0.07	–	
p-channel	3	–	5	0.04	–	0.03	0.06	–	0.02	–	
	7	–	10	0.08	–	0.07	0.13	–	0.05	–	
Negative Indicator	0.5	–	5	0.11	–	0.09	0.30	–	0.06	–	
n-channel	0.5	–	10	0.12	–	0.10	0.40	–	0.07	–	
p-channel	4.5	–	5	0.07	–	0.06	0.19	–	0.04	–	
	9.5	–	10	0.12	–	0.10	0.30	–	0.07	–	
Overflow Indicator	0.5	–	5	0.25	–	0.20	0.50	–	0.14	–	
n-channel	0.5	–	10	0.37	–	0.30	0.90	–	0.21	–	
p-channel	4.5	–	5	0.08	–	0.07	0.21	–	0.05	–	
	9.5	–	10	0.12	–	0.10	0.38	–	0.07	–	
All Other Outputs	0.5	–	5	0.11	–	0.09	0.10	–	0.06	–	
n-channel	0.5	–	10	0.06	–	0.05	0.12	–	0.03	–	
p-channel	4.5	–	5	0.02	–	0.02	0.05	–	0.01	–	
	9.5	–	10	0.06	–	0.05	0.08	–	0.03	–	
Input Leakage Current I_{IL}, I_{IH}	Any Input –	–	15	$\pm 10^{-5}$ Typ., ± 1 Max.							μA

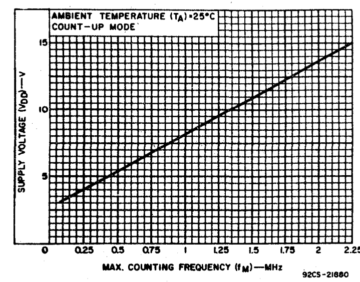


Fig. 3 — Maximum counting frequency vs. supply voltage for a typical CD4057A.

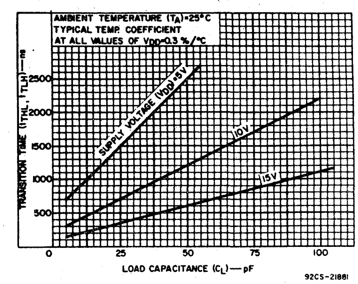


Fig. 4 — Transition time vs. load capacitance for data outputs (D1-D4).

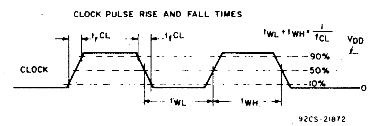


Fig. 5 — Clock pulse rise and fall times.

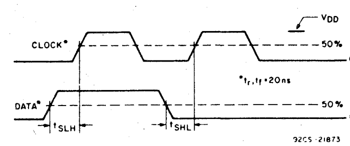


Fig. 6 — Data setup time.

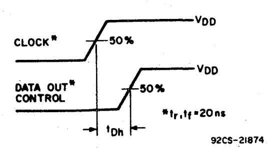


Fig. 7 — Data hold time.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$ and $C_L = 15$ pF, $R_L = 200$ kΩ, $t_r, t_f = 20$ ns

Typical Temperature Coefficient at all values of $V_{DD} = 0.3\%/°C$

CHARACTERISTICS	TEST CONDITIONS V_{DD}	LIMITS CD4057AD Min.	Typ.	Max.	UNITS
Propagation Delay Time: t_{PLH}, t_{PHL} DATA IN-to-SUM OUT	5	–	1430	3900	ns
	10	–	375	720	
CARRY IN-to-SUM OUT	5	–	915	2550	
	10	–	310	840	
DATA IN-to-CARRY OUT	5	–	950	2580	
	10	–	265	720	
CARRY IN-to-CARRY OUT	5	–	485	1320	
	10	–	175	480	
ZI Input -to- ZI Output	5	–	1980	5400	
	10	–	750	2040	
	5	–	265	720	
	10	–	110	300	
Transition Time: t_{TLH}, t_{THL} ZI Output	5	–	3700	10350	ns
	10	–	1650	4500	
	5	–	420	1140	
	10	–	220	600	
Negative Indicator and Overflow Indicator	5	–	300	825	
	10	–	165	450	
All Other Outputs	5	–	1000	2775	
	10	–	475	1275	
Minimum Clock Pulse Width, t_W	5	–	400	1200	ns
	10	–	125	375	
Clock Rise and Fall Time, t_rCL, t_fCL	5	–	–	15	µs
	10	–	–	15	
Minimum Set Up Time : t_{SLH}, t_{SHL} DATA	5	–	20	40	ns
	10	–	10	20	
OP CODE	5	–	1675	4590	ns
	10	–	485	1320	
Minimum Data Hold Time, t_{HLH}, t_{HHL}	5	–	20	40	ns
	10	–	10	20	
Maximum Clock Frequency: f_{CL} Count Mode	5	0.13	0.36	–	MHz
	10	0.46	1.35	–	
Shift Mode	5	0.33	0.90	–	
	10	1.4	3.8	–	
Input Capacitance, C_I	ANY INPUT	–	5	–	pF

LOGIC DESCRIPTION

OPERATIONAL MODES

The CD4057A arithmetic logic unit operates in one of four possible modes. These modes control the transfer of information, either serial data or arithmetic operation carries, to and from the serial-data lines. Fig. 8 shows the manner in which the four modes control the data on the serial-data lines.

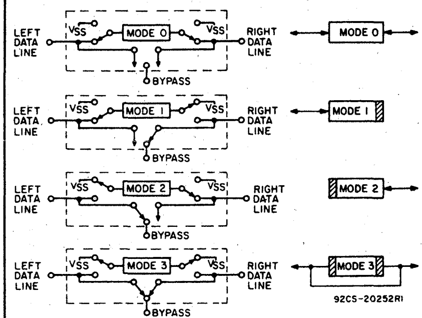


Fig. 8 – Schematic of "Mode" concept.

In MODE 0, data can enter or leave from either the left or the right serial-data line.

In MODE 1, data can enter or leave only on the left serial-data line.

In MODE 2, data can enter or leave only on the right serial-data line.

In MODE 3, serial data can neither enter nor leave the register, regardless of the nature of the operation. Furthermore, the register is by-passed electrically, i.e., there is an electrical bidirectional path between the right and left serial data terminals.

The two input lines labeled C1 and C2 in the terminal assignment diagram define one of four possible modes shown in Table I. Through the use of mode control, individual arithmetic arrays can be cascaded to form one large processor or many processors of various lengths.

TABLE I – MODE DEFINITION

C2	C1	MODE
0	0	0
0	1	1
1	0	2
1	1	3

Examples of how one " hard-wired " combination of three ALU's can form (a) a 12-bit parallel processor, (b) one 8-bit and one 4-bit parallel processor, or (c) three 4-bit parallel processors, merely by changes in the modes of each ALU are shown in Fig. 10.

CD4057A Types

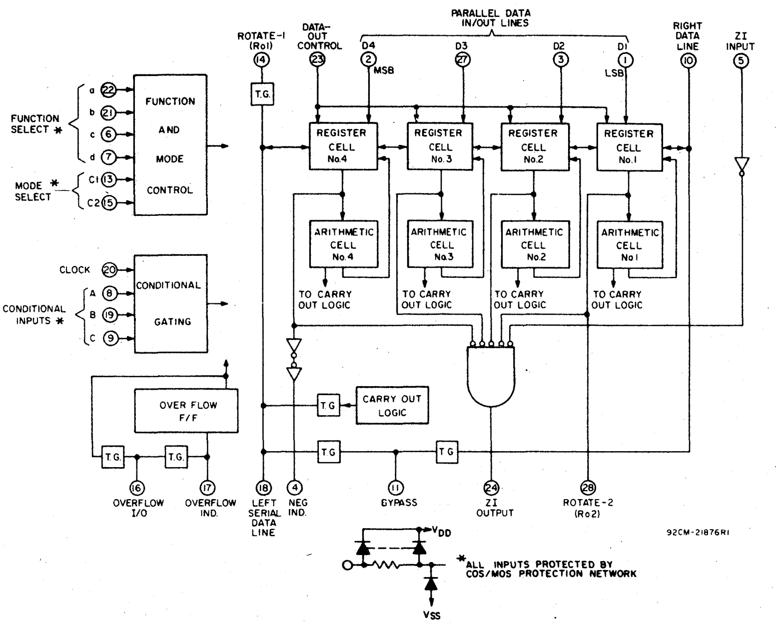


Fig. 9 – Simplified logic diagram.

Data-flow interruptions are shown by shaded areas. With these three ALU's and the four available modes, 61 more system combinations can be formed. If 4 ALU's are used, 4^4 combinations (256) are possible. *Fig.11* shows a diagram of 4 CD4057A's interconnected to form a 16-bit parallel processor.

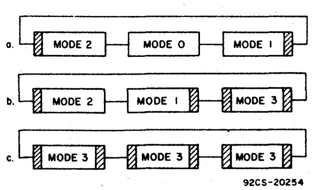


Fig. 10 – "Mode" connections for parallel processor:
(a) 12-bit unit,
(b) one 8-bit and one 4-bit unit
(c) three 4-bit units.

NOTE: The BYPASS terminal of the "most significant" CD4057A is connected to the bypass terminal of the "least significant" CD4057A. The bypass terminals on all other CD4057A's are left floating. This interconnection is performed whenever more than one CD4057A are used to form a processor.

INSTRUCTION REPERTOIRE

Four encoded lines are used to represent 16 instructions. Encoded instructions are as follows:

a	b	c	d	
0	0	0	0	NO-OP (Operational Inhibit)
0	0	0	1	AND
0	0	1	0	Count down
0	0	1	1	Count up
0	1	0	0	Subtract Stored number from zero (SMZ)
0	1	0	1	Subtract from parallel data lines (SM) (stored number from parallel data lines)
0	1	1	0	Add (AD)
0	1	1	1	Subtract (SUB) (Parallel data lines from stored number)
1	0	0	0	Set to all ones (SET)
1	0	0	1	Clear to all zeroes (CLEAR)
1	0	1	0	Exclusive-OR
1	0	1	1	OR
1	1	0	0	Input Data (From parallel data lines)
1	1	0	1	Left shift
1	1	1	0	Right shift
1	1	1	1	Rotate (cycle) right

All instructions are executed on the positive edge of the clock.

PARALLEL COMMANDS

a. **CLEAR** – sets register to zero.
b. **SET** –sets register to all ones.
c. **OR** –processes contents of register with value on parallel-data lines in a logical OR function.
d. **AND** –processes contents of register with value on parallel-data lines in a logical AND function.
e. **Exclusive-OR** – processes contents of register with data on parallel-data lines in a logical Exclusive-OR function.
f. **IN** –loads data on parallel-data lines into register.
g. **DATA OUT CONTROL** – unloads contents of register and overflow flip-flop onto parallel data lines and overflow I/O independent of all other controls.
h. **SUB:**

In Mode 0, adds to the contents of the register the one's complement of the data on the parallel-data lines. Carries can enter on the right serial data line and can leave on the left serial data line. The overflow indicator does not change state.

In Mode 1, adds to the contents of the register the two's complement of the data on the parallel-data lines. Generated carries can leave on the left serial line. The CARRY IN is set to zero. The overflow indicator does not change state.

In Mode 2, same as Mode 0, except carries cannot leave on the right serial-data line.The absence or presence of an overflow is registered.

In Mode 3, same as Mode 1, except carries cannot leave on the left serial-date line. The absence or presence of an overflow is registered.

i. **COUNT UP:**

In Mode 0, adds to the contents of the register the data on the right serial-data line and permits any resulting carry to leave on the left serial-data line. No data enters the parallel-data lines.

In Mode 1, internally adds a one to the contents of the register and permits any resulting carry to leave on the left serial-data line. No data enters or leaves the right serial-data line.

In Mode 2, adds to the contents of the register the data on the right serial-data line. No data enters or leaves the left serial-data line.

In Mode 3, internally adds a one to the contents of the register No data enters or leaves the register on any serial-data or parallel-data line.

In all modes, with the DATA OUT control high

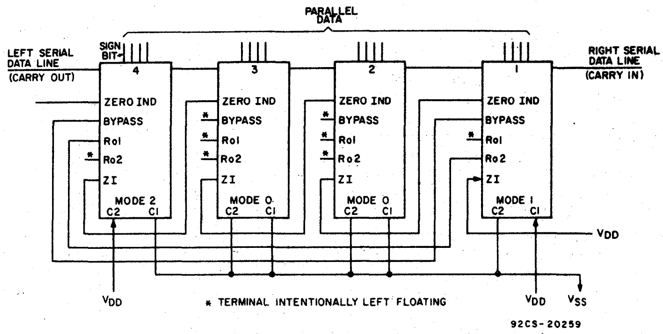


Fig. 11 — Connection for 16-bit arithmetic logic unit.

the count is presented on the parallel data lines (D1-D4).

j. COUNT DOWN:

In Mode 0, subtracts a one (2's complement form) from the contents of the register and adds to this result the data on the right serial-data line and permits any resulting carry to leave on the left serial-data line. No data enters on the parallel-data lines.

In Mode 1, internally subtracts a one from the contents of the register and permits any resulting carry to leave on the left serial-data line. No data enters or leaves the right serial-data line.

In Mode 2, subtracts a one from the contents of the register and adds to this result the data on the right serial-data line. No data enters or leaves on the left serial-data line.

In Mode 3, internally subtracts a one from the contents of the register. No data enters or leaves on the serial-data lines.

In all modes, with the DATA OUT control high the count is presented on the parallel data lines (D1-D4).

k. ADD(AD):

In Mode 0, adds the contents of the register to the data on the parallel-data lines and the right serial-data line. Any resulting carry can leave on the left serial-data line. The overflow indicator does not change state.

In Mode 1, adds the contents of the register to the data on the parallel-data lines and allows any resulting carry to leave on the left serial-data line. The right serial-data line is open-circuited. The overflow indicator does not change state. The CARRY-IN is set to zero.

In Mode 2, adds the contents of the register to the data on the parallel data lines and the right serial-data line. Any overflow sets the overflow indicator. The left serial-data line is open-circuited. The absence or presence of an overflow is registered.

In Mode 3, adds contents of the register to the data on the parallel-data lines. Any resulting carry sets the overflow indicator. The two serial-data lines are open circuited. The absence or presence of an overflow is registered. The CARRY-IN is set to zero.

l. SM — same operation as AD except the contents of the register are two's complemented during addition in Mode 1 and Mode 3. In Mode 0 or Mode 2, the contents of the register are one's complemented and added to the data on the right serial-data line and the parallel-data lines. Overflows occurring in Mode 1 or Mode 0 do not alter the overflow indicator. The presence or absence of overflows is registered on the overflow indicator in Mode 2 or Mode 3.

m. SMZ:

In Mode 0, one's complements the contents of the register and adds the data on the right serial-data line to the contents of the register. Any resulting carry can leave on the left serial-data line. The overflow indicator does not change state.

In Mode 1, two's complements the contents of the register and permits any carry to leave on the left serial-data line. No data can enter the right serial-data line. The overflow indicator does not change state. The CARRY-IN is set to zero.

In Mode 2, one's complements the contents of the register and adds the data on the right serial-data line to the contents of the register. Carries cannot leave the left serial data line. The absence or presence of an overflow alters the overflow indicator.

In Mode 3, two's complements the contents of the register. Serial data can neither enter the right serial-data line nor leave the left serial-data line. The overflow indicator is at zero. The CARRY-IN is set to zero.

n. NO-OP — no operation takes place, The clock input is inhibited and the state of all registers and indicators remains unchanged.

SERIAL-SHIFT OPERATIONS

a. ROTATE (cycle) RIGHT — This operation is internal. The contents of the register shift to the right, cyclic fashion with the leftmost stage accepting data from the rightmost stage regardless of the mode. Data can leave the register serially on the right data line only while the register is in Mode 1 or Mode 0. Data can enter the left data line serially while the register is in Mode 1 or Mode 0. The Ro1 terminal of the "Most Significant" CD4057A must be connected to the Ro2 terminal of the "Least Significant" CD4057A. All other Ro1 and Ro2 terminals must be left floating. When only one CD4057A is used, Ro1 must be connected to Ro2.

b. RIGHT SHIFT — The contents of the register shift to the right and serial operations are as follows:

In Mode 0, data can enter serially on the left data line, shift through the register, and leave on the right data line.

In Mode 1, data can enter serially on the left data line. The right data line effectively is open - circuited.

In Mode 2, data can leave serially on the right data line. The left data line effectively is open-circuited. Vacant spaces are filled with zeros.

In Mode 3, serial data can neither enter nor leave the register; however,the contents shift to the right and vacated places are filled with zeros.

In all modes, with the DATA OUT control high the data is presented on the parallel data lines (D1-D4).

c. **LEFT SHIFT** – The contents of the register shift to the left and serial operations are as follows;

In Mode 0, data can enter the right data line, shift through the register, and leave on the left data line.

In Mode 1, data can leave serially on the left data line. The right data line effectively is open-circuited. All vacant positions are filled with zeros.

In Mode 2, data can enter serially on the right data line. The left data line effectively is open-circuited.

In Mode 3, data can neither enter nor leave the register; however, the contents shift to the left, and vacated places are filled with zeros.

In all modes, with the DATA OUT control high the data is presented on the parallel data lines (D1-D4).

Because the "DATA OUT" control instruction is independent of the other 16 instructions, care must be taken not to activate this control when data are to be loaded into the processor. This instruction should only be activated when the processor is executing a NO-OP, any SHIFT, SMZ, COUNT UP or DOWN, CLEAR, or SET.

If a data line, serial or parallel, is used as an input and the logic state of that line is not defined (i.e., the line is an open circuit),then the result of any operation using that line is undefined.

OPERATIONAL SEQUENCE FOR ARITHMETIC ADD CYCLE

1. Apply IN Instruction and Word A on Parallel Data Lines (D1–D4).
2. Apply CLOCK to load Word A into the register.
3. Apply OP CODE Instruction and Word B on Data Lines.
4. Apply CLOCK to load resulting function of A and B into the register.
5. Apply "DATA OUT" control to present result to Parallel Data Lines.

NOTE: Transitions of Step 2 and Step 3 may occur almost simultaneously; i.e. separated by only one data-hold time.

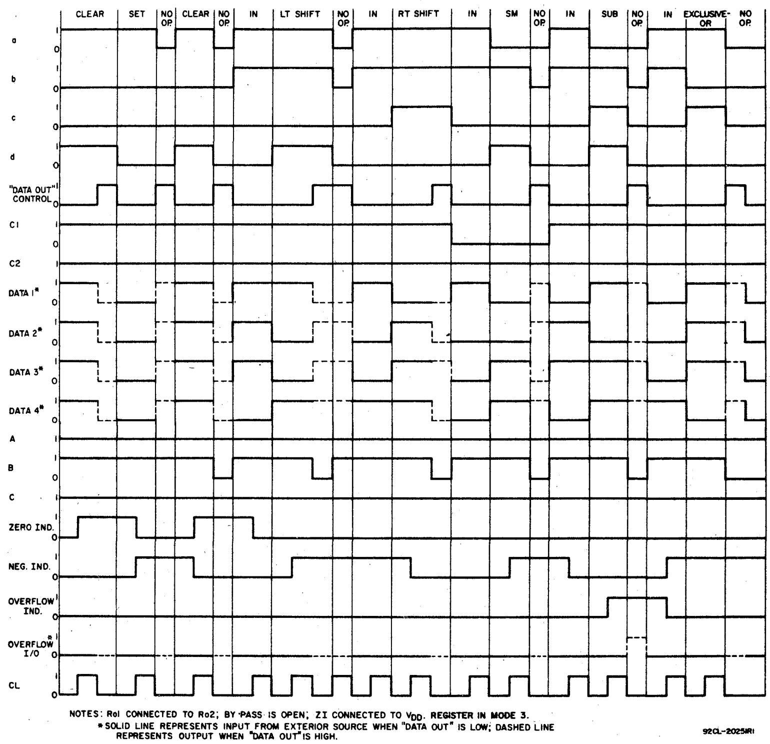


Fig. 12 – Timing diagram.

NEGATIVE-NUMBER DETECTION

The NEG IND terminal of the CD4057A is connected to the output of the flip-flop that is in the most significant bit position. A "1" on the NEG IND terminal indicates a negative number is in the register. This detection is also independent of modes.

ZERO DETECTION

The condition of "all zeros" is indicated by a "1" on the Zero Indicator terminal of the "Most Significant" CD4057A.
As shown in Fig. 11, terminal ZI of the CD4057A containing the least significant set of bits is connected to V_{DD}. Zero indication is independent of modes.

COMPLEMENTING NUMBERS

1. One's complement of number in ALU register.
   a) ALU must be in MODE 0 or MODE 2.
   b) Zero on Rt. Data Line.
   c) Execute an SMZ instruction.

(Continued)

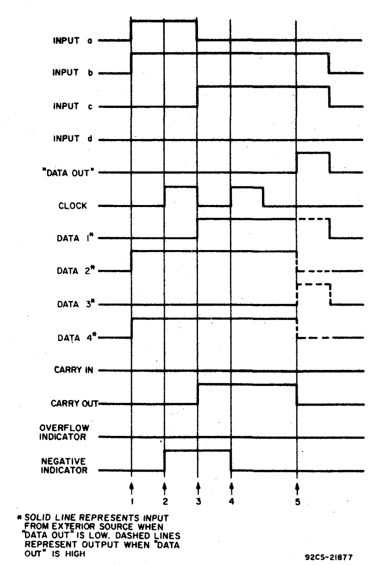
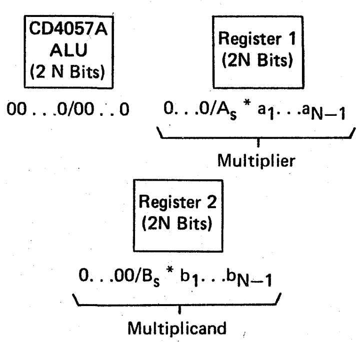


Fig. 13 – Add cycle waveforms.

2. One's complement of number to be loaded into ALU register.
   a) If zero indicator output is low, execute a CLEAR instruction, and make Rt. Data Line = 0.
   b) ALU must be in MODE 0 or MODE 2.
   c) Execute an SUB instruction.
3. Two's complement of number in ALU register.
   a) ALU must be in MODE 1 or MODE 3.
   b) Execute an SMZ instruction.
4. Two's complement of number to be loaded into ALU register.
   a) If zero indicator output is low, execute a CLEAR instruction, and make Rt. Data Line = 0.
   b) ALU must be in MODE 1 or MODE 3.
   c) Execute an SUB instruction.

The following algorithms are given as a general guideline to demonstrate some of the capabilities of the CD4057A.

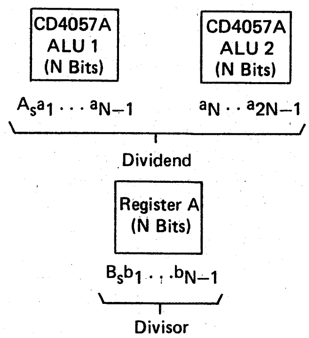
MULTIPLICATION OF TWO N-BIT NUMBERS



*A_s and B_s are sign bits

Multiplication Algorithm
1. Clear ALU to Zero
2. Store $A_s \oplus B_s$ in External Flip-Flop.
3. If $A_s = 1$, Complement Register 1.
4. If $B_s = 1$, Complement Register 2.
5. Load Register 2 into ALU.
6. Do shift Left on ALU N Times (N = number of bits).
7. Do N Times:
   (1)
   a) If MSB of ALU = 1 (Negative Indicator = High), Then shift ALU left 1 bit; add Register 1 to ALU.
   b) If MSB of ALU = 0 (Negative Indicator = Low) Then shift ALU left 1 bit.
8. If $A_s \oplus B_s = 1$, then Complement ALU.
9. Answer in ALU.

Division Algorithm



1. Store $A_s \oplus B_s$ in External Flip-Flop.
2. If $A_s = 1$, complement ALU 1 and ALU 2.
3. If $B_s = 1$, complement Register A.
4. Check for Divisor = 0
   a) If Divisor = 0; stop, indicates division by 0.
   b) If Divisor $\neq 0$; continue.
5. Apply SUB instruction to ALU 1 and the contents of Register A to ALU 1 data lines.
6. Put a zero on RT data line of ALU 2 and shift ALU 1 & ALU 2 left 1 bit.
7. Do "N" times.
   (1) Apply a sub instruction to ALU 1 and the contents of Register A to the ALU 1 data lines.
   a) If $C_O = 1$, then clock ALU 1, and put a 1 on right data line of ALU 2.
   b) If $C_O = 0$, then do not clock, and put a 0 on right data line of ALU 2.
   (2) Shift left 1 bit.
8. If sign Flip Flop = 1, complement ALU 2.
9. Answer in ALU 2.

CONDITIONAL OPERATION

Inhibition of the clock pulse can be accomplished with a programmed NO-OP instruction or through conditional input terminals A,B,and C. In a system of many CD4057A's, each CD4057A can be made to automatically control its own operation or the operation of any other CD4057A in the system in conjunction with the Overflow, Zero, or Negative (Number) indicators. Table II, the conditional inputs, truth table, defines the interactions among A,B, and C.

TABLE II – CONDITIONAL-INPUTS TRUTH TABLE

A	B	C	OPERATION PERMITTED
0	X	X	Yes
1	0	0	Yes
1	0	1	No
1	1	0	No
1	1	1	Yes

X = don't care

Two examples of how the conditional operation can be used are as follows:

1) For the Multiplication Algorithm
   A = 1, for step 7 (1)
   A = 0, for step 7 (2)
   B = 1
   C = negative Indicator
2) For the Division Algorithm
   A = 1, for step 7 (1)
   A = 0, for step 7 (2)
   B = 1
   C = C_O (left data line)

OVERFLOW DETECTION

The CD4057A is capable of detecting and indicating the presence or absence of an arithmetic two's-complement overflow. A two's-complement overflow is defined as having occurred if the signs of the two initial words are the same and the sign of the result is different while performing a carry-generating instruction.

$$\text{For example:}\quad \begin{array}{r} 0.011 \\ (+)\ \underline{0.110} \\ 1.001 \end{array}$$

Overflows can be detected and indicated only during operation in Mode 2 or Mode 3 and can occur for only four instructions (AD, SMZ, SM, and SUB). If an overflow is detected and stored in the overflow flip-flop, any one of the five instructions AD, SMZ, SM, SUB, or IN can change the overflow indicator.

When any of the three subtraction instructions is used, the sign bit of the data being subtracted is complemented and this value is used as one of the two initial signs to detect overflows. If an overflow has occurred, the final sign of the sum or difference is one's complemented and stored in the most-significant-bit position of the register.

The overflow flip-flop is updated at the same time the new result is stored in the CD4057A. Whenever data on the parallel-data lines are loaded into the CD4057A, whatever is on the Overflow I/O line is loaded into the overflow flip-flop. Also, whenever data are dumped on the parallel data lines from the CD4057A, the contents of the overflow flip-flop are dumped on the Overflow I/O line. Thus overflows may be stored elsewhere and then fed into the CD4057A at another time.

OPERATIONAL SEQUENCE AND WAVEFORMS FOR PROPAGATION-DELAY MEASUREMENTS

1. DATA-IN-to-CARRY OUT and DATA IN-to-SUM OUT
   A. Apply Word A and IN instruction
   B. Apply Clock to load word A into register
   C. Apply AD instruction
   D. Apply Word B (data in)
   E. Apply Clock to load result (sum out)
   F. Apply DATA OUT CONTROL to look at result

2. CARRY IN-to-CARRY OUT and CARRY IN-to-SUM OUT
   A. Apply Word A and IN instruction
   B. Apply Clock to load word A into register
   C. Apply AD instruction
   D. Apply Word B
   E. Apply CARRY IN (carry in)
   F. Apply Clock to load result (sum out)
   G. Apply DATA OUT CONTROL to look at result

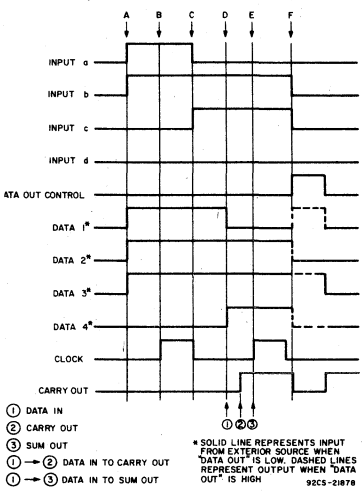


Fig. 14(a) — DATA IN-to-CARRY OUT and DATA IN-to-SUM OUT.

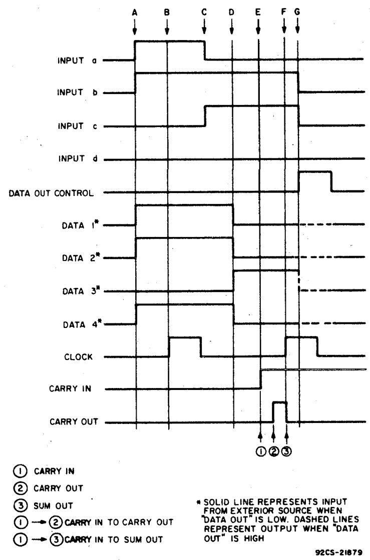


Fig. 14(b) — CARRY IN-to-CARRY OUT and CARRY IN-to-SUM OUT.

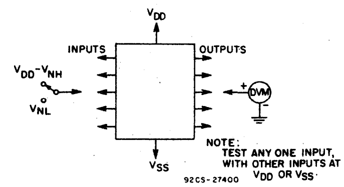


Fig. 15 — Noise-immunity test circuit.

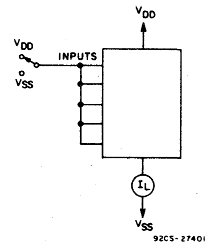


Fig. 16 — Quiescent-device-current test circuit

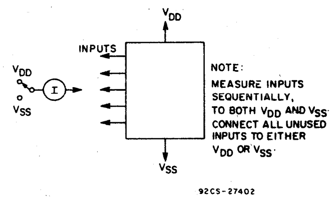


Fig. 17 — Input-leakage-current test circuit.

TYPICAL APPLICATION

The CD4057A has been designed for use as a parallel processor in flexible, programmable, easily expandable, special or general purpose computers, where minimization of external connections and data busing are primary design goals. The block diagram of Fig. 18 is an example of a computer that processes 8 bits in parallel.

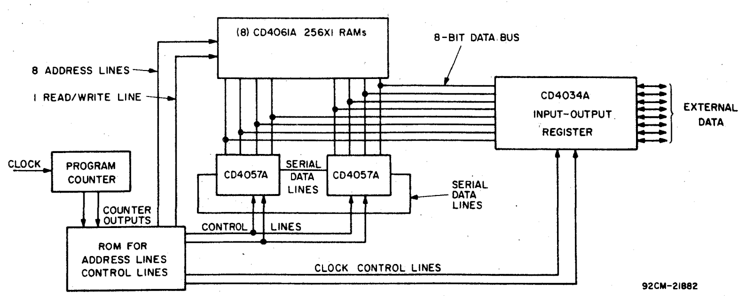
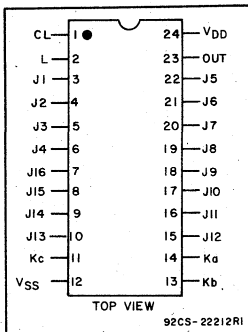


Fig. 18 — Example of computer organization using CD4057A.

COS/MOS Programmable Divide-by-"N" Counter

Standard "A"-Series Types (3-to-15-Volt Rating)



TERMINAL DIAGRAM

Operational and Performance Features:

- **Synchronous Programmable ÷ N Counter: N = 3 to 9999 or 15,999**
- **Presettable down-counter**
- **Fully static operation**
- **Mode-select control of initial decade counting function (÷ 10,8,5,4,2)**
- **T^2L drive capability**
- **Master preset initialization**
- **Latchable ÷ N output**
- **Quiescent current specified to 15 volts**
- **Max. input leakage current of 1 μA at 15 volts, full package-temperature range**
- **1 volt noise margin, full package-temperature range**
- **5-V and 10-V parametric ratings**

Applications

- **Communications digital frequency synthesizers: VHF, UHF, FM, AM, etc.**
- **Fixed or programmable frequency division**
- **"Time out" timer for consumer-application industrial controls**
- **Companion Application Note, ICAN-6374, "Application of the COS/MOS CD4059A Programmable Divide-by-N Counter in FM and Citizens Band Transceiver Digital Tuners"**

RCA-CD4059 standard "A"-Series types are divide-by-N down-counters that can be programmed to divide an input frequency by any number "N" from 3 to 15,999. The output signal is a pulse one clock-cycle wide occurring at a rate equal to the input frequency divided by N. This single output has TTL drive capability. The down-counter is preset by means of 16 jam inputs.

The three Mode-Select Inputs Ka, Kb, and Kc determine the modulus ("divide-by" number) of the first and last counting sections in accordance with the truth table shown in Table I. Every time the first (fastest) counting section goes through one cycle, it reduces by 1 the number that has been preset (jammed) into the three decades of the intermediate counting section and into the last counting section, which consists of flip-flops that are not needed for operating the first counting section. For example, in the ÷ 2 mode, only one flip-flop is needed in the first counting section. Therefore the last counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands. If ÷ 10 is desired for the first section, Ka is set to 1, Kb to 1, and Kc to 0. Jam Inputs J1, J2, J3, and J4 are used to preset the first counting section and there is no last counting section. The intermediate counting section consists of three cascaded BCD decade (÷ 10) counters presettable by means of Jam Inputs J5 through J16.

The Mode-Select Inputs permit frequency-synthesizer channel separations of 10, 12.5, 20, 25, or 50 parts. These inputs set the maximum value of N at 9999 (when the first counting section divides by 5 or 10) or 15,999 (when the first counting section divides by 8, 4, or 2).

The three decades of the intermediate counting section can be preset to a binary 15 instead of a binary 9, while their place values are still 1, 10, and 100, multiplied by the number of the ÷ N mode. For example, in the ÷ 8 mode, the number from which counting-down begins can be preset to:

3rd decade:	1500
2nd decade:	150
1st decade:	15
Last counting section	1000

The total of these numbers (2665) times 8 equals 21,320. The first counting section can be preset to 7. Therefore, 21,327 is the maximum possible count in the ÷ 8 mode.

The highest count of the various modes is shown in the column entitled Extended Counter Range of Table 1. Control inputs Kb and Kc can be used to initiate and lock the counter in the "master preset" state. In this condition the flip-flops in the counter are preset in accordance with the jam inputs and the counter remains in that state as long as Kb and Kc both remain low. The counter begins to count down from the preset state when a counting mode other than the master preset mode is selected.

The counter should always be put in the master preset mode before the ÷5 mode is selected.

Whenever the master preset mode is used, control signals Kb=0 and Kc=0 must be applied for at least 3 full clock pulses.

After the Master Preset Mode inputs have been changed to one of the ÷ modes, the next positive-going clock transition changes an internal flip-flop so that the countdown can begin at the second positive-going clock transition. Thus, after an MP (Master Preset) mode, there is always one extra count before the output goes high. Fig.1 illustrates a total count of 3 (÷ 8 mode). If the Master Preset mode is started two clock cycles or less before an output pulse, the output pulse will appear at the time due. If the Master Preset Mode is not used the counter jumps back to the "JAM" count when the output pulse appears.

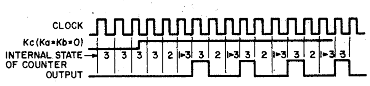


Fig.1 — Total count of 3.

A "1" on the Latch Enable input will cause the counter output to remain high once an output pulse occurs, and to remain in the high state until the latch input returns to "0". If the Latch Enable is "0", the output pulse will remain high for only 1 cycle of the clock-input signal.

As illustrated in the sample applications, this device is particularly advantageous in communication digital frequency synthesis (VHF, UHF, FM, AM, etc.) where programmable divide-by-"N" counters are an integral part of the synthesizer phase-locked-loop subsystem. The CD4059A can also be used to perform the synthesizer "Fixed Divide-by-R" counting function. It is also useful in general-purpose counters for instrumentation functions such as totalizers, production counters, and "time out" timers.

The CD4059A series types are available in a 24-lead ceramic dual-in-line package, 24-lead dual-in-line plastic package, 24-lead ceramic flat package, and in chip form.

CD4059A Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, V_{DD} (Voltages referenced to V_{SS} terminal) . . . . −0.5 to +15 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (Package Type E) . . . . 500 mW
For T_A = +60 to +85°C (Package Type E) . . . . Derate Linearly to 200 mW
For T_A = −55 to +100°C (Package Types D,H) . . . . 500 mW
For T_A = +100 to +125°C (Package Types D,H) . . . . . Derate Linearly to 100 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full package-temperature range (All package types) . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
Package Types D,H . . . . −55 to +125°C
Package Type E . . . . −40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{STG}) . . . . −65 to 150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . . . +265°C

OPERATING CONDITIONS AT T_A = 25°C
(Unless otherwise specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units
Supply Voltage Range (over full temp. range)	–	3	12	V
Clock Pulse Width	5	200	–	ns
	10	100	–	
Clock Input Frequency	5	–	1.5	MHz
	10	–	3	
Clock Input Rise and Fall Time	5	–	15	µs
	10	–	5	

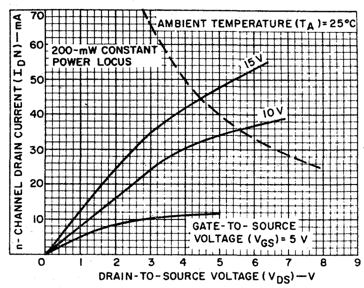


Fig.2 – Minimum output n-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions V_O (V)	V_{IN} (V)	V_{DD} (V)	Limits: *Values at −55°C,+25°C,+125°C Apply to D, H Packages; Values at −40°C,+25°C,+85°C Apply to E Packages* −55°	−40°	+85°	+125°	+25° Min.	Typ.	Max.	Units
Quiescent Device Current, I_L Max.			5	10	10	700	300	–	0.02	10	µA
			10	20	20	200	400	–	0.02	20	
			15	–	–	–	–	–	–	500	
Output Voltage: Low Level, V_{OL} Max.		0,5	5	0.05				–	0	0.05	V
		0,10	10	0.05				–	0	0.05	
High Level, V_{OH} Min.		0,5	5	4.95				4.95	5	–	
		0,10	10	9.95				9.95	10	–	
Noise Immunity: Inputs Low, V_{NL} Min.			5	1.5				1.5	2.25	–	V
			10	3				3	4.5	–	
Inputs High, V_{NH} Min.			5	1.5				1	2.25	–	
			10	3				3	4.5	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5		5	1							V
	9		10	1							
Inputs High, V_{NMH} Min.	0.5		5	1							
	1		10	1							
Output Drive Current: N-Channel (Sink) I_DN Min.	0.4		5	2.5	2.3	1.6	1.4	2	4	–	mA
	0.5		10	5	4.7	3.3	2.8	4	9	–	
P-Channel (Source) I_DP Min.	2.5		5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	4.6		5	−0.5	−0.45	−0.36	−0.3	−0.4	−0.8	–	
	9.5		10	−1.1	−1	−0.75	−0.65	−0.9	−1.8	–	
Input Leakage Current:* I_{IL}, I_{IH} Max.			15	±1					$\pm10^{-5}$	±1	µA

* Any Input

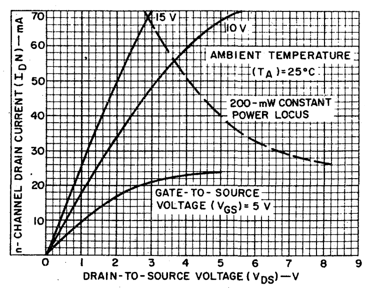


Fig.3 – Typical output n-channel drain characteristics.

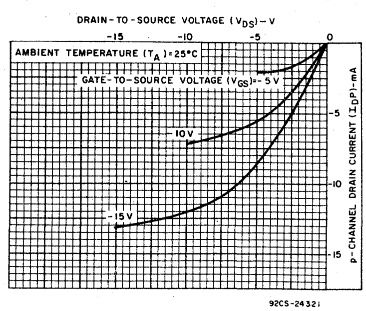
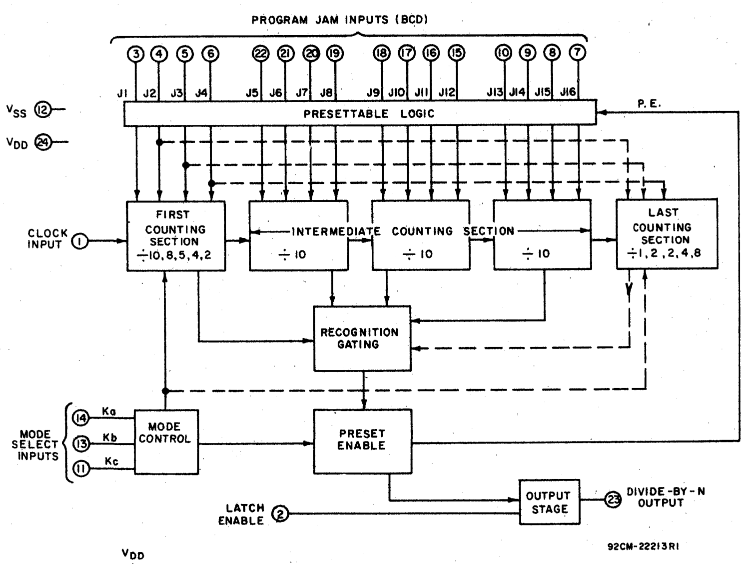
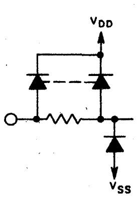


Fig.4 – Minimum output p-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS AT T_A = 25°C, C_L = 50 pF, Input t_r, t_f = 20 ns, R_L = 200 kΩ

CHARACTERISTIC		CONDITIONS V_{DD} (V)	LIMITS ALL PACKAGES Min.	Typ.	Max.	UNITS
Propagation Delay Time; t_{PHL}, t_{PLH}		5	–	180	360	ns
		10	–	90	180	
Transition Time:	t_{THL}	5	–	35	70	ns
		10	–	20	40	
	t_{TLH}	5	–	100	200	
		10	–	50	100	
Maximum Clock Input Frequency, f_{CL}		5	1.5	3	–	MHz
		10	3	6	–	
Average Input Capacitance, C_I (any input)		–	–	5	–	pF





ALL INPUTS (TERMS. 1-11, 13-22) PROTECTED BY COS/MOS PROTECTION NETWORK

Fig.5 – Functional block diagram.

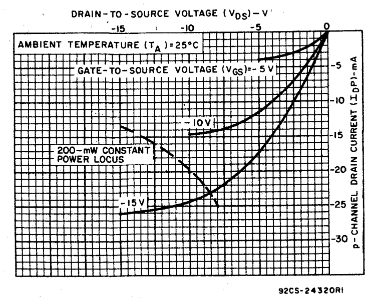


Fig.6 – Typical output p-channel drain characteristics.

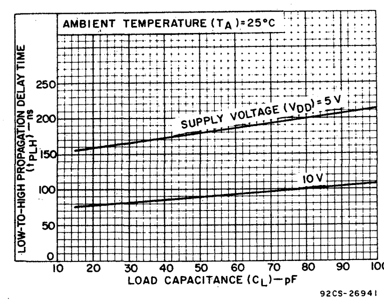


Fig.7 – Typical low-to-high propagation delay time vs. load capacitance.

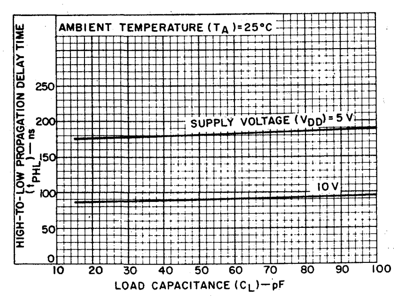


Fig.8 – Typical high-to-low propagation delay time vs. load capacitance.

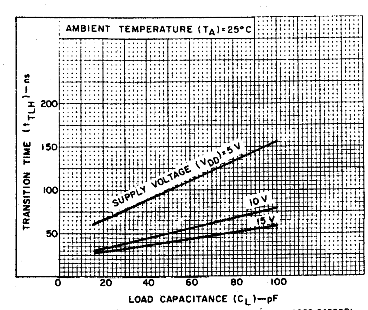


Fig.9 – Typical low-to-high transition time vs. load capacitance.

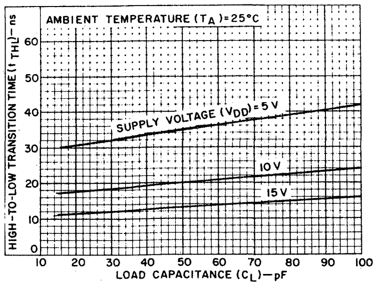


Fig.10 – Typical high-to-low transition time vs. load capacitance.

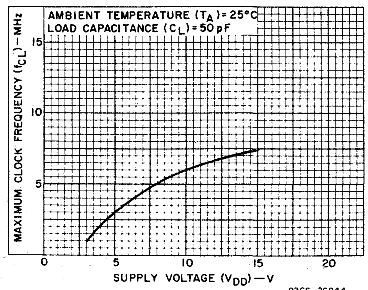


Fig.11 – Typical max. clock frequency vs. supply voltage.

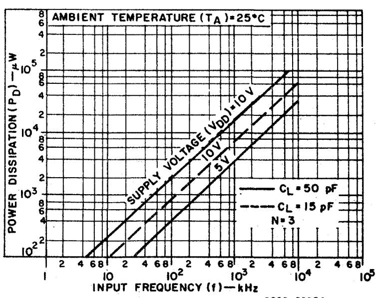


Fig.12 – Typical power dissipation vs. input frequency.

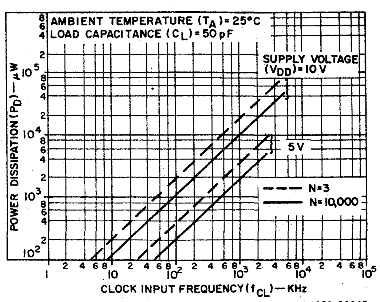


Fig.13 – Typical power dissipation vs. clock input frequency.

TABLE I

MODE SELECT INPUT			FIRST COUNTING SECTION			LAST COUNTING SECTION			COUNTER RANGE DESIGN	COUNTER RANGE EXTENDED
Ka	Kb	Kc	MODE Di-vides by:	Can be preset to a max of:	Jam▲ inputs used:	MODE Di-vides by:	Can be preset to a max of:	Jam▲ inputs used:	Max.	Max.
1	1	1	2	1	J1	8	7	J2,J3,J4	15,999	17,331
0	1	1	4	3	J1,J2	4	3	J3,J4	15,999	18,663
1	0	1	5#	4	J1,J2,J3	2	1	J4	9,999	13,329
0	0	1	8	7	J1,J2,J3	2	1	J4	15,999	21,327
1	1	0	10	9	J1,J2,J3,J4	1	0	–	9,999	16,659
X	0	0	MASTER PRESET			MASTER PRESET			–	–

X = Don't Care

▲ J1 = Least significant bit.
J4 = Most significant bit.

#Operation in the ÷5 mode (1st counting section) requires going through the Master Preset mode prior to going into the ÷5 mode. At power turn-on, kc must be a logic "0" for a period of 3 input clock pulses after V_{DD} reaches a minimum of 3 volts. See Fig. 21 for a suggested external preset circuit.

HOW TO PRESET THE CD4059A TO DESIRED ÷ N

The value N is determined as follows:

N = [MODE*] [1000 x Decade 5 Preset + 100X Decade 4 Preset + 10X Decade 3 Preset + 1X Decade 2 Preset] + Decade 1 Preset (1)

* MODE= First counting section divider (10, 8, 5, 4 or 2)

To calculate preset values for any N count, divide the N count by the Mode.

The resultant is the corresponding preset values of the 5th through 2nd decade with the remainder being equal to the 1st decade value.

$$\text{Preset Value} = \frac{N}{\text{Mode}} \quad (2)$$

Examples:

A) N = 8479, Mode = 5

1695 + 4 ← Preset Values

5 | 8479

Mode N

MODE SELECT = 5

Ka	Kb	Kc
1	0	1

PROGRAM JAM INPUTS (BCD)

4			1	5				9				6			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
0	0	1	1	1	0	1	0	1	0	0	1	0	1	1	0

To verify the results use equation 1 :

N = 5 (1000X 1 + 100 X 6 + 10 X 9 + 1 X 5) + 4

N = 8479

MODE SELECT = 8

B) N = 12382, Mode = 8

1547 + 6

8 | 12382

Ka	Kb	Kc
0	0	1

PROGRAM JAM INPUTS

6		1		7				4				5			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
0	1	1	1	1	1	1	0	0	0	1	0	1	0	1	0

To verify:

$N = 8\,(1000 \times 1 + 100 \times 5 + 10 \times 4 + 1 \times 7) + 6$

$N = 12382$

MODE SELECT = 10

C) N = 8479, Mode = 10

$$10 \overline{)8479} \quad 0847 + 9$$

Ka	Kb	Kc
1	1	0

PROGRAM JAM INPUTS

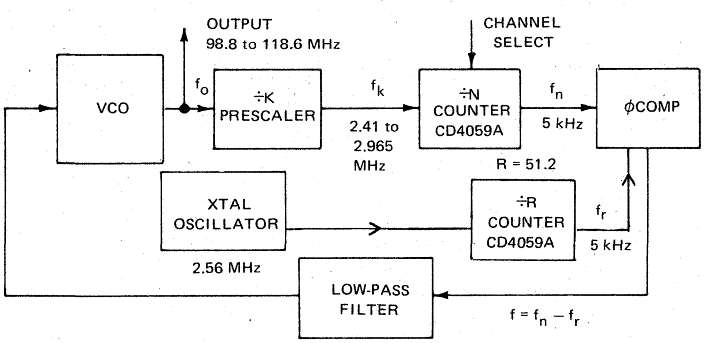
9				7				4				8			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
1	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1

To Verify:

$N = 10\,(1000 \times 0 + 100 \times 8 + 10 \times 4 + 1 \times 7) + 9$

$N = 8479$

DIGITAL PHASE-LOCKED LOOP (PLL) FOR FM BAND SYNTHESIZER



1) Calculating Min & Max "N" Values :

Output Freq. Range (f_o) = 98.8 to 118.6 MHz

Channel Spacing Freq. (f_c) = 200 kHz

Division Factor (k) = 40

$$\text{Reference Freq. } (fr) = \frac{f_c}{k} = \frac{200}{40}\ \text{kHz} = 5\ \text{kHz}$$

$$f_k = \frac{f_o}{40} \; : \; f_k\text{Max.} = \frac{118.6\ \text{MHz}}{40} = 2.965\ \text{MHz};\ f_k\text{Min} = \frac{98.8\ \text{MHz}}{40} = 2.47\ \text{MHz}$$

$$\therefore\ N = \frac{f_o}{f_c}$$

$$N_{Max} = \frac{118.6\ \text{MHz}}{200\ \text{kHz}} = 593 \qquad N_{Min} = \frac{98.8\ \text{MHz}}{200\ \text{kHz}} = 494 \qquad R = \frac{2.56\ \text{MHz}}{5\ \text{kHz}} = 512$$

"CASCADING" VIA OTHER COUNTERS

Fig. 14 shows a BCD-switch compatible arrangement suitable for ÷ 8 and ÷ 5 modes, which can be adapted, with slight changes, to the other divide-by-modes. In order to be able to preset to any number from three to about 256,000, while preserving the BCD-switch compatible character of the jam inputs, a rather complex cascading scheme is required. Such a cascading scheme is necessary because the CD4059A can never be preset to a count less than 3 and logic is needed to detect the condition that one of the numbers to be preset in the CD4059A is rather small. In order to simplify the detection logic, only that condition is detected where the jam inputs to terminals 6, 7, and 9 would be low during one count. If such a condition is detected, and if at least 1 is expected to be jammed into the MSB counter, the detection logic removes one from the number to be jammed into the MSB counter (with a place value of 2000 times the divide-by-mode) and jams the same 2000 into the CD4059A by forcing terminals 6, 7, and 9 high.

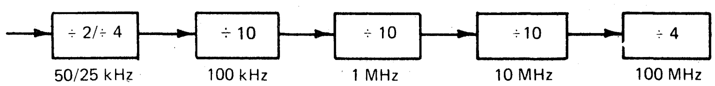
The clock of the CD4013A may be driven directly from the output of the CD4059A, as shown by dashed option (1), or by the inverted output of the CD4059A, option (2). If option (2) is used the CD4029A cannot count cycles shorter than 3. If option (1) is used propagation delay problems may occur at high counting speeds.

The general circuit in Fig.14 can be simplified considerably if the range of the cascaded counters does not have to start at a very low value. Fig.15 shows an arrangement in the ÷ 4 mode, where the counting range extends in a BCD-switch compatible manner from 88,003 to 103,999. The arrangement shown in Fig.15 is easy to follow; once during each cycle, the less significant digits are jammed in (14,712 in this case) and then 11,000 (4 x 2750) is jammed in eight times in succession, by forcing jam inputs high or low, as required.

Numbers larger than the extended counter range can also be produced by cascading the CD4059A with some other counting device. Fig.16 shows such an arrangement where only one fixed divide-by number is desired which is close to three times the extended counter range as shown in the last column of Table I. The dual flip-flop wired to produce a ÷ 3 count, can be replaced by other counters such as the CD4029, CD4510, CD4516, CD4017, or the CD4022. In Fig.16 the ÷ N subsystem is preset once to a number smaller than the desired divide-by number. This smaller number represents the less significant digits of the divide-by number. The subsystem is then preset one or more times to a round number (e.g. 1000, 2000) and multiplied by the number of the divide-by mode (÷ 2 in the example of Fig.16). It is important that the second counting device has an output that is high or low, as the case may be, during only one of its counting states.

CD4059A Types

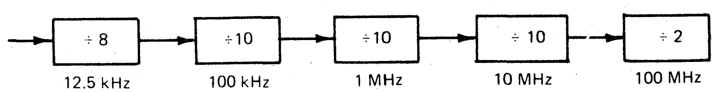
2) ÷ N Counter Configuration for UHF – 220 to 400 MHz
Channel Spacing: 50 kHz or 25 kHz



$$N_{Max} = \frac{400\ \text{MHz}}{25\ \text{kHz}} = 16{,}000 \qquad N_{Max} = \frac{400\ \text{MHz}}{50\ \text{kHz}} = 8{,}000$$

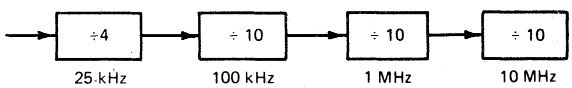
$$N_{Min} = \frac{220\ \text{MHz}}{25\ \text{kHz}} = 8{,}800 \qquad N_{Min} = \frac{220\ \text{MHz}}{50\ \text{kHz}} = 4{,}400$$

3) ÷ N Counter Configuration to VHF – 116 MHz
Channel Spacing = 12.5 kHz



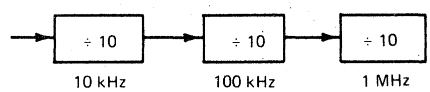
$$N_{Max} = \frac{160\ \text{MHz}}{12.5\ \text{kHz}} = 12{,}800 \qquad N_{Min} = \frac{116\ \text{MHz}}{12.5\ \text{kHz}} = 9{,}300$$

4) ÷ N Counter Configuration for VHF – 30 to 80 MHz
Channel Spacing: 25 kHz



$$N_{Max} = \frac{80\ \text{MHz}}{25\ \text{kHz}} = 3{,}200 \qquad N_{Min} = \frac{30\ \text{MHz}}{25\ \text{kHz}} = 1200$$

5) ÷ N Counter Configuration for AM – 995 to 2055 kHz
Channel Spacing = 10 kHz



$$N_{Max} = \frac{2055\ \text{kHz}}{10\ \text{kHz}} = 205 \qquad N_{Min} = \frac{995\ \text{kHz}}{10\ \text{kHz}} = 99$$

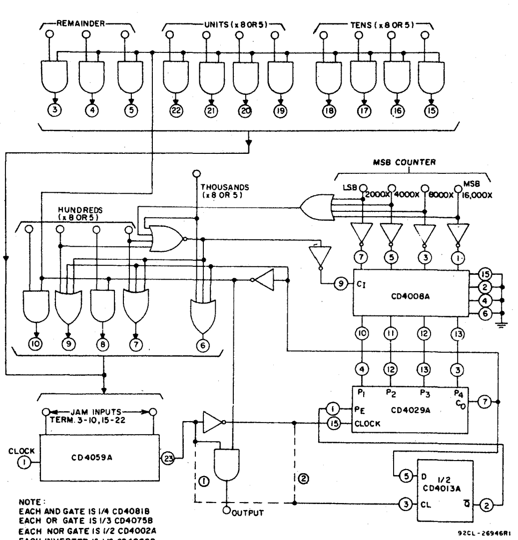


Fig. 14 – BCD switch-compatible ÷N system of the most general kind.

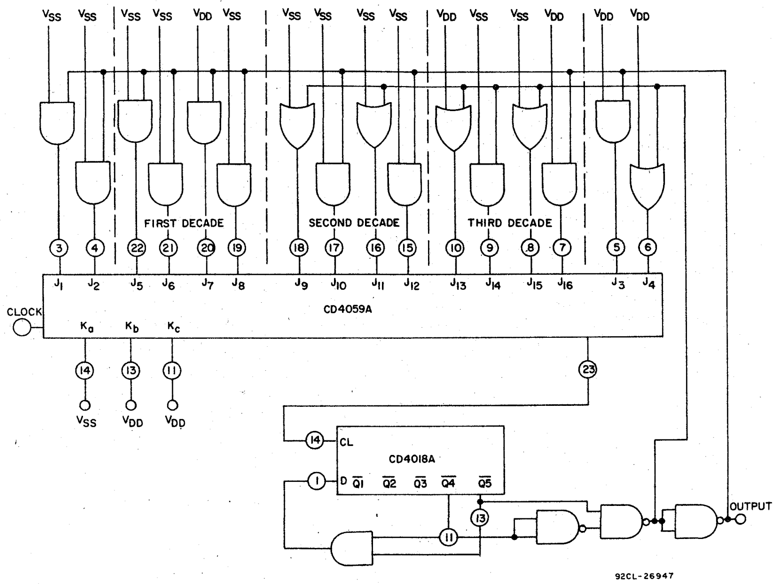


Fig.15 – Dividing by any number from 88,003 to 103,999.

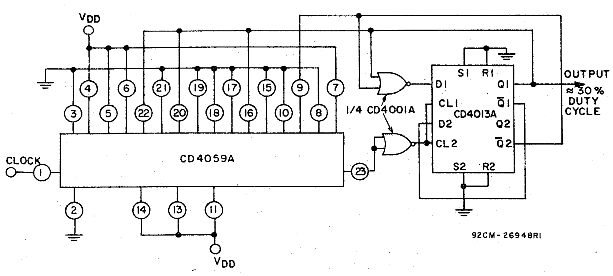


Fig.16 – Division by 47,690 in ÷2 mode.

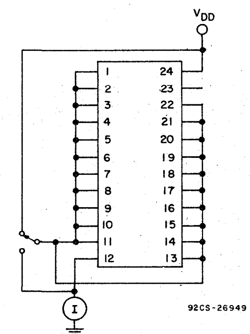


Fig.17 – Quiescent device current test circuit.

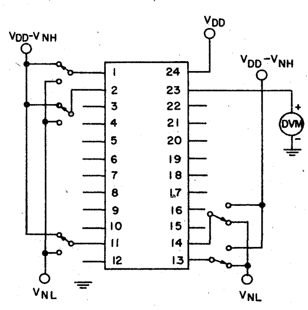


Fig.18 – Noise immunity test circuit.

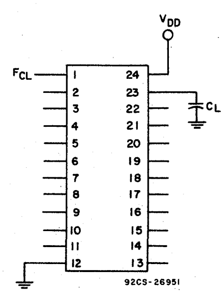


Fig.19 – Power dissipation test circuit (all ÷ modes).

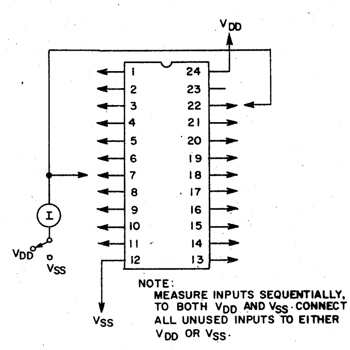
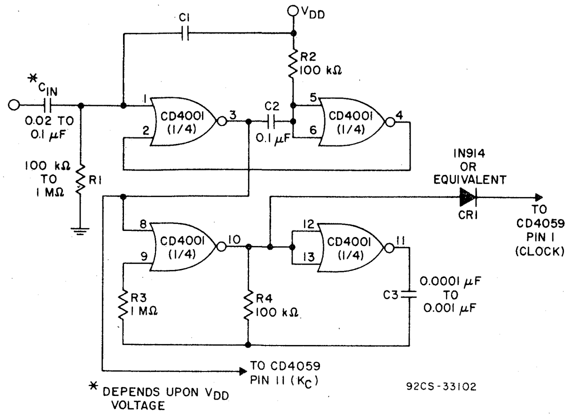
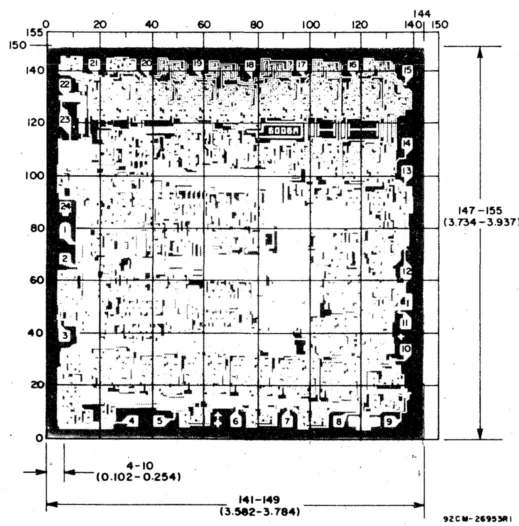


Fig.20 – Input leakage current test circuit.



For changing from any mode other than mode 5 (with power on), apply positive pulse to C_{in}. This circuit automatically selects master preset mode ($K_b = 0$, $K_c = 0$) before going into the select conditions for mode 5 ($K_a = 1$, $K_b = 0$, $K = 1$). The selection of C_1 and C_2 is critical. C_1 is determined by the VDD voltage--the lower VDD's need larger C_1's. C_2 must be 0.1 μF or larger.

Fig.21 - CD4059A mode 5 power on master preset circuit.



The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for CD4059AH.

COS/MOS 14-Stage Ripple-Carry Binary Counter/Divider and Oscillator

The RCA-CD4060A consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which resets the counter to the all-O's state and disables the oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of $\phi_I (\phi_O)$. All inputs and outputs are fully buffered.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

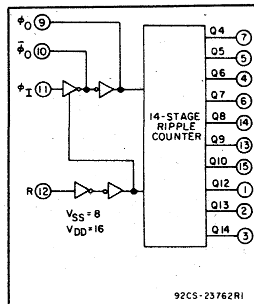
- **4-MHz operating frequency (typ.) at $V_{DD} - V_{SS}$ = 10 V**
- **Common reset**
- **Fully static operation**
- **10 buffered outputs available**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 µA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Oscillator Features:

- **All active components on chip**
- **RC or crystal oscillator configuration**

Applications:

- **Timers**
- **Frequency dividers**



CD4060A FUNCTIONAL DIAGRAM

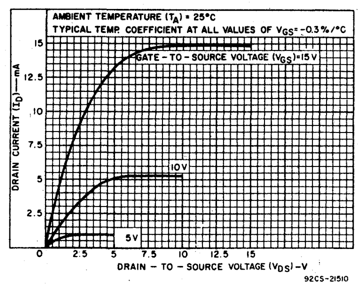


Fig. 1 — Typical n-channel drain characteristics.

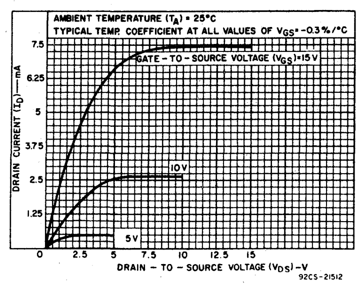


Fig. 2 – Minimum n-channel drain characteristics.

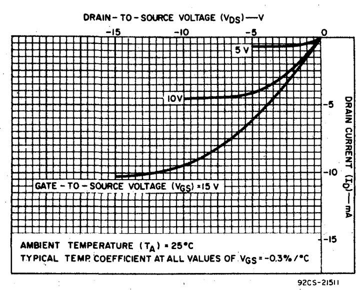


Fig. 3 — Typical p-channel drain characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . –55 to +125°C
PACKAGE TYPE E . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A= –40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
FOR T_A= +60 to +85°C (PACKAGE TYPE E) . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A= –55 to +100°C (PACKAGE TYPES D, F) . . . . 500 mW
FOR T_A= +100 to +125°C (PACKAGE TYPES D, F) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A= FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	VDD (V)	LIMITS D,F,H Packages Min.	Max.	E Package Min.	Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Input-Pulse Width, t_W f = 100 kHz	5 10	400 110	– –	500 125	– –	ns
Input-Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$	5 10	– –	15 7.5	– –	15 7.5	µs
Input-Pulse Frequency, f_ϕ	5 10	– –	1 3	– –	0.9 2.75	MHz
Reset Pulse Width, t_W	5 10	1000 500	– –	1250 600	– –	ns

CD4060A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	+25 Typ.	+25 Limit	+125	–40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	15	0.5	15	900	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	2.5	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	10	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current:* n-Channel (Sink), I_DN Min.	0.5	–	5	0.22	0.36	0.18	0.125	0.21	0.36	0.18	0.15	mA
	0.5	–	10	0.44	0.75	0.36	0.25	0.42	0.75	0.36	0.3	
p-Channel (Source), I_DP Min.	4.5	–	5	-0.15	-0.25	-0.125	-0.085	-0.145	-0.25	-0.125	-0.1	
	9.5	–	10	-0.3	-0.5	-0.25	-0.175	-0.29	-0.5	-0.25	-0.2	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm10^{-5}$ Typ., ±1 Max.								μA

* Data not applicable to Terminal 9 or 10

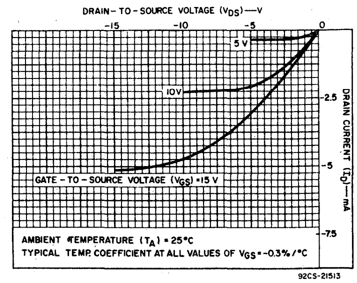


Fig. 4 – Minimum p-channel drain characteristics.

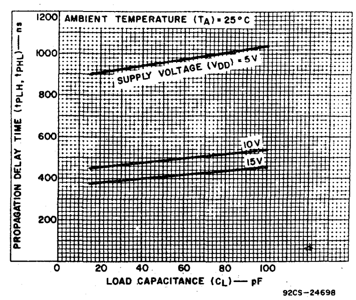


Fig. 5 – Typical propagation delay time vs. load capacitance (ϕ_I to Q4 output).

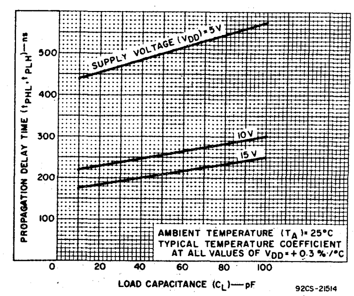


Fig. 6 – Typical propagation delay time vs. load capacitance (Q_n to Q_{n+1}).

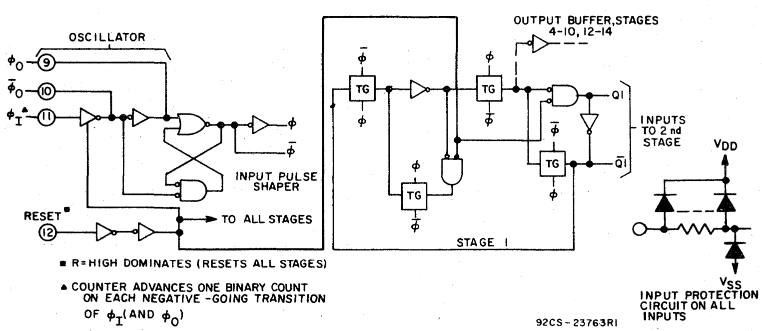


Fig. 7 – Logic diagram of CD4060A oscillator, pulse shaper, and 1 of 14 counter stages.

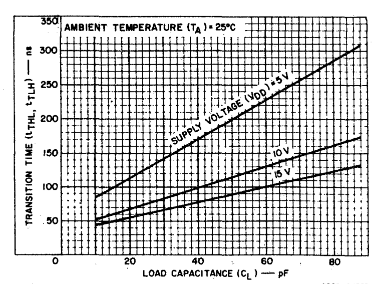


Fig. 8 – Typical output transition time vs. load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D,F,H Packages			*E Package*			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input-Pulse Operation									
Propagation Delay Time, ϕ_I to Q4 Out; t_{PHL}, t_{PLH}		5	–	900	1800	–	900	1900	ns
		10	–	450	900	–	450	950	
Propagation Delay Time, Q_n to Q_{n+1}; t_{PHL}, t_{PLH}		5	–	450	900	–	450	950	ns
		10	–	225	450	–	225	475	
Transition Time, t_{THL}, t_{TLH}		5	–	150	300	–	150	350	ns
		10	–	75	150	–	75	175	
Min. Input-Pulse Width t_W	f=100 kHz	5	–	200	400	–	200	500	ns
		10	–	75	110	–	75	125	
Input-Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$		5	–	–	15	–	–	15	μs
		10	–	–	7.5	–	–	7.5	
Max. Input-Pulse Frequency, f_ϕ		5	1	1.75	–	0.9	1.75	–	MHz
		10	3	4	–	2.75	4	–	
Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
Reset Operation									
Propagation Delay Time, t_{PHL}		5	–	500	1000	–	500	1250	ns
		10	–	250	500	–	250	600	
Minimum Reset Pulse Width, t_W		5	–	500	1000	–	500	1250	ns
		10	–	250	500	–	250	600	

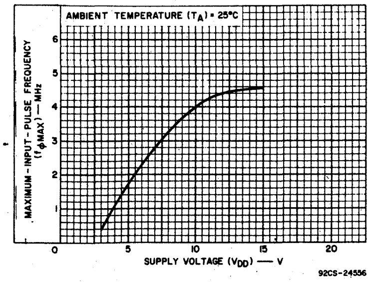


Fig. 9 – Typical maximum-input-pulse frequency vs. supply voltage.

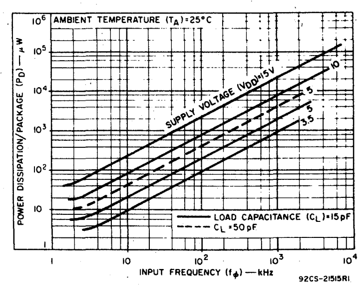


Fig. 10 – Typical dynamic power dissipation characteristics.

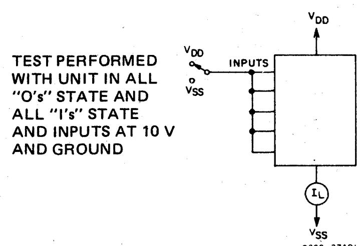


Fig. 11 – Quiescent-device current test circuit.

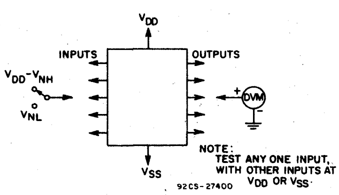


Fig. 12 – Noise-immunity test circuit.

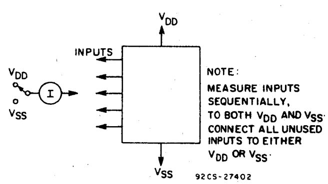


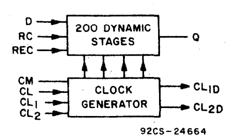
Fig. 13 – Input-leakage-current test circuit.

CD4062A Types

COS/MOS 200-Stage Dynamic Shift Register

MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150° C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES T, H	-55 to +125° C
DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal):	-0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)	
FOR T_A = -55 to +100° C (PACKAGE TYPES T)	500 mW
FOR T_A = +100 to +125° C (PACKAGE TYPES T)	Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265° C



CD4062A
FUNCTIONAL DIAGRAM

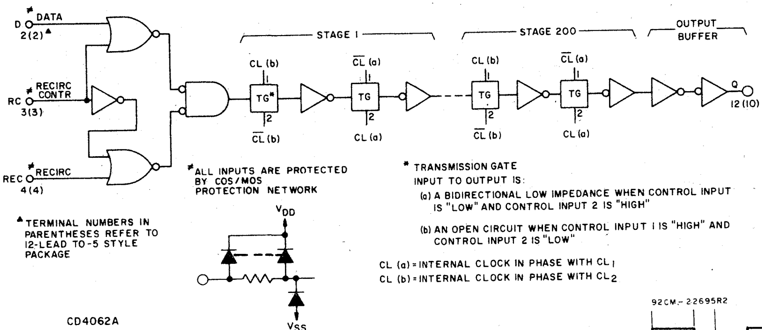


Fig. 1 – CD4062A logic block diagram.

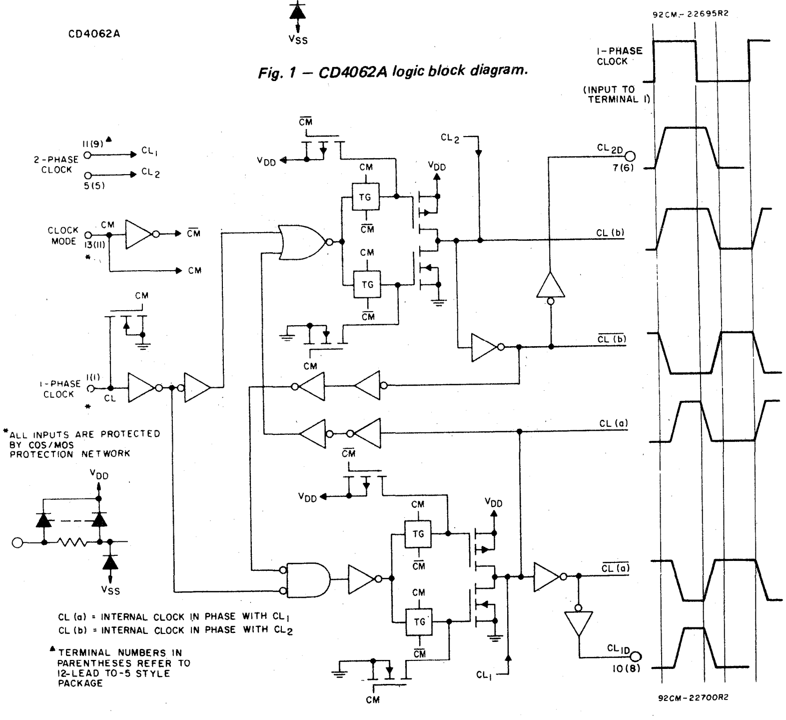


Fig. 2 – Clock circuit logic diagram.

The RCA-CD4062A is a 200-stage dynamic shift register with provision for either single- or two-phase clock input signals. Single-phase-clocked operation is intended for low-power, low clock-line capacitance requirements. Single-phase clocking is specified for medium-speed operation (< 1 MHz) at supply voltages up to 10 volts. Clock input capacitance is extremely low (< 5 pF), and clock rise and fall times are non-critical. The clock-mode signal (CM) must be low for single-phase operation.

Two-phase clock-input signals may be used for high-speed operation (up to 5 MHz) or to further reduce clock rise and fall time requirements at low speeds. Two-phase operation is specified for supply voltages up to 15 volts. Clock input capacitance is only 50 pF/phase. The clock-mode signal (CM) must be high for two-phase operation. The single-phase-clock input has an internal pull-down device which is activated when CM is high and may be left unconnected in two-phase operation.

The logic level present at the data input is transferred into the first stage and shifted one stage at each positive-going clock transition for single-phase operation, and at the positive-going transition of CL_1 for two-phase operation.

The CD4062A-Series types are supplied in 12-lead hermetic TO-5 packages (T suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Minimum shift rates over full temperature range—**

  Single-phase clock: 3 V ≤ V_{DD} ≤ 10 V; f_{min} = 10 kHz; -55° C ≤ T_A ≤ +125° C (f_{min} = 1 kHz up to T_A ≤ 75° C)

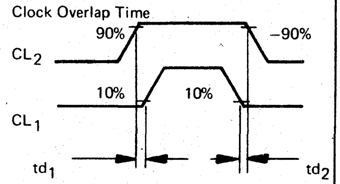
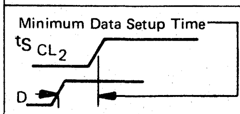
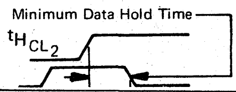
  Two-phase clock: 3 V ≤ V_{DD} ≤ 15 V; f_{min} = 10 kHz; -55° C ≤ T_A ≤ +125° C (f_{min} = 1 kHz up to T_A ≤ 75° C)

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range): Single-Phase Clock		3	10	V
Two-Phase Clock		3	12	V
Clock Input Frequency, f_{CL}*	5	0.15	500	kHz
	10	0.15	1000	kHz
Clock Pulse Width, t_W*	5	250	66.7 X 10⁶	ns
	10	500	66.7 X 10⁶	ns
Clock Rise or Fall Times, t_rCL or t_fCL*	5	–	10	μs
	10	–	1	μs
Data Hold Time, t_H*	5	150	–	ns
	10	50	–	ns

* For single-phase clock, 50% duty cycle

Two-Phase Clock Operation (CL_1, CL_2); Clock Mode (CM) = High; 3 V ≤ V_{DD} ≤ 15 V. See Figure 4.

CHARACTERISTIC	TEST CONDITIONS	V_{DD} V	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Maximum Clock Input Frequency, f_{CL}		5	1.25	2.5	–	MHz
		10	2.5	5	–	MHz
Minimum Clock Input Frequency, f_{CL}		5	150	10	–	Hz
		10	150	10	–	Hz
Clock Overlap Time 			40	–	–	ns
Average Input Capacitance, C_I CL_1, CL_2			–	50	–	pF
Propagation Delays; t_{PHL}, t_{PLH} CL_1 to Q		5	–	250	500	ns
		10	–	100	200	ns
CL_1 to CL_{1D}, CL_2 to CL_{2D}		5	–	250	500	ns
		10	–	100	200	ns
Minimum Data Setup Time t_S 		5	–	150	300	ns
		10	–	50	100	ns
Minimum Data Hold Time t_H 		5	–	–	0	ns
		10	–	–	0	ns
Clock Rise and Fall Times t_rCL_1, CL_2 t_fCL_1, CL_2			No Restrictions If Clock Overlap Requirement Is Met			

Features (Cont'd):

- **Low power dissipation**
  0.3 mW/bit at 1 MHz and 10 V
  0.04 mW/bit at 0.5 MHz and 5V
  (alternating 1-0 data pattern)
- **Data output TTL-DTL compatible**
- **Recirculating capability**
- **Delayed two-phase clock outputs available for cascading registers**
- **Asynchronous ripple-type presettable to all 1's or 0's**
- **Ultra-low-power-dissipation standby operation**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Serial shift registers**
- **Time-delay circuits**
- **CRT refresh memory**
- **Long serial memory**

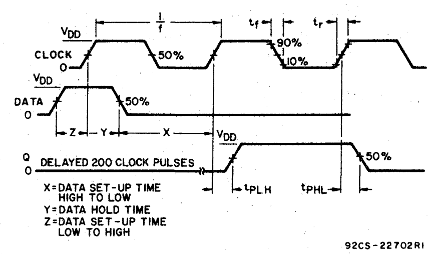


Fig. 3 – Timing diagram–single-phase clock.

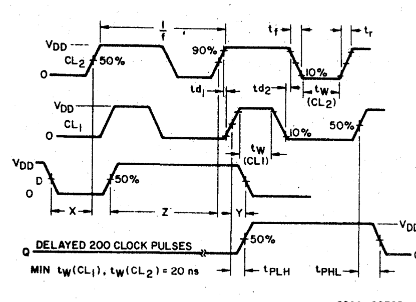


Fig. 4 – Timing diagram–two-phase clock.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)				UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	
Quiescent Device Current, I_L Max. CM=High, CL_1=High, CL_2=Low	–	–	5	12	0.5	12	720	μA
	–	–	10	25	1	25	1500	μA
	–	–	15	50	1	50	2000	μA
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max				V
	–	10	10	0 Typ.; 0.05 Max				V
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.				V
	–	0	10	9.95 Min.; 10 Typ.				V
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.				V
	9	–	10	3 Min.; 4.5 Typ.				V
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.				V
	1	–	10	3 Min.; 4.5 Typ.				V
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.				V
	9	–	10	1 Min.				V
Inputs High, V_{NMH}	0.5	–	5	1 Min.				V
	1	–	10	1 Min.				V
Output Drive Current: N-Channel (Sink), I_DN Min. Q Output	0.4	–	4.5	1.6	2.6	1.3	0.91	mA
	0.5	–	10	5	8*	4	3.2	mA
CL_{1D}, CL_{2D}	0.5	–	5	0.87	1.4	0.7	0.49	mA
	0.5	–	10	2.2	3.6	1.8	1.26	mA
P-Channel (Source):	4.5	–	5	-0.31	-0.5	-0.25	-0.17	mA
I_DP Min. Q Output	2.5	–	5	-0.93	-1.5	-0.75	-0.52	mA
	9.5	–	10	-0.87	-1.4	-0.7	-0.49	mA
CL_{1D}, CL_{2D}	4.5	–	5	-0.43	-0.7	-0.35	-0.24	mA
	9.5	–	10	-1.1	-1.8	-0.9	-0.63	mA
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	±10^{-5} Typ., ±1 Max.				μA

* Maximum power dissipation rating ⩽ 200 mW.

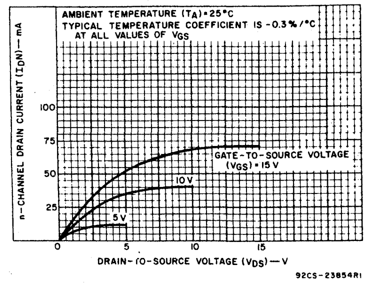


Fig. 5— Typical n-channel drain characterstics for Q output.

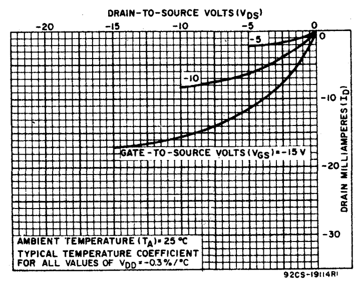


Fig. 6— Typical p-channel drain characteristics for Q output.

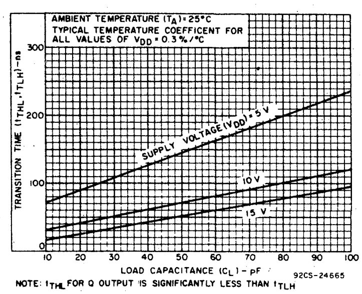


Fig. 7— Typical transition time vs. C_L for data outputs.

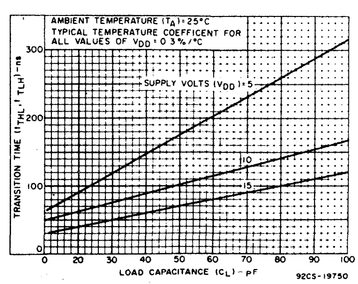


Fig. 8— Typical transition time vs. C_L for delayed clock output.

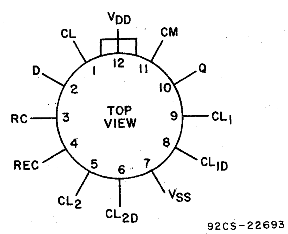
DYNAMIC CHARACTERISTICS AT T_A = 25°C, V_{SS} = 0 V, C_L = 50 pF, Input t_r, t_f = 20 ns, except t_rCL and t_fCL

Single-Phase-Clock Operation; Clock Mode (CM) = Low; 3 V ⩽ V_{DD} ⩽ 10 V (See Figure 3)

CHARACTERISTIC	TEST CONDITIONS	V_{DD} V	LIMITS MIN.	TYP.	MAX.	UNITS
Maximum Clock Input Frequency, f_{CL} (50% Duty Cycle)	t_r, t_f=20 ns	5	0.5	1	–	MHz
		10	1	2	–	
Minimum Clock Input Frequency, f_{CL} (50% Duty Cycle)		5	150	10	–	Hz
		10	150	10	–	
Clock Rise and Fall Times** t_rCL, t_fCL		5	–	–	10	μs
		10	–	–	1	
Average Input Capacitance, C_I	All Inputs Except CL_1 and CL_2		–	5	–	pF
Propagation Delays: CL to Q		5	–	1000	2000	ns
		10	–	400	800	
CL to CL_{1D} (Positive Going)	(50% Points)	5	–	750	1500	ns
		10	–	300	600	
CL to CL_{2D} (Positive Going)	(50% Points)	5	–	500	1000	
		10	–	200	400	
CL to CL_{1D} (Negative Going)	(50% Points)	5	–	450	900	
		10	–	175	350	
CL to CL_{2D} (Negative Going)	(50% Points)	5	–	750	1500	
		10	–	300	600	
Transition Time: t_{TLH}, t_{THL} Q Output		5	–	100	200	ns
		10	–	50	100	
CL_{1D}, CL_{2D}		5	–	200	400	
		10	–	100	200	
Data Set-Up Time t_S		5	–	–	0	ns
		10	–	–	0	
▲Data Hold Time t_H		5	–	–	150	ns
		10	–	–	150	

** If more than one unit is cascaded in single-phase parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 15 pF, and the transition time of the output driving stage. (See Figs. 5 and 7 for cascading options.)

▲ Use of delayed clock permits high-speed logic to precede CD4062A register (see cascade register operation).



CD4062AT
TERMINAL DIAGRAM

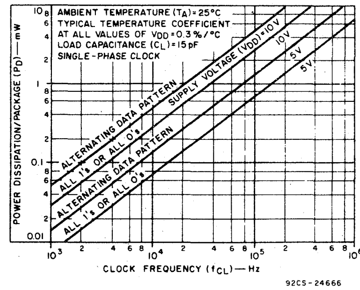


Fig. 9— Typical power dissipation vs. frequency.

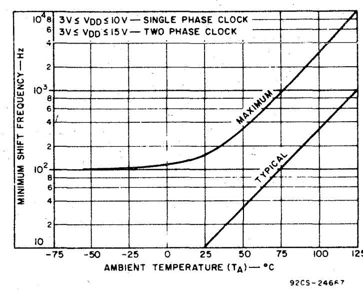


Fig. 10— Minimum shift frequency vs. ambient temperature.

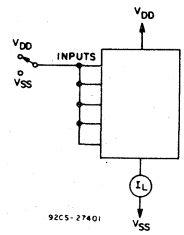


Fig. 11— Quiescent-device-current test circuit.

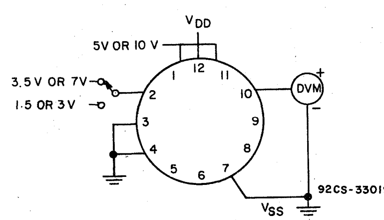


Fig. 12— Noise-immunity test circuit.

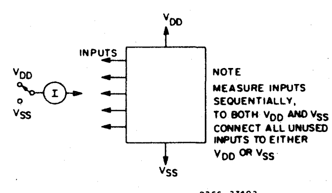


Fig. 13—Input-leakage-current test circuit.

CD4066A Types

COS/MOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

RCA CD4066A is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with RCA-CD4016, but exhibits a much lower ON resistance. In addition, the ON resistance is relatively constant over the full input-signal range.

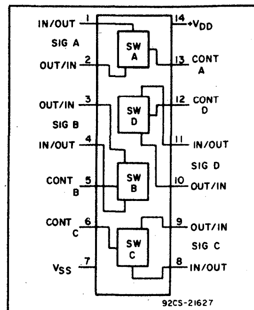
The CD4066A consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased ON or OFF simultaneously by the control signal. As shown in Fig. 1, the well of the n-channel device on each switch is either tied to the input when the switch is ON or to V_{SS} when the switch is OFF. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the ON resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant ON impedance over the input-signal range. For sample-and-hold applications, however, the CD4016 is recommended.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **15-V digital or ± 7.5-V peak-to-peak switching**
- **80Ω typical ON resistance for 15-V operation**
- **Switch ON resistance matched to within 5 Ω over 15-V signal-input range**
- **ON resistance flat over full peak-to-peak signal range**
- **High ON/OFF output-voltage ratio: 65 dB typ. @ f_{is} = 10 kHz, R_L = 10 kΩ**
- **High degree of linearity: < 0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 V_{p-p}, $V_{DD}-V_{SS} \geq$ 10 V, R_L = 10 kΩ**
- **Extremely low OFF switch leakage resulting in very low offset current and high effective OFF resistance: 10 pA typ. @ $V_{DD}-V_{SS}$ = 10 V, T_A = 25°C**
- **Extremely high control input impedance (control circuit isolated from signal circuit): 10^{12} Ω typ.**
- **Low crosstalk between switches: -50 dB typ. @ f_{is} = 0.9 MHz, R_L = 1 kΩ**
- **Matched control-input to signal-output capacitance: Reduces output signal transients**
- **Frequency response, switch ON = 40 MHz (typ.)**
- **Quiescent current specified to 15-V**
- **Maximum control input leakage current of 1-μA at 15-V (Full package-temperature range)**



CD4066A
FUNCTIONAL DIAGRAM

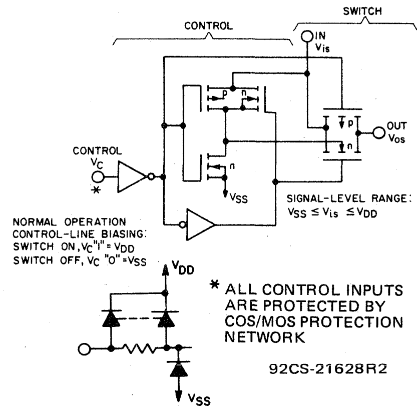


Fig. 1 – Schematic diagram of 1 of 4 identical switches and its associated control circuitry.

SPECIAL CONSIDERATIONS – CD4066A

1. In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 CD4066A bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from CD4066A.
2. In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown).

   No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10.
3. Minimum bilateral switch output load resistance is 100 Ω.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE TEMPERATURE RANGE (T_{stg}) . . . . -65 to +125°C
OPERATING TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H. . . . . -55 to +125°C
PACKAGE TYPE E . . . . -40 to +85°C
DC SUPPLY VOLTAGE RANGE, V_{DD}
(Voltages referenced to V_{SS}) . . . . -0.5 to +15 V
INPUT CURRENT (TRANSMISSION GATE INCL.) . . . . ±10 mA
POWER DISSIPATION PER PACKAGE:
FOR T_A = -40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C . . . . . . 200 mW
FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K) . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) Derate Linearly at 12 mW/°C . . . 200 mW
DEVICE DISSIPATION PER SECTION:
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . . 100 mW
ALL SIGNAL AND DIGITAL CONTROL INPUTS . . . . $V_{SS} \leq V_I \leq V_{DD}$
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

OPERATING CONDITIONS AT T_A = 25°C

For maximum reliability, nominal operating conditions should be selected *so that operation is always within the following ranges.*

CHARACTERISTIC	V_{DD}	MIN.	MAX.	UNITS
Supply Voltage Range (T_A = Full Package Temperature Range)	–	3	12	V

Applications:

- Analog signal switching/multiplexing
  - Signal gating   Modulator
  - Squelch control   Demodulator
  - Chopper   Commutating switch
- Digital signal switching/Multiplexing
- Transmission-gate logic implementation
- Analog-to-digital & digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS *All Voltage Values Are in Volts*			LIMITS Values at -55°C, +25°C, +125°C Apply to D, F, H Packages; Values at -40°C, +25°C, +85°C Apply to E Package						UNITS
			V_{DD} (V)	-55°	-40°	+85°	+125°	+25° TYP.	+25° MAX.	
Quiescent Device Current, I_L max. D, F, H Pkgs.			5	0.25	–	–	7.5	0.01	0.25	μA
			10	0.5	–	–	15	0.01	0.5	
			15	2	–	–	40	0.02	2	
E Pkg.			5	–	2.5	15	–	0.25	2.5	μA
			10	–	5	30	–	0.25	5	
			15	–	50	500	–	0.5	50	
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})										
	$V_C = V_{DD}$	V_{SS}	V_{is}							
ON Resistance, R_{ON} Max.	$R_L = 10kΩ$•									Ω
	+7.5	-7.5	-7.5 to +7.5	220	250	300	320	80	280	
	+15	0	0 to +15							
	+5	-5	-5 to +5	400	450	520	550	120	500	
	+10	0	0 to +10							
	+2.5	-2.5	-2.5 to +2.5	3000	3500	5200	5500	270	5000	
	+5	0	0 to +5							
Δ ON Resistance Between Any 2 of 4 Switches, ΔR_{ON}	$R_L = 10kΩ$•									Ω
	+7.5 or +15	-7.5 or 0	+7.5 to -7.5 / +15 to 0	–	–	–	–	5	–	
	+5 or +10	-5 or 0	+5 to -5 / +10 to 0	–	–	–	–	10	–	
Sine Wave Response (Distortion)	+5	-5	5V p-p▲	–	–	–	–	0.4	–	%
	$R_L = 10kΩ$, $f_{is} = 1kHz$									
Frequency Response Switch ON (Sine-Wave Input)	+5	-5	-5 p-p	–	–	–	–	40	–	MHz
	$R_L = 1kΩ$, $20 \log_{10} \frac{V_{os}}{V_{is}} = -3dB$									
Feedthrough-Switch OFF	+5	-5	-5 p-p	–	–	–	–	1.25	–	MHz
	$R_L = 1kΩ$, $20 \log_{10} \frac{V_{os}}{V_{is}} = -50dB$									
Input or Output Leakage – Switch OFF (Effective OFF Resistance)	V_{DD}	$V_C = V_{SS}$								
	+7.5	-7.5	±7.5	–	–	–	–	±0.1	±100*	nA
	+5	-5	±5	–	–	–	–	±0.1	±100*	
Crosstalk Between Any 2 of the 4 Switches (f at –50 dB)	$V_C(A)=V_{DD}=+5$, $V_C(B)=V_{SS}=-5$, $R_L = 1kΩ$, $20 \log_{10} \frac{V_{os}(B)}{V_{is}(A)} = -50dB$		(A) 5V p-p	–	–	–	–	0.9	–	MHz

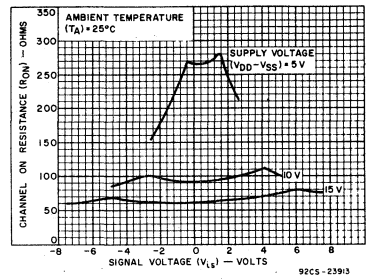


Fig. 2 (a) – Typical channel ON resistance vs. signal voltage for three values of supply voltage ($V_{DD}-V_{SS}$).

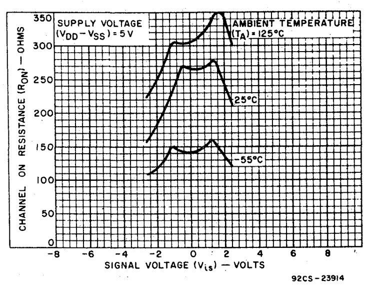


Fig. 2 (b) – Typical channel ON resistance vs. signal voltage with supply voltage ($V_{DD}-V_{SS}$) = 5 V.

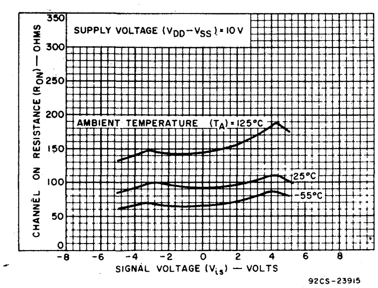


Fig. 2 (c) – Typical channel ON resistance vs. signal voltage with supply voltage ($V_{DD}-V_{SS}$) = 10 V.

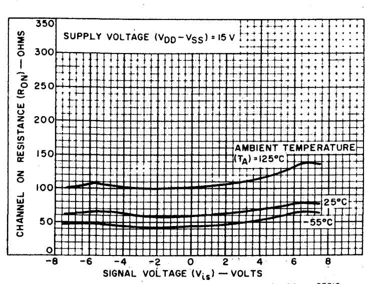


Fig. 2 (d) – Typical channel ON resistance vs. signal voltage with supply voltage ($V_{DD}-V_{SS}$) = 15 V.

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS (All Voltage Values Are in Volts)	V_{DD} (V)	LIMITS: -55°	-40°	+85°	+125°	+25° TYP.	+25° MAX.	UNITS
			Values at -55°C, +25°C, +125°C Apply to D, F, H Packages. Values at -40°C, +25°C, +85°C Apply to E Package						
Propagation Delay (Signal Input to Signal Output) t_{pd}	$V_C = V_{DD}$, V_{SS} = GND, C_L = 15pF, V_{is} = sq. wave, t_r, t_f = 20 ns (Input Signal)	V_{DD} = 5	–	–	–	–	20	50	ns
		V_{DD} = 10	–	–	–	–	10	25	ns
Capacitance: Input, C_{is}	V_{DD} = +5, $V_{CC} = V_{SS}$ = -5		–	–	–	–	8	–	pF
Output, C_{os}			–	–	–	–	8	–	pF
Feedthrough, C_{ios}			–	–	–	–	0.5	–	pF
CONTROL (V_C)									
Noise Immunity, V_{NL} Min.	$V_{is} \leq V_{DD}$, I_{is} = 10µA, $V_{DD} - V_{SS}$ = 10		2	2	2	2	2 min 4.5	–	V
Input Leakage Current, I_{IL} Max.	$V_{is} \leq V_{DD}$, $V_{DD} - V_{SS}$ = 15, $V_C \leq V_{DD} - V_{SS}$		±1				$\pm10^{-6}$	±1	µA
Crosstalk Control Input to Signal Output	$V_{DD}-V_{SS}$ = 10, V_C = 10 (sq. wave), R_L = 10kΩ		–	–	–	–	50	–	mV
Propagation Delay, t_{pdC}	$t_{rc} = t_{fc}$ = 20 ns, R_L = 300kΩ, $V_{is} \leq 10$, C_L = 15pF		–	–	–	–	35	–	ns
Maximum Allowable Control Input Repetition Rate	V_{DD} = 10, V_{SS} = GND, R_L = 1kΩ, C_L = 15pF, V_C = 10 (sq. wave), t_r, t_f = 20 ns		–	–	–	–	10	–	MHz
Av. Input Capacitance, C_I			–	–	–	–	5	–	pF

* Limit determined by minimum feasible leakage measurement for automatic testing.

△ Symmetrical about 0 volts. • For all test conditions.

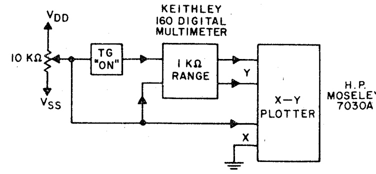


Fig. 3 – Channel ON resistance measurement circuit.

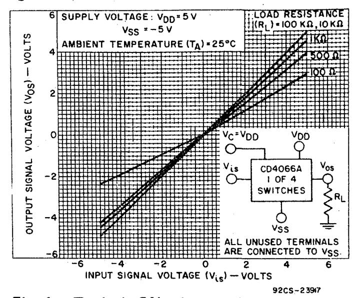


Fig. 4 – Typical ON characteristics for 1 of 4 channels.

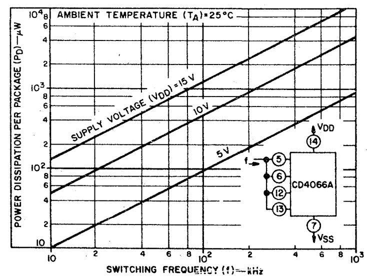


Fig. 5 – Power dissipation per package vs. switching frequency.

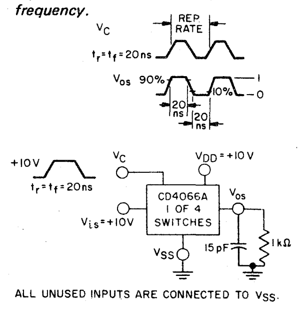


Fig. 10 - Maximum allowable control input repetition rate.

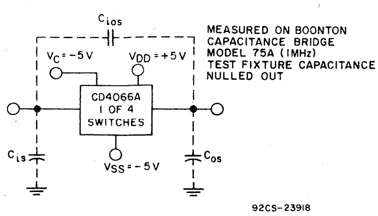


Fig. 6 – Capacitance test circuit.

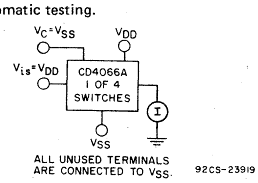


Fig. 7 – OFF switch input or output leakage.

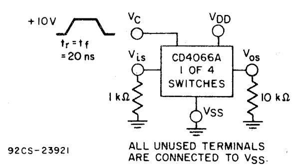


Fig. 9 – Crosstalk-control input to signal output.

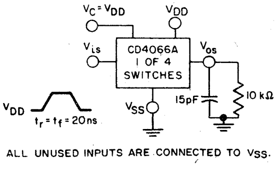


Fig. 8 – Propagation delay time signal input (V_{is}) to signal output (V_{os}).

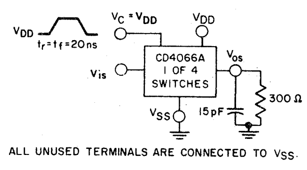


Fig. 11 – Propagation delay t_{PLH}, t_{PHL} control-signal output.

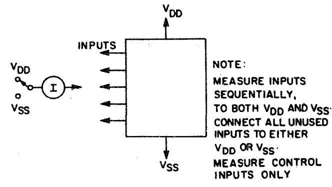


Fig. 12 – Input leakage current test circuit.

COS/MOS Telecommunications, Display-Driver, and Interface Circuits

Technical Data

CD22100 Types

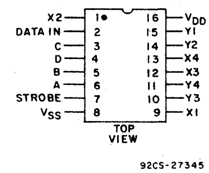
COS/MOS 4 x 4 Crosspoint Switch with Control Memory

High-Voltage Types (20-Volt Rating)

The RCA-CD22100 combines a 4 x 4 array of crosspoints (transmission gates) with a 4-line-to-16-line decoder and 16 latch circuits. Any one of the sixteen transmission gates (crosspoints) can be selected by applying the appropriate four line address. The selected transmission gate can be turned on or off by applying a logical one or zero, respectively, to the data input and strobing the strobe input to a logical one. Any number of the transmission gates can be ON simultaneously. When the required operating power is applied to the CD22100, the states of the 16 switches are indeterminate. Therefore, all switches must be turned off by putting the strobe high and data-in low, and then addressing all switches in succession.

Features:

- **Low ON resistance — 75 Ω typ. at V_{DD} = 12 V**
- **"Built-in" control latches**
- **Large analog signal capability — ± $V_{DD}/2$**
- **10-MHz switch bandwidth**
- **Matched switch characteristics ΔR_{ON} = 18Ω typ. at V_{DD} = 12 V**
- **High linearity — 0.5% distortion (typ.) at f = 1 kHz, V_{IN} = 5 V_{p-p}, V_{DD} = 10 V, and R_L = 1 kΩ**
- **Standard COS/MOS noise immunity**
- **100% tested for maximum quiescent current at 20 V**



Terminal Assignment

MAXIMUM RATINGS, ***Absolute-Maximum Values:***

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT*	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER TRANSMISSION GATE	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

* Maximum current through transmission gates (switches) = 25 mA.

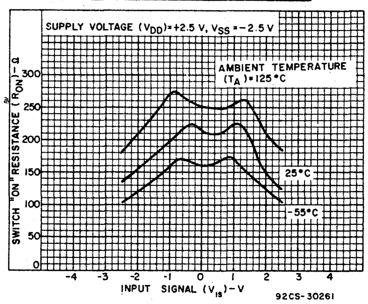


Fig. 2— Typical ON resistance as a function of input signal voltage at V_{DD} = $-V_{SS}$ = 2.5 V.

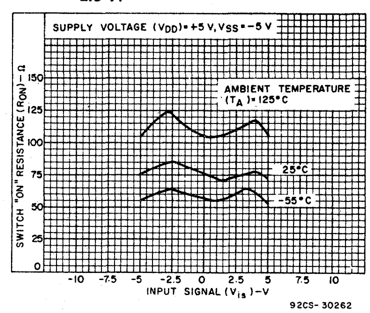


Fig. 3— Typical ON resistance as a function of input signal voltage at V_{DD} = $-V_{SS}$ = 5 V.

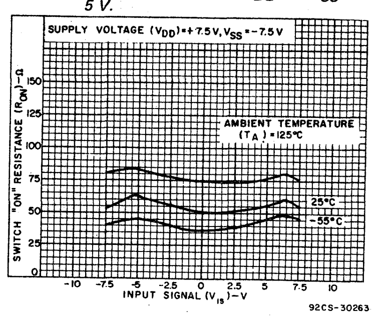


Fig. 4 — Typical ON resistance as a function of input signal voltage at V_{DD} = $-V_{SS}$ = 7.5 V.

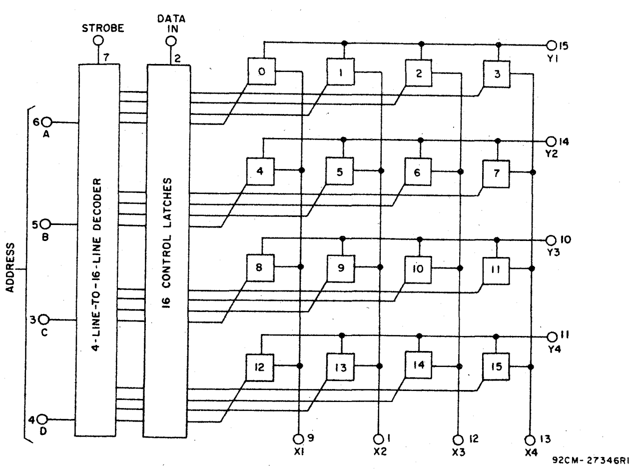


Fig. 1 — Functional diagram.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

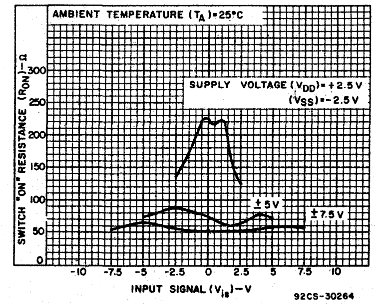


Fig. 5— Typical ON resistance as a function of input signal voltage at T_A = 25°C.

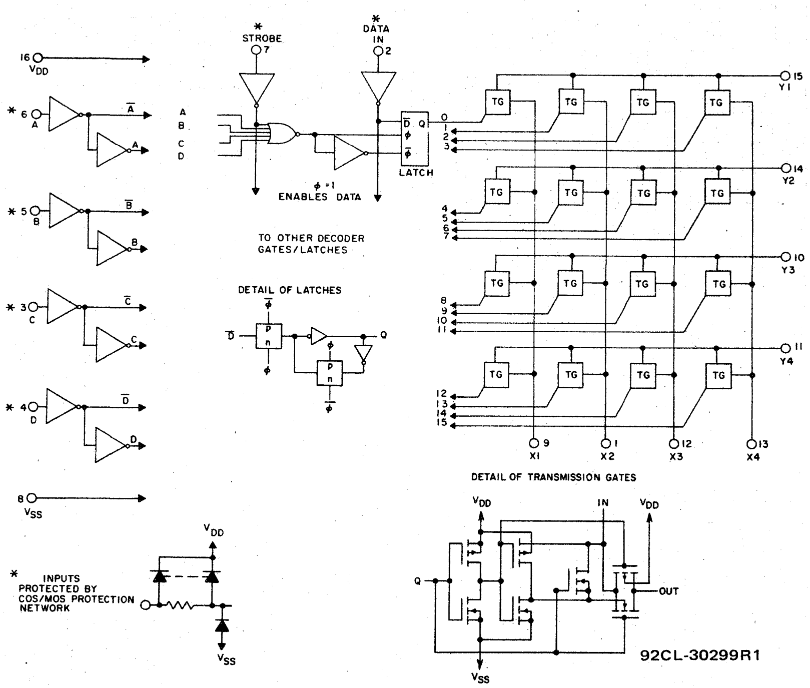


Fig. 6— Schematic diagram.

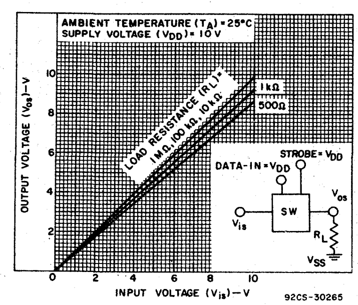


Fig. 7 — Typical switch ON transfer characteristics (1 of 16 switches).

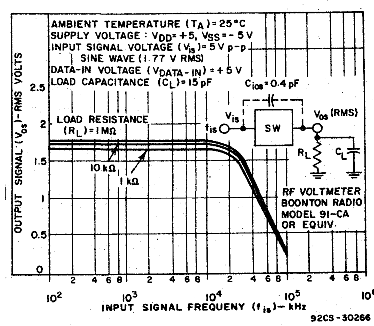


Fig. 8 — Typical switch ON frequency response characteristics.

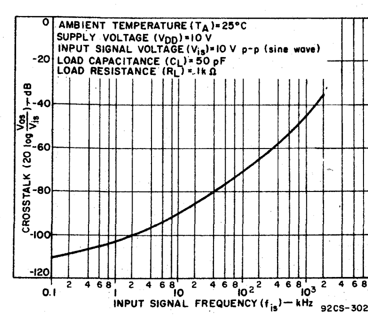


Fig. 9 — Typical crosstalk between switches as a function of signal frequency.

TRUTH TABLE

Address				Select	Address				Select
A	B	C	D		A	B	C	D	
0	0	0	0	X1Y1	0	0	0	1	X1Y3
1	0	0	0	X2Y1	1	0	0	1	X2Y3
0	1	0	0	X3Y1	0	1	0	1	X3Y3
1	1	0	0	X4Y1	1	1	0	1	X4Y3
0	0	1	0	X1Y2	0	0	1	1	X1Y4
1	0	1	0	X2Y2	1	0	1	1	X2Y4
0	1	1	0	X3Y2	0	1	1	1	X3Y4
1	1	1	0	X4Y2	1	1	1	1	X4Y4

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS	V_{IN} (V)	V_{DD} (V)	LIMITS at Indicated Temperature (°C) Values at −55,+25,+125,apply to D,F,H pkg Values at −40,+25,+85,apply to E pkg −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	Units
CROSSPOINTS											
Quiescent Device Current, I_{DD} Max.		–	5	5	5	150	150	–	0.04	5	µA
		–	10	10	10	300	300	–	0.04	10	
		–	15	20	20	600	600	–	0.04	20	
		–	20	100	100	3000	3000	–	0.08	100	
ON Resistance R_{ON} Max.	Any Switch V_{IS} = 0 to V_{DD}	–	5	450	1000	1440	1625	–	225	1250	Ω
		–	10	135	145	205	230	–	85	180	
		–	12	100	110	155	175	–	75	135	
		–	15	70	75	110	125	–	65	95	
ΔON Resistance, ΔR_{ON}	Between any two switches	–	5	–	–	–	–	–	35	–	Ω
		–	10	–	–	–	–	–	20	–	
		–	12	–	–	–	–	–	18	–	
		–	15	–	–	–	–	–	15	–	
OFF Switch Leakage Current I_L Max.	All switches OFF	0,18	18	±100		±1000		–	±1	±100*	nA
CONTROLS											
Input Low Voltage V_{IL} Max.	OFF switch I_L <0.2 µA	–	5	1.5				–	–	1.5	V
		–	10	3				–	–	3	
		–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	ON switch see R_{ON} characteristic	–	5	3.5				3.5	–	–	
		–	10	7				7	–	–	
		–	15	11				11	–	–	
Input Current, I_{IN} Max.	Any control	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	µA

* Determined by minimum feasible leakage measurement for automatic testing.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	CONDITIONS f_{is} kHz	R_L kΩ	V_{is}• (V)	V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
CROSSPOINTS								
Propagation Delay Time, (Switch ON) Signal Input to Output, t_{PHL}, t_{PLH}	–	10	5	5	–	30	60	ns
			10	10	–	15	30	
			15	15	–	10	20	
	C_L = 50 pF; t_r, t_f = 20 ns							
Frequency Response, (Any Switch ON)	1	1	5	10	–	40	–	MHz
	Sine wave input, $20 \log \frac{V_{os}}{V_{is}} = -3$ dB							
Sine Wave Response, (Distortion)	1	1	5	10	–	0.5	–	%
Feedthrough (All Switches OFF)	1.6	1	5	10	–	−80	–	dB
	Sine wave input							

•Peak-to-peak voltage symmetrical about $\frac{V_{DD}}{2}$.

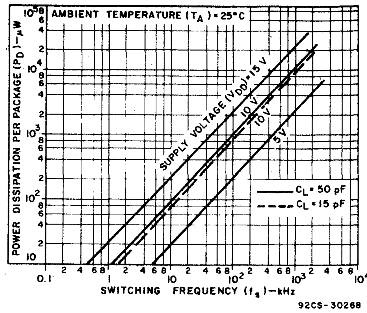


Fig. 10 – Typical dynamic power dissipation as a function of switching frequency.

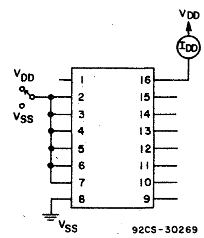


Fig. 11 – Quiescent current test circuit.

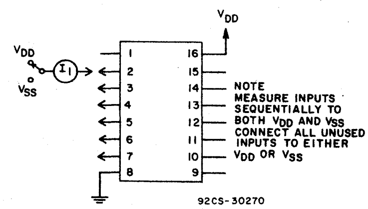


Fig. 12 – Input current test circuit.

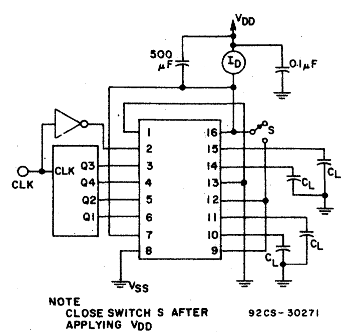


Fig. 13 – Dynamic power dissipation test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	CONDITIONS f_{is} kHz	R_L kΩ	V_{is}● (V)	V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
CROSSPOINTS (CONT'D)								
Frequency for Signal Crosstalk Attenuation of 40 dB	–	1	10	10	–	1.5	–	MHz
Attenuation of 110 dB	Sine wave input					0.1		kHz
Capacitance, X_n to Ground		–	–	5-15	–	18	–	pF
Y_n to Ground		–	–	5-15	–	30	–	pF
Feedthrough		–	–	–	–	0.4	–	pF
CONTROLS			See Fig.					
Propagation Delay Time: Strobe to Output, t_{PZH} (Switch Turn-ON to High Level)	R_L=1kΩ, C_L=50pF, t_r,t_f = 20 ns ↓		18	5	–	300	600	ns
				10	–	125	250	ns
				15	–	80	160	ns
Data-In to Output, t_{PZH} (Turn-On to High Level)	↓		19	5	–	110	220	ns
				10	–	40	80	ns
				15	–	25	50	ns
Address to Output, t_{PZH} (Turn-ON to High Level)	↓		20	5	–	350	700	ns
				10	–	135	270	ns
				15	–	90	180	ns
Propagation Delay Time: Strobe to Output, t_{PHZ} (Switch Turn-OFF)	↓		18	5	–	165	330	ns
				10	–	85	170	ns
				15	–	70	140	ns
Data-In to Output, t_{PZL} (Turn-ON to Low Level)	↓		19	5	–	210	420	ns
				10	–	110	220	ns
				15	–	100	200	ns
Address to Output, t_{PHZ} (Turn-OFF)	↓		20	5	–	435	870	ns
				10	–	210	420	ns
				15	–	160	320	ns
Minimum Setup Time, Data-In to Strobe, Address, t_{SU}	↓			5	–	95	190	ns
				10	–	25	50	ns
				15	–	15	30	ns
Minimum Hold Time, Data-In to Strobe, Address, t_H	↓			5	–	180	360	ns
				10	–	110	220	ns
				15	–	35	70	ns
Maximum Switching Frequency, f_ϕ	R_L=1kΩ, C_L=50 pF t_r, t_f = 20 ns			5	0.6	1.2	–	MHz
				10	1.6	3.2	–	MHz
				15	2.5	5	–	MHz
Minimum Strobe Pulse Width, t_W	R_L=1kΩ, C_L=50 pF t_r, t_f = 20 ns			5	–	300	600	ns
				10	–	120	240	ns
				15	–	90	180	ns
Control Crosstalk, Data-In, Address, or Strobe to Output	–	10	10	10	–	75	–	mV (peak)
	Square wave input t_r, t_f = 20 ns							
Input Capacitance, C_{IN}	Any Control Input			–	–	5	7.5	pF

● Peak-to-peak voltage symmetrical about $\frac{V_{DD}}{2}$.

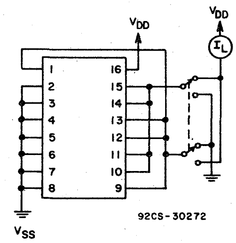


Fig. 14 — OFF switch input or output leakage current test circuit.

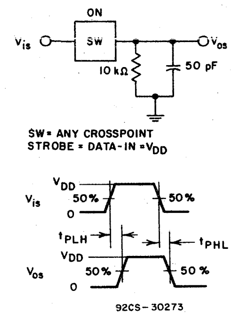


Fig. 15 — Propagation delay time test circuit and waveforms (signal input to signal output, switch ON).

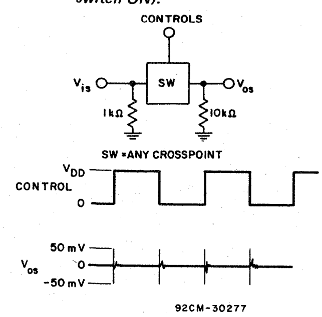


Fig. 16— Test circuit and waveforms for crosstalk (control input to signal output).

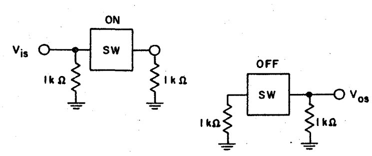


Fig. 17 — Test circuit for crosstalk between switch circuits in the same package.

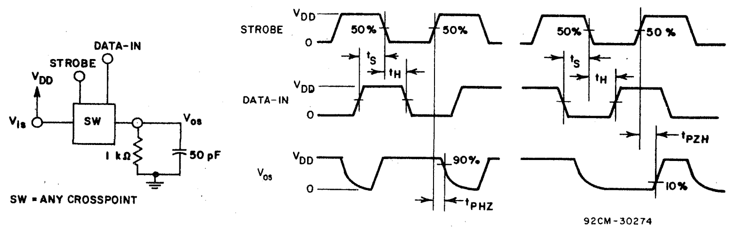


Fig. 18 — Propagation delay time test circuit and waveforms (strobe to signal output, switch Turn-ON or Turn-OFF).

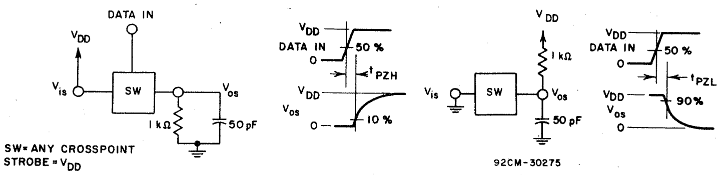


Fig. 19 — Propagation delay time test circuit and waveforms (data-in to signal output, switch Turn-ON to high or low level).

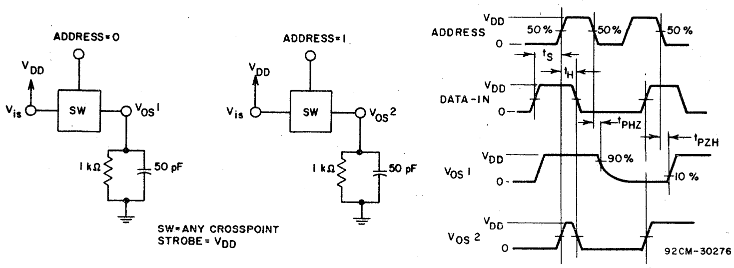
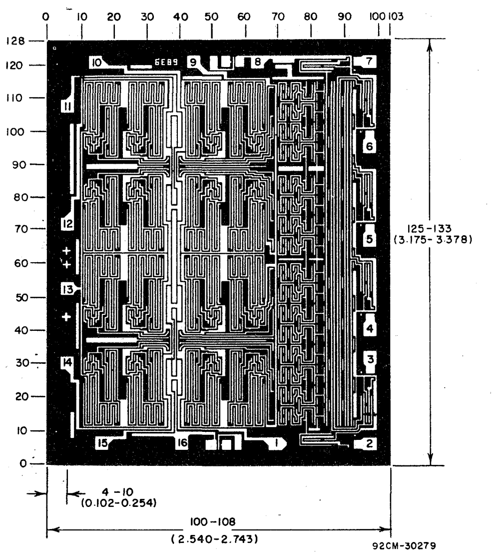


Fig. 20 — Propagation delay time test circuit and waveforms (address to signal output, switch Turn-On or Turn-OFF).



Dimensions and pad layout for CD22100H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

COS/MOS 4 x 4 x 2 Crosspoint Switches With Control Memory

The RCA-CD22101 and CD22102 crosspoint switches consist of 4 x 4 x 2 arrays of crosspoints (transmission gates), 4-line to 16-line decoders, and 16 latch circuits. Any one of the sixteen crosspoint pairs can be selected by applying the appropriate four-line address, and any number of crosspoints can be ON simultaneously. Corresponding crosspoints in each array are turned on and off simultaneously, also.

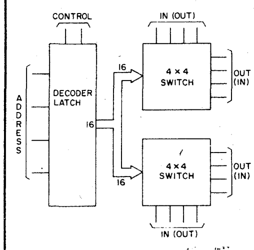
In the CD22101, the selected crosspoint pair can be turned on or off by applying a logical ONE or ZERO, respectively, to the data input, and applying a ONE to the strobe input. When the device is "powered up", the states of the 16 switches are indeterminate. Therefore, all switches must be turned off by putting the strobe high, data-in low, and then addressing all switches in succession.

The selected pair of crosspoints in the CD22102 is turned on by applying a logical ONE to the K_a (set) input while a logical ZERO is on the K_b input, and turned off by applying a logical ONE to the K_b (reset) input while a logical ZERO is on the K_a input. In this respect, the control latches of the CD22102 are similar to SET/RESET flip-flops. They differ, however, in that the simultaneous application of ONEs to the K_a and K_b inputs turns off (resets) all crosspoints. All crosspoints in both devices must be turned off as V_{DD} is applied.

The CD22101 and CD22102 types are supplied in 24-lead hermetic dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

- **Low ON resistance — 75 Ω typ. at V_{DD} = 12 V**
- **"Built-in" latched inputs**
- **Large analog signal capability — ± $V_{DD}/2$**
- **10 MHz switch bandwidth**
- **Matched switch characteristics ΔR_{ON} = 8 Ω typ. at V_{DD} = 12 V**
- **High linearity — 0.25% distortion (typ.) at f = 1 kHz, V_{IN} = 5 V_{p-p}, $V_{DD} - V_{SS}$ = 10 V, and R_l = 1 kΩ**
- **Standard COS/MOS noise immunity**



CD22101, CD22102 Functional Diagram

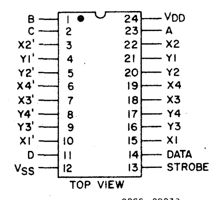
Applications:

- **Telephone systems**
- **PBX**
- **Studio audio switching**
- **Multisystem bus interconnect**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT*	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

* Maximum current through transmission gates (switches) = 25 mA.

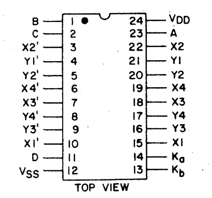


Top View
CD22101 Terminal Diagram

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V



Top View
CD22102 Terminal Diagram

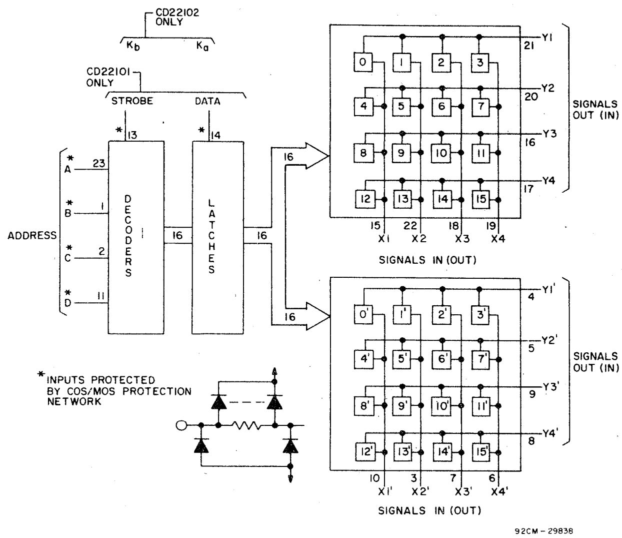


Fig. 1 – Functional block diagram.

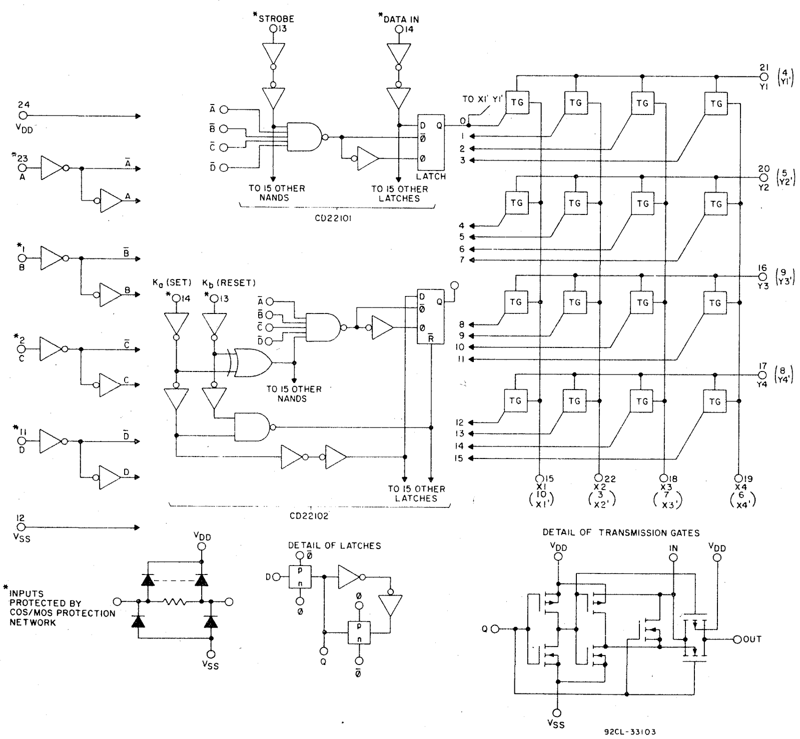


Fig. 2 – Logic diagram.

DECODER TRUTH TABLE

Address A	B	C	D	Select	Address A	B	C	D	Select
0	0	0	0	X1Y1 & X1'Y1'	0	0	0	1	X1Y3 & X1'Y3'
1	0	0	0	X2Y1 & X2'Y1'	1	0	0	1	X2Y3 & X2'Y3'
0	1	0	0	X3Y1 & X3'Y1'	0	1	0	1	X3Y3 & X3'Y3'
1	1	0	0	X4Y1 & X4'Y1'	1	1	0	1	X4Y3 & X4'Y3'
0	0	1	0	X1Y2 & X1'Y2'	0	0	1	1	X1Y4 & X1'Y4'
1	0	1	0	X2Y2 & X2'Y2'	1	0	1	1	X2Y4 & X2'Y4'
0	1	1	0	X3Y2 & X3'Y2'	0	1	1	1	X3Y4 & X3'Y4'
1	1	1	0	X4Y2 & X4'Y2'	1	1	1	1	X4Y4 & X4'Y4'

CONTROL TRUTH TABLE FOR CD22101

Function	Address A	B	C	D	Strobe	Data	Select
Switch On	1	1	1	1	1	1	15 (X4Y4) & 15' (X4'Y4')
Switch Off	1	1	1	1	1	0	15 (X4Y4) & 15' (X4'Y4')
No Change	X	X	X	X	0	X	X X X X

1 = High Level; 0 = Low Level; X = Don't Care

CONTROL TRUTH TABLE FOR CD22102

Function	Address A	B	C	D	K_a	K_b	Select
Switch On	1	1	1	1	1	0	15 (X4Y4) & 15' (X4'Y4')
Switch Off	1	1	1	1	0	1	15 (X4Y4) & 15' (X4'Y4')
All Switches Off	X	X	X	X	1	1	All
No Change	X	X	X	X	0	0	X X X X

1 = High Level; 0 = Low Level; X = Don't Care

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	TYPICAL VALUE	UNITS
Quiescent Device Current, I_L	Switches OFF or ON	12	20	nA
Crosspoint: OFF Leakage Current, I_L	R_L 10 kΩ	12	100	pA
ON Resistance, R_{ON}	R_L 10 kΩ	12	75	Ω
ΔON Resistance, ΔR_{ON}	R_L 10 kΩ	12	5	Ω
Feedthrough Capacitance, C_{IOS}	R_L 10 kΩ	12	0.2	pF
Channel Input or Output Capacitance, C_{IS}, C_{OS}	R_L 10 kΩ	12	30	pF
Control Input Capacitance, C_I	R_L 10 kΩ	12	5	pF
Sine Wave Response (Distortion)	f_{is} = 1 kHz R_L = 10 kΩ	12	0.4	%
Feedthrough, Crosspoints OFF	f_{is} = 1.6 kHz R_L = 1 kΩ	12	−95	dB

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	TYPICAL VALUE	UNITS
Propagation Delay Time: Address or Strobe Inputs To Output, t_{PHL}, t_{PLH}	R_L = 10 kΩ C_L = 50 pF	12	200	ns
Across Crosspoint, t_{PHL}, t_{PLH}	R_L = 10 kΩ C_L = 50 pF	12	20	ns
Minimum Strobe Pulse Width	R_L = 10 kΩ C_L = 50 pF	12	80	ns

COS/MOS Four-Digit LCD Decoder-Drivers

12-V Rating

The RCA-CD22104 types are non-multiplexed, four-digit, seven-segment, liquid-crystal display decoder-drivers.

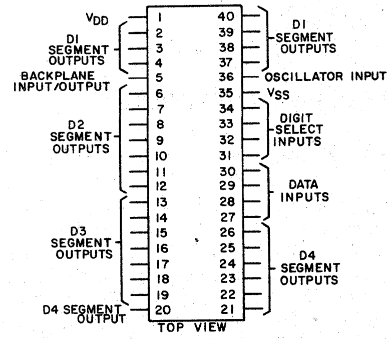
The CD22104 types contain all the circuitry necessary to drive conventional LCD displays (no external components required). Outputs are four sets of seven-segment driver signals and a backplane driver signal. The backplane signal, derived from an on-board free-running oscillator, is common to all four digit displays. These outputs combine to provide the zero dc components necessary for long display life.

There are four data inputs and four digit select inputs. The four-bit binary input is decoded by means of a PROM into seven-segment hexadecimal outputs for the CD22104 and into decimal seven-segment display outputs for the CD22104A. These devices are pin-compatible with the Intersil ICM7211IPL and ICM7211AIPL, respectively.

Features
- *12-V supply-voltage rating*
- *No external components necessary*
- *4-digit segment drive capability*
- *Backplane input/output allows synchronization for cascading devices to drive more digits*
- *Decodes multiplexed binary to hexadecimal (CD22104) and decimal (CD22104A) outputs*

Applications
- *Digital meters and calculators*
- *General-purpose displays*
- *Wall and table clocks*
- *Automobile dashboard displays*
- *Appliance control panels*

The CD22104 types are supplied in the 40-lead dual-in-line plastic (E suffix) package.



CD22104, CD22104A Terminal Assignment

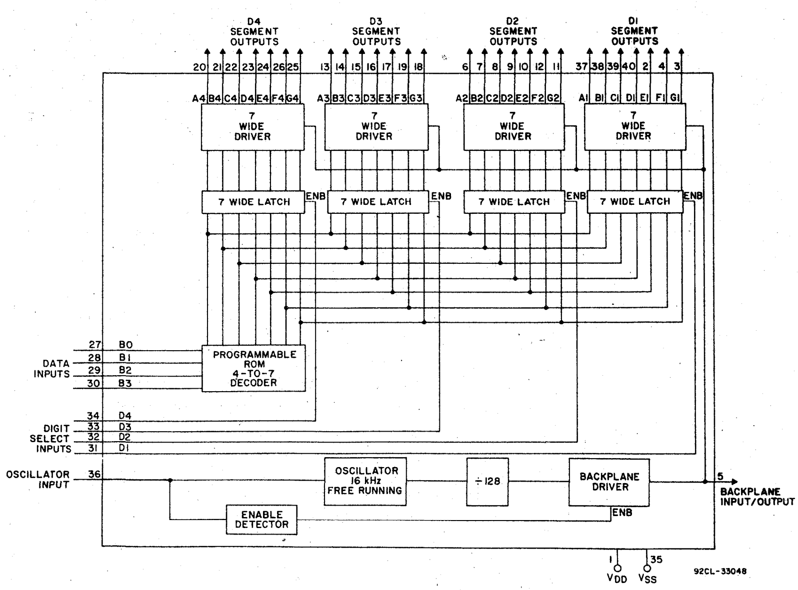


Fig. 1 - Block diagram of CD22104 and CD22104A.

Table I — Output Codes

Binary Input B3 B2 B1 B0	Display Hexadecimal CD22104	Display Decimal CD22104A
0 0 0 0	0	0
0 0 0 1	1	1
0 0 1 0	2	2
0 0 1 1	3	3
0 1 0 0	4	4
0 1 0 1	5	5
0 1 1 0	6	6
0 1 1 1	7	7
1 0 0 0	8	8
1 0 0 1	9	9
1 0 1 0	A	-
1 0 1 1	b	E
1 1 0 0	C	H
1 1 0 1	d	L
1 1 1 0	E	P
1 1 1 1	F	(BLANK)

92CS-33050

CD22105, CD22105A Types

Objective Data

COS/MOS Four-Digit LCD Decoder-Drivers

12-V Rating

The RCA-CD22105 types are non-multiplexed, four-digit, seven-segment, liquid-crystal display decoder-drivers.

The CD22105 types contain all the circuitry necessary to drive conventional liquid-crystal displays (no external components required). Outputs are four sets of seven-segment driver signals and a backplane driver signal. The backplane signal, derived from an on-board free-running oscillator, is common to all four digit displays. These outputs combine to provide the zero dc components necessary for long display life.

A four-bit data-input latch and a two-bit select-code latch under the control of two chip-select inputs permit interfacing with a microprocessor. This device simplifies designing a seven-segment display into a microprocessor system, without requiring extensive ROM or CPU time for decoding and display updating. The four-bit binary input is decoded by means of a PROM into a seven-segment hexadecimal output for the CD22105 type and into a decimal display for the CD22105A type. These types are pin-compatible with the Intersil ICM7211MIPL and ICM7211AMIPL, respectively.

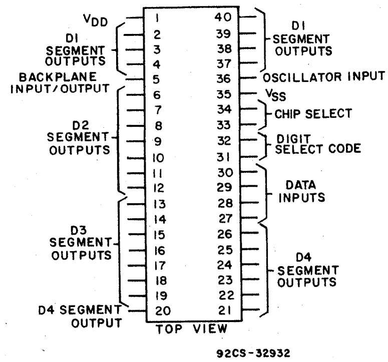
The CD22105 types are supplied in the 40-lead dual-in-line plastic (E suffix) package.

Features

- *12-V supply-voltage rating*
- *No external components necessary*
- *4-digit segment drive capability*
- *Backplane input/output allows synchronization for cascading devices to drive more digits*
- *Direct microprocessor interface*
- *Decodes binary into hexadecimal (CD22105) and decimal (CD22105A) outputs*

Applications

- *Microprocessor-controlled digital meters and calculators*
- *General-purpose displays*
- *Microprocessor-controlled automotive dashboard displays*
- *Microprocessor appliance control panels*



CD22105, CD22105A Terminal Assignment

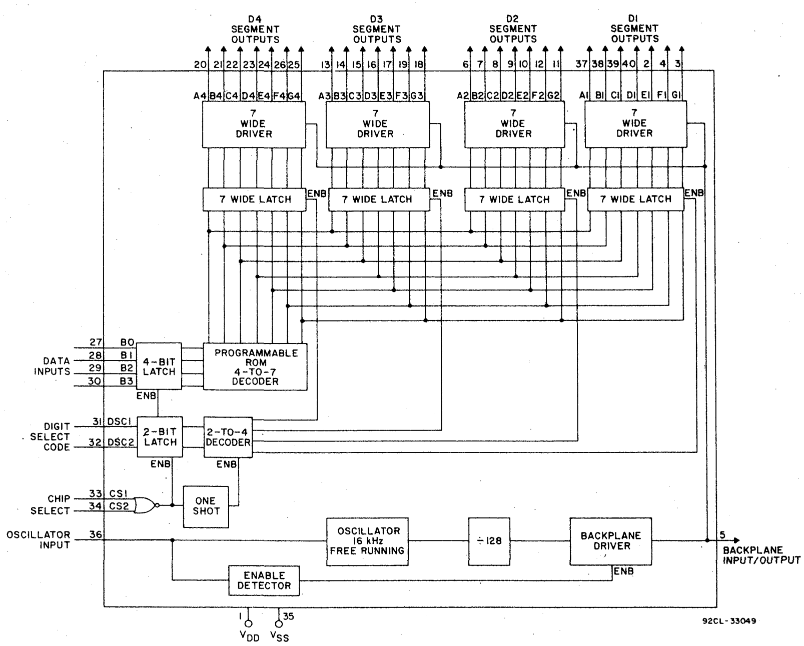


Fig. 1 - Block diagram of CD22105 and CD22105A.

Table I — Output Codes

Binary Input	Display	
B3 B2 B1 B0	Hexadecimal CD22105	Decimal CD22105A
0 0 0 0	0	0
0 0 0 1	1	1
0 0 1 0	2	2
0 0 1 1	3	3
0 1 0 0	4	4
0 1 0 1	5	5
0 1 1 0	6	6
0 1 1 1	7	7
1 0 0 0	8	8
1 0 0 1	9	9
1 0 1 0	A	-
1 0 1 1	b	E
1 1 0 0	C	H
1 1 0 1	d	L
1 1 1 0	E	P
1 1 1 1	F	(BLANK)

92CS-33150

COS/MOS Dual-Tone Multifrequency Tone Generator

For Use in Dual-Tone Telephone Dialing Systems

Features

- *Mute drivers on chip*
- *Device power can either be regulated dc or telephone loop current*
- *Use of an inexpensive 3.579545-MHz TV crystal provides high accuracy and stability for all frequencies*

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE ($V_{DD} - V_{SS}$) .... −0.5 to +12 V
INPUT VOLTAGE RANGE .... −0.5 to V_{DD} + 0.5 V
POWER DISSIPATION, P_D:
At T_A = −40 °C to +60 °C .... 500 mW
At T_A = +60 °C to +85 °C .... Derate Linearly at 12 mW/ °C to 200 mW
POWER DISSIPATION PER OUTPUT .... 100 mW
OPERATING TEMPERATURE RANGE .... −40 °C to +85 °C
LEAD TEMPERATURE DURING SOLDERING:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm)
from case for 10 s max. .... +265 °C

General Description

The RCA-CD22859 is a CMOS dual-tone multifrequency (DTMF) tone generator for use in dual-tone telephone dialing systems. The device can easily be interfaced to a standard pushbutton telephone keyboard, to provide enabling operation directly with the telephone lines.

The CD22859 generates standard DTMF sinusoidal dialing tones from an on-chip reference crystal oscillator. The reference oscillator uses an inexpensive 3.579545-MHz color TV crystal to create highly stable and accurate tones. The sinusoidal tones are digitally synthesized by a stair-step approximation.

One of four low-frequency band row tones and one of four high-frequency band column tones are selected by driving one of the four row inputs and one of the four column inputs low. Simultaneous selection of more than one row input and/or more than one column input will inhibit tone generation, or generate a single-tone sinusoid. These operating modes are described in the functional truth table.

Control logic is included to allow easy interface to standard K500-type telephones. Two CMOS outputs Tx, Rx, capable of driving external p-n-p receiver and transmitter muting transistors are provided. A low input to the CD pin, inhibits tone generation, turns off the reference oscillator, and causes Tx and Rx outputs to logic '0'. During tone generation mode, $\overline{CD}$ = 1 and Tx, Rx = logic 1.

All row, column, and $\overline{CD}$ inputs are provided with pull-up resistors to allow the use of SPST switch matrixes.

The CD22859 types are supplied in a 16-lead hermetic dual-in-line side-brazed ceramic package (D suffix), and a 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).

DTMF Generator Functional Truth Table

	Inputs				Outputs		
Keyboard Mode	**Number of Column Inputs Activated "Low"**	**Number of Row Inputs Activated Low**	**$\overline{CD}$**	**Tone**	**OSC Running**	**RX**	**TX**
X	X	X	"0"	None	No	"0"	"0"
No key depressed	0	0	"1"	None	No	"0"	"0"
	0	1	"1"	Dual Tone R_a, C_1	Yes	"1"	"1"
	1,2,3, or 4	0	"1"	None	No	"0"	"0"
Normal Dialing One Key Depressed (See Note 1)	1	1	"1"	Dual Tone R_a, C_b	Yes	"1"	"1"
Two or More Keys In Same Row (See Note 2)	2,3, or 4	1	"1"	Single Row Tone R_a	Yes	"1"	"1"
Two or More Keys In Same Column	1	2,3, or 4	"1"	Single Column Tone C_b	Yes	"1"	"1"
Two or More Keys In Different Rows & Columns	2,3 or 4	1	"1"	None	Yes	"1"	"1"
	1		1	None	Yes	"1"	"1"

Where:
X = Do Not Care
R_a, C_b refers to Tone Output frequencies corresponding to Row 1, Row 2, Row 3, Row 4, Column 1, Column 2, Column 3, Column 4
a = 1,2,3,4 b = 1,2,3,4 a = b, or a ≠ b

1. Corresponds to normal dual-tone operation.
2. Corresponds to single-tone generation mode.

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -25\,°C$ to $+60\,°C$

CHARACTERISTIC	V_{DD} (V)	V_O (V)	LIMITS Min.	LIMITS Max.	UNITS
Tone Outputs ($R_L = 82$)					
V_O; Dual-Tone Output	3.7-9.3		350	700	mV rms
$V_O(C_L)$; Single-Tone Output, Column*	3.7-9.3		300	—	mV rms
$V_O(R_L)$; Single-Tone Output, Row**	3.7-9.3		260	—	mV rms
Distortion (Note 1)	3.9-9.3		—	10	%
Rise and Fall Time (Dual-Tone Out) (Note 2)	3.9-9.3		—	5	ms
Pre-Emphasis (Note 3)	3.9-9.3		1	3	dB
Output Frequency (Note 4)	3.9-9.3		(Nom. − 1%)	(Nom. + 1%)	Hz
Mute Output Current					
Transmitter					
I_{OH} (Source)	1.7 10	1.2 9.5	−0.5 −3.4	— —	mA
I_{OL} (Sink)	10	2.5	—	10	μA
Receiver					
I_{OH} (Source)	1.7 10	1.2 9.5	−0.5 −3.4	— —	mA
I_{OL} (Sink)	10	2.5	—	10	μA

*Two or more row inputs low, and one column input low.
**Two or more column inputs low, and one row input low.

Notes:

1. Distortion is defined as: The ratio of all extraneous frequency components generated in the voiceband 0.5 kHz to 3 kHz, to the power of the dual-tone signal, measure across R_L.

$$= \frac{(V_1{}^2 + V_2{}^2 = \ldots + V_n{}^2)}{V_L{}^2 + V_H{}^2}$$

where $V_1, V_2, \ldots V_n$ are extraneous frequency components in the voiceband 0.5 kHz to 3 kHz, V_L is the low-band frequency tone, and V_H is the high-band frequency tone.
2. Tone rise time is defined as the time for each of the 2 DTMF frequencies to attain 90% of full amplitude, measured from the time when a row and column signal are driven low.
3. Pre-emphasis is the ratio of the high-group level to the low-group level.
4. Refer to Fig. 1 for standard DTMF frequencies.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -25\,°C$ to $+60\,°C$
All voltages referenced to $V_{SS} = 0$ V.

CHARACTERISTIC	V_{DD}	LIMITS Min.	LIMITS Max.	UNITS
DC Supply Voltage				
Tone Generation Mode with Valid Input*		2.5	10	V
Non-Tone Generation**		1.7	10	V
Operating Current				
Tone Generation Mode (Outputs Unloaded)	3.7 V 9.3 V		1.7 13	mA
No Keydown Mode	3.7 V 9.3 V		100 200	μA
Input Pull-Up Current	3-10 V		400	μA
Input Low Voltage (V_{IL}) Max.	3-10 V		0.2 V_{DD}	V
Input High Voltage (V_{IH}) Min.	3-10 V	0.8 V_{DD}		V

*All logic and counters functional.
**Mute switches remain open.

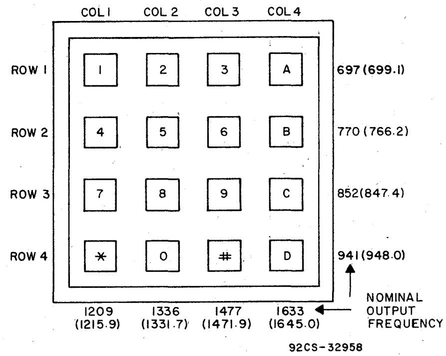
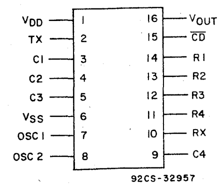


Fig. 1 - Bell and nominal output frequencies (in parenthesis) for 3.579545-MHz crystal.



Terminal Assignment

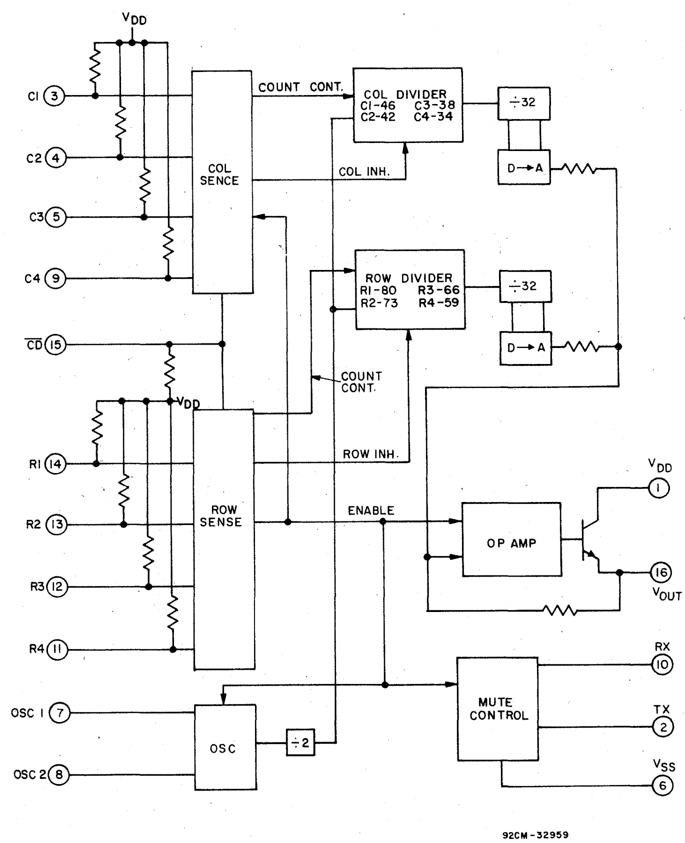


Fig. 2 - Touch-tone generator.

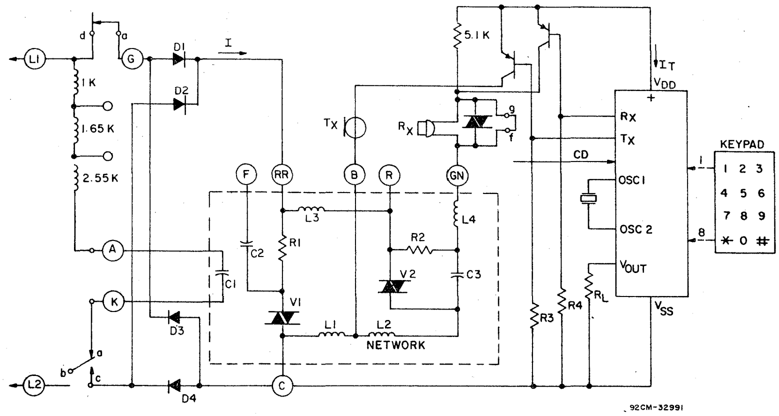
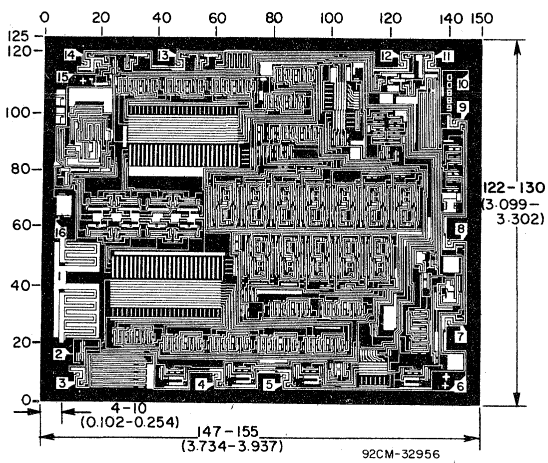


Fig. 3 - Interface with standard K500 telephone network.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for CD22859H chip.

COS/MOS High-Speed 8-Bit Bidirectional CMOS/TTL Interface Level Converter

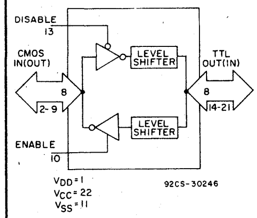
The RCA-CD40115 is a high-speed 8-bit integrated circuit designed to interface CMOS logic levels with TTL logic levels on the data bus of microprocessor-based systems. CMOS/TTL interface is provided by eight parallel bidirectional buffer/level converters. Buffer INPUT/OUTPUT terminals are either inputs or outputs depending on the desired direction of data flow. A low on both the ENABLE and DISABLE control inputs selects the direction of data flow from CMOS Inputs to TTL Outputs. A high on both control inputs selects the direction of data flow from TTL Inputs to CMOS Outputs. A low on the ENABLE and a high on the DISABLE inhibits data flow in either direction and places the CMOS Outputs in a high-impedance (3-state) mode.

The TTL Input/Output terminals and the ENABLE and DISABLE control inputs are TTL-compatible without the use of external pull-up resistors. The TTL input logic 0 to logic 1 transition occurs at a level of approximately 1.5 volts. The ENABLE and DISABLE inputs may be driven to the V_{DD} rail; therefore, either TTL or CMOS logic drivers, capable of sinking one TTL load, may be used to determine the direction of data flow. The large CMOS and TTL output buffers in this device have high output sink and source current capability and can drive the data bus capacitance with a transition time of approximately 0.1 ns/pF. This fast output transition time, together with the small propagation delay time of the device, allow high-speed operation.

The CD40115 is supplied in a 22-lead hermetic dual-in-line ceramic package.

Features:

- **Eight inverting channels with 5V-to-12V or 12V-to-5V level conversion**
- **Three operating modes:**
  - **CMOS-to-TTL level conversion**
  - **TTL-to-CMOS level conversion**
  - **Interface off; high-impedance CMOS input/output**
- **Low propagation delay time:**
  - **CMOS-to-TTL conversion — 10 ns typ.**
  - **TTL-to-CMOS conversion — 30 ns typ.**
- **High TTL sink current — 30 mA typ.**
- **No external TTL input pull-up resistors required**
- **High speed drive of large data bus capacitances**
- **Input/output and power supply terminals located for ease of PC board layout**



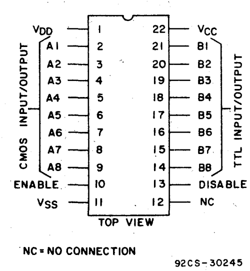
Functional Diagram

Applications:

- **Interface CMOS microprocessor with TTL memories and peripheral devices**
- **Interface between and within logic systems which combine CMOS and TTL devices**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE (Voltages referenced to VSS Terminal)	
V_{DD}	–0.5 to +12.6 V
V_{CC}	–0.5 to +6 V
INPUT VOLTAGE RANGE:	
Data Inputs, CMOS to TTL	–0.5 to V_{DD}+0.5 V
Data Inputs, TTL to CMOS	–0.5 to V_{CC}+0.5 V
Enable, Disable Inputs	–0.5 to V_{DD}+0.5 V
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = –55°C to +100°C	500 mW
For T_A = +100 to +125°C	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = Full Package-Temperature Range	100 mW
OPERATING TEMPERATURE RANGE (T_A)	–55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg})	–65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance of 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C



TERMINAL ASSIGNMENT

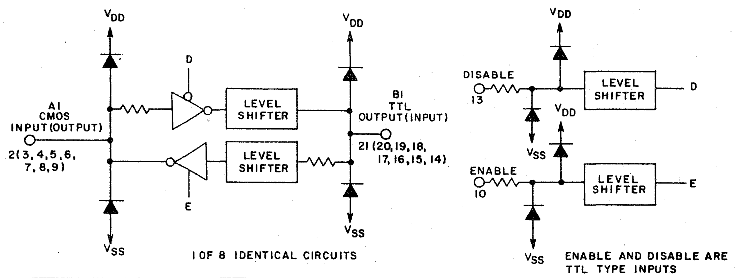
TRUTH TABLE

ENABLE	DISABLE	FUNCTION
0	0	Convert CMOS Level to TTL Level
1	1	Convert TTL Level to CMOS Level
0	1	High Impedance (Z)
1	0	Invalid*

0 = Low Level 1 = High Level
Z = High Impedance on CMOS Output side; TTL side are inputs.
INVALID = Both CMOS and TTL sides are ON as outputs.

See Operating and Handling Considerations — Bypassing and Unused Inputs.

* Excessively high currents from V_{DD} to V_{SS} could flow in this mode during power turn-on or turn-off if other IC's drive into the bus lines (on either the TTL or CMOS side). This high current condition could occur during a transient or steady-state invalid mode.



Input (Output)		Output (Input)	
Data	Terminal No.	Data	Terminal No.
A1	2	B1	21
A2	3	B2	20
A3	4	B3	19
A4	5	B4	18
A5	6	B5	17
A6	7	B6	16
A7	8	B7	15
A8	9	B8	14

Fig. 1 — Functional block diagram.

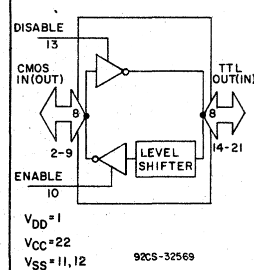
STATIC ELECTRICAL CHARACTERISTICS At $T_A = 25^oC$, $V_{DD} = 12$ V, $V_{CC} = 5$ V

CHARACTERISTIC		TEST CONDITIONS	TYPICAL VALUES	UNITS
Data Flow — CMOS Inputs to TTL Outputs				
Quiescent Device Current, From V_{DD} Supply, From V_{CC} Supply,	I_{DD} I_{CC}		4 5	mA µA
Input Current,	I_{IN}	V_{IN}=0,12 V; Any CMOS input	±50	µA
Output Current,	I_{OH} I_{OL}	V_{OH}=3 V, V_{IL}=2 V V_{OL}=0.4 V, V_{IH}=10 V	15 30	mA
Data Flow — TTL Inputs to CMOS Outputs				
Quiescent Device Current, From V_{DD} Supply, From V_{CC} Supply,	I_{DD} I_{CC}		4 5	mA µA
Input Current,	I_{IL} I_{IH}	V_{IL}=0 to 0.7 V; Any TTL input V_{IH}=2.3 V; Any TTL input	–250 –50	µA
Output Current,	I_{OH} I_{OL}	V_{OH}=11.5 V, V_{IL}=0.7 V V_{OL}=0.5 V, V_{IH}=2.3 V	20 20	mA
CMOS 3-State Output Leakage Current,	I_{OUT}	V_O=0,12 V, V_{IN}=0,5 V	±50	µA
Enable and Disable Inputs				
Input Current,	I_{IL} I_{IH} I_{IH}	V_{IL}=0 to 0.7 V V_{IH}=2.3 V (TTL) V_{IH}=12 V (CMOS)	–250 –50 50	µA

DYNAMIC ELECTRICAL CHARACTERISTICS At $T_A = 25^oC$, $V_{DD} = 12$ V, $V_{CC} = 5$ V

CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES		UNITS
	INPUT	OUTPUT	C_L=50 pF	C_L=200 pF	
Propagation Delay Times, Data-In to Data-Out, t_{PHL}, t_{PLH}	CMOS TTL	TTL CMOS	10 30	15 40	ns
Enable or Disable to Data-Out, t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL}			35		ns
Transition Time, t_{THL}, t_{TLH}	CMOS TTL	TTL CMOS	10 10	15 15	ns

COS/MOS High-Speed 8-Bit Bidirectional CMOS/TTL Interface Level Converter



Functional Diagram

The RCA-CD40116 is a high-speed 8-bit integrated circuit designed to interface CMOS logic levels with TTL logic levels on the data bus of microprocessor-based systems. CMOS/TTL interface is provided by eight parallel bidirectional buffer/level converters. Buffer INPUT/OUTPUT terminals are either inputs or outputs depending on the desired direction of data flow.

A low level on the DISABLE input with the ENABLE input either high or low, permits conversion of CMOS inputs to TTL outputs. A high level on both the DISABLE and ENABLE inputs permits data flow from TTL inputs to CMOS outputs. A low level on the ENABLE input and a high level on the DISABLE input sets both inputs/outputs to the high-impedance state.

The TTL Input/Output terminals and the ENABLE and DISABLE control inputs are TTL-compatible without the use of external pull-up resistors. The TTL input logic 0 to logic 1 transition occurs at a level of approximately 1.5 volts. The ENABLE and DISABLE inputs may be driven to the V_{DD} rail; therefore, either TTL or CMOS logic drivers, capable of sinking one TTL load, may be used to determine the direction of data flow. The large CMOS and TTL output buffers in this device have high output sink and source current capability and can drive the data bus capacitance with a transition time of approximately 0.25 ns/pF. This fast output transition time, together with the small propagation delay time of the device, allow high-speed operation.

The CD40116 is supplied in a 22-lead hermetic dual-in-line ceramic package, (D suffix) and in a 22-lead plastic package (E suffix).

Features:

- **Eight inverting channels with conversion from V_{DD} to V_{CC} or V_{CC} to V_{DD} ($4\ V \leq V_{DD} \leq 12\ V$ and $4\ V \leq V_{CC} \leq V_{DD}$)**
- **Three operating modes:**
  CMOS-to-TTL level conversion
  TTL-to-CMOS level conversion
  Interface off; high-impedance on both sides
- **Low propagation delay time:**
  CMOS-to-TTL conversion — 15 ns typ.
  TTL-to-CMOS conversion — 30 ns typ.
  (V_{DD} = 12 V, V_{CC} = 5 V)
- **High TTL sink current — 11 mA typ.**
- **No external TTL input pull-up resistors required**
- **High speed drive of large data bus capacitances**
- **Input/output and power supply terminals located for ease of PC board layout**

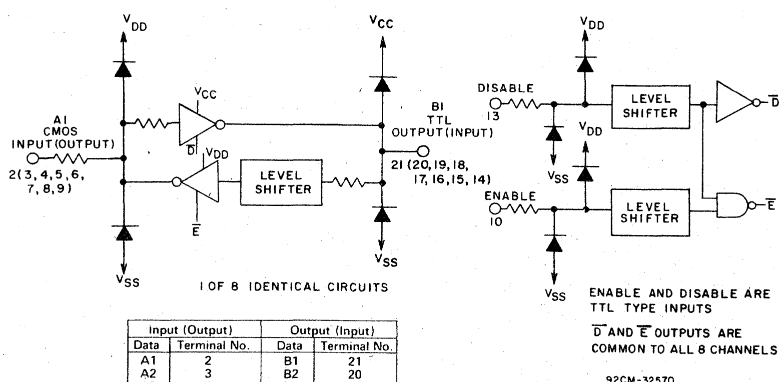
Applications:

- **Interface CMOS microprocessor with TTL memories and peripheral devices**
- **Interface between and within logic systems which combine CMOS and TTL devices**

TRUTH TABLE

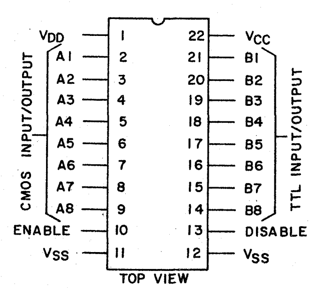
ENABLE	DISABLE	FUNCTION
X	0	Convert CMOS Level to TTL Level
1	1	Convert TTL Level to CMOS Level
0	1	High Impedance (Z)

0 = Low Level 1 = High Level X = Don't Care
Z = High Impedance on both CMOS and TTL sides.
See Operating and Handling Considerations — Bypassing and Unused Inputs.



Input (Output)		Output (Input)	
Data	Terminal No.	Data	Terminal No.
A1	2	B1	21
A2	3	B2	20
A3	4	B3	19
A4	5	B4	18
A5	6	B5	17
A6	7	B6	16
A7	8	B7	15
A8	9	B8	14

Fig. 1—Functional block diagram.



92CS-30245

TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE (Voltage referenced to VSS Terminal)
- V_{DD} .... —0.5 to V_{DD}
- V_{CC} .... —0.5 to V_{DD}

INPUT VOLTAGE RANGE:
- Data Inputs, CMOS to TTL .... —0.5 to V_{DD} +0.5 V
- Data Inputs, TTL to CMOS .... —0.5 to V_{CC} +0.5 V
- Enable, Disable Inputs .... —0.5 to V_{DD} +0.5 V

POWER DISSIPATION PER PACKAGE (P_D):
- For T_A = —40 to +60°C (Package Type E) .... 500 mW
- For T_A = 60 to +85°C (Package Type E) .... Derate linearly at 12 mW/°C to 200 mW
- For T_A = —55°C to + 100°C .... 500 mW
- For T_A = +100 to +125°C .... Derate linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR
- For T_A= Full Package-Temperature Range .... 100 mW

OPERATING TEMPERATURE RANGE (T_A):
- Package Type D .... —55 to +125°C
- Package Type E .... —40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) .... —65 to +150°C

LEAD TEMPERATURE (During Soldering):
- At distance of 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max .... +265°C

STATIC CHARACTERISTICS at T_A = 25°C, V_{DD} = 12 V, V_{CC} = 5 V

CHARACTERISTIC		TEST CONDITIONS	TYPICAL VALUES	UNITS
Quiescent Device Current,		ENABLE = 1	1	mA
From V_{DD} Supply,	I_{DD}	ENABLE = 0	200	μA
From V_{CC} Supply,	I_{CC}		5	μA
Data Flow — CMOS Inputs to TTL Outputs				
Input Current,	I_{IN}	V_{IN} = 0,12 V; Any CMOS input	±5	μA
Output Current,	I_{OH}	V_{OH} = 3 V, V_{IL} = 2 V	−12	mA
	I_{OL}	V_{OL} = 0.4 V, V_{IH} = 10 V	11	mA
TTL 3-State Output Leakage		ENABLE = 1	—250	
Current	I_{OUT}	ENABLE = 0	±5	μA
Data Flow — TTL Inputs to CMOS Outputs				
Input Current,	I_{IL}	V_{IL} = 0 to 0.7 V; Any TTL input	—250	μA
	I_{IH}	V_{IH} = 2.3 V; Any TTL input	—150	μA
Output Current,	I_{OH}	V_{OH} = 11.5 V, V_{IL} = 0.7 V	− 6.5	mA
	I_{OL}	V_{OL} = 0.5 V, V_{IH} = 2.3 V	6.5	mA
CMOS 3-State Output Leakage Current,	I_{OUT}	V_O = 0,12 V, V_{IN} = 0,5 V	±5	μA
Enable and Disable Inputs				
	I_{IL}	V_{IL} = 0 to 0.7 V	—250	
Input Current,	I_{IH}	V_{IH} = 2.3 V (TTL)	—150	μA
	I_{IH}	V_{IH} = 12 V (CMOS)	5	

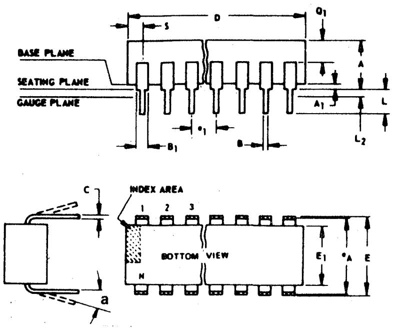
DYNAMIC ELECTRICAL CHARACTERISTICS At T_A = 25°C, V_{DD} = 12 V, V_{CC} = 5 V

CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES		UNITS
	INPUT	OUTPUT	C_L = 50 pF	C_L = 200 pF	
Propagation Delay Times, Data-In to Data-Out, t_{PHL}, t_{PLH}	CMOS	TTL	15	35	ns
	TTL	CMOS	30	50	ns
Enable or Disable to Data-Out, t_{PHZ},t_{PZH},t_{PLZ},t_{PZL}			30		ns
Transition Time, t_{THL}, t_{TLH}	CMOS	TTL	20	55	ns
	TTL	CMOS	20	55	ns

Dimensional Outlines

Dimensional Outlines

Dual-In-Line Welded-Seal Ceramic Packages



NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(D) SUFFIX (JEDEC MO-001-AD)
14-Lead Dual-In-Line Welded-Seal Ceramic Package

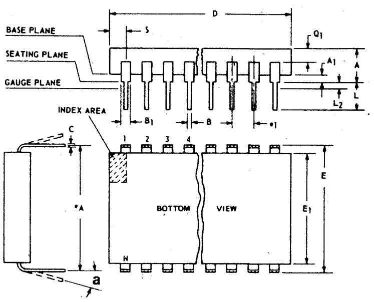
SYMBOL	INCHES MIN.	INCHES MAX.	NOTE	MILLIMETERS MIN.	MILLIMETERS MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
a	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.065	0.090		1.66	2.28

92SS-4411R2

(D) SUFFIX (JEDEC MO-001-AE)
16-Lead Dual-In-Line Welded-Seal Ceramic Package

SYMBOL	INCHES MIN.	INCHES MAX.	NOTE	MILLIMETERS MIN.	MILLIMETERS MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
a	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.015	0.060		0.39	1.52

92SS-4286R5



NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(D) SUFFIX (JEDEC MO-015-AG)
24-Lead Dual-In-Line Welded-Seal Ceramic Package

SYMBOL	INCHES MIN.	INCHES MAX.	NOTE	MILLIMETERS MIN.	MILLIMETERS MAX.
A	0.090	0.200		2.29	5.08
A_1	0.020	0.070		0.51	1.78
B	0.015	0.020		0.381	0.508
B_1	0.045	0.055		1.143	1.397
C	0.008	0.012	1	0.204	0.304
D	1.15	1.22		29.21	30.98
E	0.600	0.625		15.24	15.87
E_1	0.480	0.520		12.20	13.20
e_1	0.100 TP		2	2.54 TP	
e_A	0.600 TP		2,3	15.24 TP	
L	0.100	0.180		2.54	4.57
L_2	0.000	0.030		0.00	0.76
a	0°	15°	4	0°	15°
N	24		5	24	
N_1	0		6	0	
Q_1	0.020	0.080		0.51	2.03
S	0.020	0.060		0.51	1.52

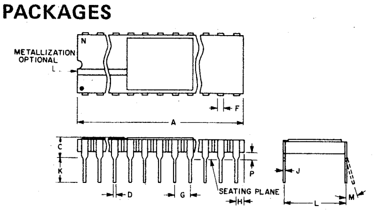
92CS-19948R4

(D) SUFFIX (JEDEC MO-015-AH)
28-Lead Dual-In-Line Welded-Seal Ceramic Package

SYMBOL	INCHES MIN.	INCHES MAX.	NOTE	MILLIMETERS MIN.	MILLIMETERS MAX.
A	0.090	0.200		2.29	5
A_1	0	0.070	2	0	1.77
B	0.015	0.020		0.381	0.508
B_1	0.015	0.055		0.39	1.39
C	0.008	0.012	1	0.204	0.304
D	1.380	1.420		35.06	36.06
E	0.600	0.625		15.24	15.87
E_1	0.485	0.515		12.32	13.08
e_1	0.100 TP		2	2.54 TP	
e_A	0.600 TP		2,3	15.24 TP	
L	0.100	0.200		2.6	5
L_2	0	0.030		0	0.76
a	0°	15°	4	0°	15°
N	28		5	28	
N_1	0		6	0	
Q_1	0.020	0.070		0.51	1.77
S	0.040	0.070		1.02	1.77

92CM-20250R2

DUAL-IN-LINE SIDE-BRAZED CERAMIC PACKAGES



NOTES:
1. Leads within 0.005" (0.13 mm) radius of True Position at maximum material condition.
2. Center to center of leads when formed parallel.
3. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).

(D) SUFFIX
40-Lead Dual-In-Line Side-Brazed Ceramic Package

SYMBOL	INCHES MIN.	INCHES MAX.	NOTE	MILLIMETERS MIN.	MILLIMETERS MAX.
A	1.980	2.020		50.30	51.30
C	0.095	0.155		2.43	3.93
D	0.017	0.023		0.43	0.56
F	0.050 REF.			1.27 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.030	0.070		0.76	1.78
J	0.008	0.012	3	0.20	0.30
K	0.125	0.175		3.18	4.45
L	0.580	0.620	2	14.74	15.74
M	–	7°		–	7°
P	0.025	0.050		0.64	1.27
N	40			40	

92CM-27029R2

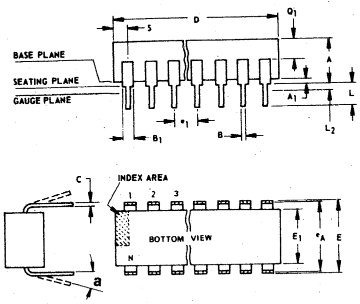
(D) SUFFIX
22-Lead Dual-In-Line Side-Brazed Ceramic Package

SYMBOL	INCHES MIN.	INCHES MAX.	NOTE	MILLIMETERS MIN.	MILLIMETERS MAX.
A	1.065	1.100		27.05	27.94
C	0.085	0.145		2.16	3.68
D	0.017	0.023		0.43	0.56
F	0.040 REF.		1	1.02 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.030	0.070		0.76	1.78
J	0.008	0.012	3	0.20	0.30
K	0.125	0.175		3.18	4.45
L	0.380	0.420	2	9.65	10.67
M	–	7°		–	7°
P	0.025	0.050		0.64	1.27
N	22			22	

92CS-25186R2

Dimensional Outlines (Cont'd)

Dual-In-Line Plastic and Frit-Seal Ceramic Packages



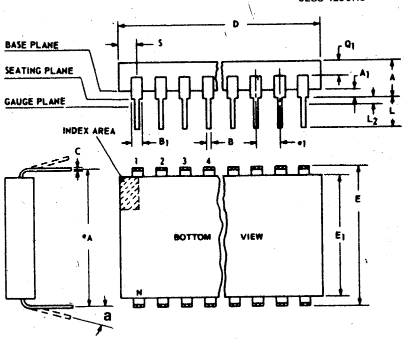
NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(E) and (F) SUFFIXES (JEDEC MO-001-AB)
14-Lead Dual-In-Line Plastic or Frit-Seal Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
a	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.065	0.090		1.66	2.28

92SS-4296R3



NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at guage plane with maximum material condition and unit installed
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(E) and (F) SUFFIXES (JEDEC MO-001-AC)
16-Lead Dual-In-Line Plastic or Frit-Seal Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
a	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

92CM-15967R4

(E) SUFFIX
22-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.015	0.020		0.381	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D		1.120			28.44
E	0.390	0.420		9.91	10.66
E_1	0.345	0.355		8.77	9.01
e_1	0.100 TP		2	2.54 TP	
e_A	0.400 TP		2, 3	10.16 TP	
L	0.125	0.150		3.18	3.81
L_2	0	0.030		0	0.762
a	2°	15°	4	2°	15°
N	22		5	22	
N_1	0		6	0	
Q_1	0.055	0.085		1.40	2.15
S	0.015	0.060		0.381	1.27

92CS-30830

(E) and (F) SUFFIXES (JEDEC MO-015-AA)
24-Lead Dual-In-Line Plastic or Frit-Seal Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.250		3.10	6.30
A_1	0.020	0.070		0.51	1.77
B	0.016	0.020		0.407	0.508
B_1	0.028	0.070		0.72	1.77
C	0.008	0.012	1	0.204	0.304
D	1.20	1.29		30.48	32.76
E	0.600	0.625		15.24	15.87
E_1	0.515	0.580		13.09	14.73
e_1	0.100 TP		2	2.54 TP	
e_A	0.600 TP		2,3	15.24 TP	
L	0.100	0.200		2.54	5.00
L_2	0.000	0.030		0.00	0.76
a	0°	15°	4	0°	15°
N	24		5	24	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.040	0.100		1.02	2.54

92CS26938R2

(E) SUFFIX (JEDEC MO-001-AN)
8-Lead Dual-In-Line Plastic (Mini-DIP) Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.889	1.65
C	0.008	0.012	1	0.203	0.304
D	0.370	0.400		9.40	10.16
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.762
a	0°	15°	4	0°	15°
N	8		5	8	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.381	1.52

92CS-24026RI

(F) SUFFIX (JEDEC MO-001-AG)
16-Lead Dual-In-Line Frit-Seal Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.165	0.210		4.20	5.33
A_1	0.015	0.045		0.381	1.14
B	0.015	0.020		0.381	0.508
B_1	0.045	0.070		1.15	1.77
C	0.009	0.011	1	0.229	0.279
D	0.750	0.795		19.05	20.19
E	0.295	0.325		7.50	8.25
E_1	0.245	0.300		6.23	7.62
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.120	0.160		3.05	4.06
L_2	0.000	0.030		0.000	0.76
a	2°	15°	4	2°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.050	0.080		1.27	2.03
S	0.010	0.060		0.254	1.52

92CM-22284R1

(E) SUFFIX
40-Lead Dual-In-Line Plastic Package

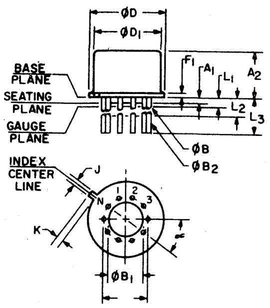
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.250		3.10	6.30
A_1	0.020	0.070		0.51	1.77
B	0.016	0.020		0.407	0.508
B_1	0.028	0.070		0.72	1.77
C	0.008	0.012	1	0.204	0.304
D	2.000	2.090		50.80	53.09
E_1	0.515	0.580		13.09	14.73
e_1	0.100 TP		2	2.54 TP	
e_A	0.600 TP		2,3	15.24 TP	
L	0.100	0.200		2.54	5.00
L_2	0.000	0.030		0.00	0.76
a	0°	15°	4	0°	15°
N	40		5	40	
N_1	0		6	0	
Q_1	0.065	0.095		1.66	2.41
S	0.040	0.100		1.02	2.54

92CS-30959

Dimensional Outlines (Cont'd)

TO-5 Style Package

(T) SUFFIX (JEDEC MO-006-AG)
12-Lead Metal Package



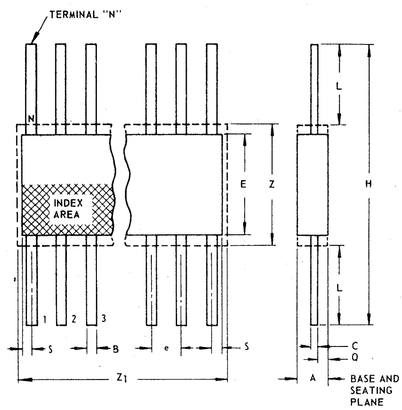
92CS-19774

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.230		2	5.84 TP	
A_1	0	0		0	0
A_2	0.165	0.185		4.19	4.70
φB	0.016	0.019	3	0.407	0.482
$φB_1$	0	0		0	0
$φB_2$	0.016	0.021	3	0.407	0.533
φD	0.335	0.370		8.51	9.39
$φD_1$	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
a	30° TP			30° TP	
N	12		6	12	
N_1	1		5	1	

NOTES:
1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
3. φB applies between L_1 and L_2. $φB_2$ applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. φD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

Ceramic Flat Packs

(K) SUFFIX (JEDEC MO-004-AF)
14-Lead



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	14		3	14	
Q	0.005	0.050		0.13	1.27
S	0.000	0.050		0.00	1.27
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

92SS-4300R3

NOTES:
1. Refer to JEDEC Publication No. 95 for Rules for Dimensioning Peripheral Lead Outlines.
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.

(K) SUFFIX (JEDEC MO-004-AG)
16-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	16		3	16	
Q	0.005	0.050		0.13	1.27
S	0.000	0.025		0.00	0.63
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

92CS-17271R3

(K) SUFFIX
24-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.075	0.120		1.91	3.04
B	0.018	0.022	1	0.458	0.558
C	0.004	0.007	1	0.102	0.177
e	0.050 TP		2	1.27 TP	
E	0.600	0.700		15.24	17.78
H	1.150	1.350		29.21	34.29
L	0.225	0.325		5.72	8.25
N	24		3	24	
Q	0.035	0.070		0.89	1.77
S	0.060	0.110	1	1.53	2.79
Z	0.700		4	17.78	
Z_1	0.750		4	19.05	

92CS-19949R2

(K) SUFFIX
28-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.075	0.120		1.91	3.04
B	0.018	0.022	1	0.458	0.558
C	0.004	0.007	1	0.102	0.177
e	0.050 TP		2	1.27 TP	
E	0.600	0.700		15.24	17.78
H	1.150	1.350		29.21	34.29
L	0.225	0.325		5.72	8.25
N	28		3	28	
Q	0.035	0.070		0.89	1.77
S	0	0.060	1	0	1.53
Z	0.700		4	17.78	
Z_1	0.750		4	19.05	

92CS-20972

Application Notes

Timekeeping Advances Through COS/MOS Technology

by S.S. Eaton

Most COS/MOS timing circuits consist of three basic parts: an oscillator, or main timing standard; some digital processing logic, usually in the form of frequency-dividing circuits; and logic-circuit drivers for mechanical or electrical output devices controlled by the digital processing logic. The oscillator is perhaps the most important because the accuracy of the total COS/MOS timing system is entirely dependent upon the accuracy of the oscillator. This Note discusses basic oscillator design considerations, practical COS/MOS oscillator circuits, and some typical COS/MOS timing-circuit applications.

BASIC OSCILLATOR DESIGN CONSIDERATIONS

A basic oscillator circuit consists of an amplifier and a feedback section, as shown in Fig. 1. For oscillation to occur, the gain of the amplifier times the attenuation of the feedback network must be greater than one. In addition, the total phase shift through the amplifier and feedback network must be equal to n times 360 degrees, where n is an integer. These conditions imply that oscillations occur in any system in which an amplified signal is returned in phase to the amplifier input after being attenuated less than it was originally amplified. In such a system, any noise present at

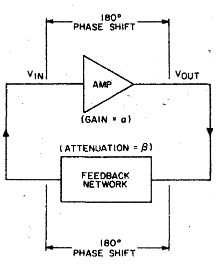


Fig. 1— Basic oscillator circuit.

the amplifier input causes oscillation to build up at a rate determined by the loop gain, or $\alpha\beta$ product, of the over-all circuit.

The frequency stability of an oscillator is primarily dependent upon the phase-changing properties of the feedback network. For high stability, quartz crystals and tuning forks are commonly used as feedback network elements. The quartz crystal is the more popular because of its higher Q or greater inherent frequency stability.

Selection of Crystal Operating Mode

Fig. 2 shows the equivalent circuit of a quartz crystal, and Table I lists typical component values of the elements included in the equivalent circuit for different crystal cuts and operating frequencies. The basic circuit can be resolved into equivalent resistive (R_e) and reactive (X_e) components. Fig. 3 shows curves of these components as functions of frequency for a typical 32.768-kHz crystal. Fig. 3(b) shows two points at which the crystal appears purely resistive, (i.e., points at which X_e = 0). These points are defined as the resonant (f_r) and antiresonant (f_a) frequencies. Series-resonant oscillator circuits are designed to oscillate at or near f_r. Parallel-resonant circuits oscillate between f_r and f_a, depending upon the value of a parallel loading capacitor, as discussed later. In contrast to series-resonant circuits, parallel resonant-circuits work best with amplifiers that have high input impedances. The parallel-resonant circuit, therefore, is most applicable to crystal oscillators that employ COS/MOS amplifiers.[1]

Feedback-Circuit Configuration

A feedback circuit suitable for use with a parallel-resonant oscillator circuit is shown in Fig. 4. This circuit, known as a crystal pi network, is intended for use after an amplifier that provides a 180-degree phase shift. The pi network is designed to provide the additional 180-degree phase shift required for oscillation. The phase angle for this type of feedback circuit is extremely sensitive to a change in frequency, a condition necessary for stable oscillation. If the equivalent resistance of the crystal were in fact zero (infinite

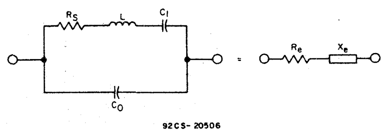


Fig. 2— Equivalent circuit for a quartz crystal.

Table I – Typical Component Values for Common Cuts of Quartz Oscillator Crystals

FREQUENCY	32 kHz	280 kHz	525 kHz	2MHz
Cut	XY Bar	DT	DT	AT
R_s (ohms)	40K	1820	1400	82
L (Hy)	4800	25.9	12.7	0.52
C_1 (pF)	0.00491	0.0125	0.00724	0.0122
C_o (pF)	2.85	5.62	3.44	4.27
C_o/C_1	580	450	475	350
Q	25000	25000	30000	80000

Q), a change in the phase angle of the feedback circuit would not cause any change in oscillator frequency; the frequency, therefore, would be insensitive to any phase change in the amplifier. Though practical crystals allow only a slight change in frequency for large variations in phase angle, the amplifier phase angle should, to the extent possible, be made independent of temperature and supply-voltage variations in order to minimize the phase compensation required of the feedback network. Any required phase compensation will, of course, dictate a corresponding change in the frequency of oscillation consistent with practical values of crystal Q. For this reason, the equivalent resistance of the crystal should be maintained as low as possible, and the amplifier should be designed to roll off at frequencies greater than the crystal frequency.

Oscillator Amplifier

Fig. 5 shows a COS/MOS amplifier circuit that may be used to provide the amplification function in a crystal-controlled oscillator. The amplifier is biased so that the output voltage V_{OUT} is equal to the input voltage V_{IN} or typically is equal to one-half the supply voltage V_{DD}, (i.e., $V_{OUT} = V_{IN} = V_{DD}/2$). Biasing is accomplished by means of a resistor that has a value high enough to prevent loading of the feedback network, yet that is low in comparison to the amplifier input resistance. Resistor values of 10 to 500 megohms will satisfy these criteria; however, lower values in the order of 15 megohms are generally used to allow greater input leakage without any severe change in bias point. The gain of the amplifier varies with supply voltage, the size of the n- and p-channel MOS transistors, and the sum of the threshold voltages of the n- and p-channel transistors. When an oscillator amplifier is designed to roll off at frequencies greater than the crystal frequency, care must be taken to assure that the transistor sizes are large enough for the particular supply voltage used and range of threshold voltages expected. For any circuit, though, the sum of the threshold voltages of the n- and p-channel transistors must always be less than the supply voltage.

The oscillator amplifier governs, to a certain extent, the selection of the components for the feedback network. The amplifier current consumption is strongly dependent upon the attenuation across the feedback network. As the attenuation becomes greater, the signal at the amplifier input becomes smaller, which, in turn, increases the amplifier current consumption. Large voltage swings at the amplifier input cause little current to flow because the resistance of either the n- or p-channel transistor is high during a large portion of the cycle. On the basis of power considerations, it is best to design the feedback network for a small attenuation.

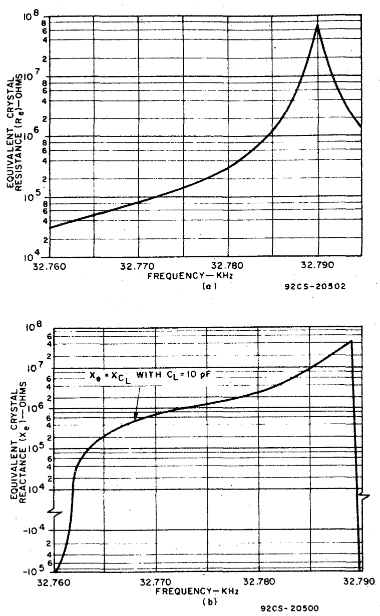


Fig. 3— Impedance characteristics of a quartz oscillator crystal: (a) equivalent crystal resistance as a function of frequency; (b) equivalent crystal reactance as a function of frequency.

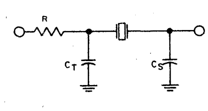


Fig. 4— Crystal pi-type feedback network.

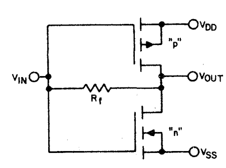


Fig. 5— COS/MOS amplifier.

Equivalent Crystal Resistance

The equivalent resistance R_s of the crystal should be maintained as small as possible in order to obtain minimum attenuation across the feedback network. For any given circuit, the oscillator current always increases with a rise in crystal resistance. This factor and stability considerations provide strong arguments for the purchase of crystals that have low series resistance, although the usual cost tradeoffs prevail.

Crystal Load Capacitance

Another factor that influences the over-all power consumption is the size of the pi-network capacitor at the amplifier output. For minimum current consumption, this capacitor, obviously, should be kept small. This condition, however, does not always imply high frequency stability. The choice of the capacitor value first involves a determination of the over-all crystal load capacitance. The phase angle of the feedback network approaches 180 degrees when the crystal equivalent reactive component X_e is equal to the reactance (X_{CL}) of a capacitor placed in parallel with the crystal. Fig. 4 shows that the effective capacitance across the crystal consists of the two pi-network capacitors in series. If the value of the equivalent reactance X_e at the crystal frequency, as may be determined from Fig. 3(b), is equal to the value of the crystal load capacitance C_L, then the equivalent value of the two series-connected pi-network capacitors can be calculated from the following relationship:

$$C_L = 1/\omega X_e \qquad (1)$$

The value of the load capacitance C_L, in general, is chosen first, and the crystal manufacturer is required to cut the crystal to oscillate at the desired frequency for the specified value of load capacitance.

The choice of a load capacitance is important in terms of over-all power consumption and frequency stability. Higher values of C_L generally improve frequency stability, but also increase power dissipation. The timing industry presently seems to have standardized on values of C_L between 10 and 20 picofarads.

The choice of the total equivalent load capacitance C_L only fixes the series sum of the two pi-network capacitors. The individual capacitors themselves can be found from the following equations:

$$C_T = 4C_L/(1 - 5fR_eC_L) \qquad (2)$$

$$C_S = 4C_L/(3 + 5fR_eC_L) \qquad (3)$$

The actual value of C_S used in the feedback circuit should be about 3 picofarads less than the calculated value to allow for the amplifier input capacitance. The value of the amplifier output capacitor C_T should not normally be fixed. A trimmer capacitor should be placed in parallel with, or used in place of, a fixed output capacitor to allow for variations in stray capacitance and circuit components. The mid-range value of the output capacitor combination should be equal to the calculated value of C_T.

Frequency-Trimming Capability

The required capacitance range for the oscillator trimmer capacitor is determined by the variation in oscillation frequency with a change in load capacitance.[2] The total frequency-trimming range of a crystal-controlled oscillator circuit is mainly a function of the crystal characteristics, or more explicity, is inversely proportional to the slope of the crystal reactance curve, shown in Fig. 3(b). The slope of this curve is a function of the difference between the resonant frequency f_r and the antiresonant frequency f_a. This frequency difference, in turn, is a function of the crystal capacitance ratio C_o/C_1, where C_o and C_1 are the inherent shunt and series capacitances, respectively, of the crystal structure, as shown in Fig. 2. The slope of the reactance curve is also a function of the total external crystal load capacitance C_L. As shown in Fig. 3(b), this slope decreases as the equivalent reactance increases, (i.e., for smaller values of the capacitance C_L). Fig. 6 and Table II show trimming-range data for a typical 32.768-kHz crystal that has a capacitance ratio C_o/C_1 of 580. These data show that smaller values of load capacitance result in greater trimming-range capability.

Temperature Stability

Another important oscillator consideration is temperature stability. Most crystals have a negative parabolic temperature coefficient.[2] Fig. 7 shows a typical curve of the variation in crystal frequency as a function of temperature. The frequency of the total oscillator circuit also exhibits a similar temperature dependence. Temperature compensation of the over-all oscillator circuit can be achieved by use of a capacitor that has a positive parabolic temperature coefficient in the pi feedback network.[3] For comparison, Fig. 7 also shows a typical resultant curve for the over-all circuit.

The temperature characteristics of a crystal are determined to a large extent by the crystal cut. Popular low-frequency cuts include the NT and XY Bar. The XY Bar is the more popular of the two types because it can be made smaller for a given Q and is easier to trim. The disadvantage of a slightly lower shock resistance of XY Bar crystals is compensated by the superior aging chacteristics of this type.

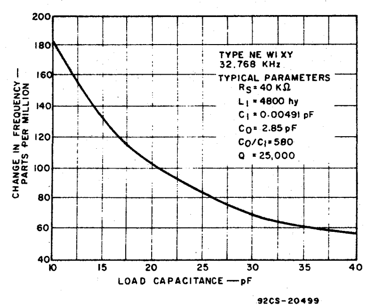


Fig. 6— Frequency as a function of load capacitance for a typical 32-kHz crystal.

AT-cut crystals, when used at frequencies greater than 1 MHz, are characterized by excellent temperature stability and ruggedness. Temperature characteristics for this type of crystal cut as well as for the XY Bar and NT types are shown in Fig. 8.

Crystal Dimensions

Size is also an important consideration in the design of oscillator crystals. The length of quartz required for any given cut is inversely proportional to the square root of frequency. Dimensions for a typical packaged 32-kHz, XY Bar crystal are 0.6 inch by 0.2 inch by 0.11 inch. The smallest XY Bar crystals currently available have dimensions in the order of 0.53 inch by 0.2 inch by 0.11 inch. A 1-MHz AT-cut crystal is significantly larger; however, dimensions again decrease with frequency. Crystal manufacturers are currently working to develop wristwatch-size AT-cut crystals with the anticipation of circuit improvements that will allow low-current operation at high frequencies.

Crystal Shock Resistance and Aging Rate

A prime concern of the timing industry today is that of crystal shock resistance and aging. The aging of a crystal results primarily from aging of the mounting material rather than from aging of the quartz itself. The mounting material enters into the crystal equivalent circuit, and the slowest aging rate results when the mount consists of the least amount of supporting material. This condition of course, results in lower shock resistance, and an optimum trade-off must be achieved. At present, 32-kHz crystals can be made that can withstand a mechanical shock of about 1500 G's applied for 0.5 millisecond and that have aging rates that result in a frequency change of 2 to 5 parts per million for the first year and essentially no aging thereafter. Any mechanical or thermal shock, however, will interrupt the normal aging process. The aging rate of 2 to 5 parts per million presently appears acceptable to the timing industry, although shock resistances of 3,000 to 5,000 G's are desired. This shock level corresponds approximately to the shock experienced by dropping the crystal from a height of one meter onto a hardwood floor.

Table II – Trimming Data for a Typical 32-kHz Quartz Oscillator Crystal

TRIM	LOAD CAPACITANCE, CL			
	5 pF	11.5 pF	20 pF	32 pF
± 20 PPM	−0.45 / +0.51 pf	−1.6 / +2.0 pf	−3.7 / +5.5 pf	−8.0 / +14.7 pf
± 25 PPM	−.55 / +.65 pf	−1.9 / +2.6 pf	−4.5 / +7.3 pf	−9.4 / +20.5 pf
± 30 PPM	−0.66 / +0.79 pf	−2.3 / +3.3 pf	−5.2 / +9.3 pf	−10.7 / +27.9 pf

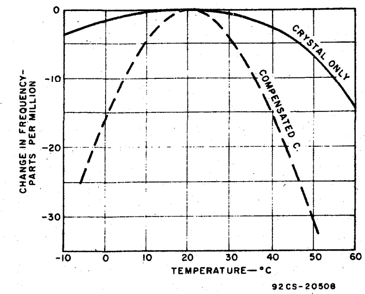


Fig. 7— Effect of temperature on crystal frequency.

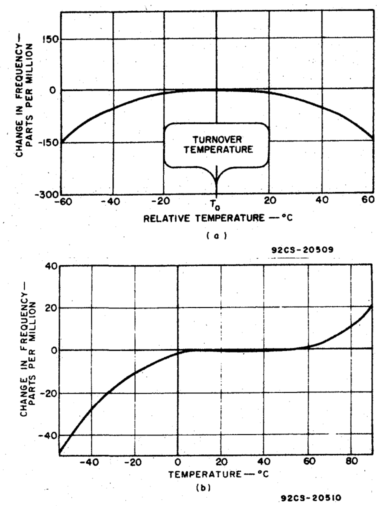


Fig. 8— Frequency-temperature characteristics for various crystal cuts: (a) XY-Bar and NT cuts; (b) AT cut.

PRACTICAL OSCILLATOR CIRCUITS

The basic amplifier, feedback-network, and crystal considerations discussed in the preceding paragraphs can be combined in the design of COS/MOS oscillator circuits. In the circuits, the crystal selected has an equivalent resistance R_e of 50 kilohms and is cut to operate at a frequency of 32.768 kHz with a load capacitance C_L of 10 picofarads. The values of pi feedback-network capacitors C_T and C_S can be calculated by use of Eqs. (2) and (3) as C_T = 43 picofarads and C_S = 13 picofarads. The value of the feedback-network resistance R can be calculated as follows:

$$R = \frac{(3X_e + 0.27\,R_e)(X_e - 0.8\,R_e)}{16\,R_e}$$

$$\approx 1\,M\Omega$$

This value is the maximum value of resistance allowd for a minimum feedback-network attenuation of 0.75, a value chosen on the basis of power and stability considerations.[1] The calculated value of R includes any fixed resistance plus the amplifier output resistance. Because the output resistance is often appreciable and varies with supply voltage, transistor size, and threshold voltages, it is generally best to add resistance experimentally until the desired power consumption and frequency stability are reached. The effect of this resistance on operating current and frequency stability can be predicted from data given in Table III for the three different COS/MOS crystal oscillator circuits shown in Fig. 9. In each circuit, the pi-network capacitors C_T and C_S are 39 picofarads and 10 picofarads, respectively. These capacitances are slightly less than the calculated values because of stray and amplifier capacitances.

The circuit shown in Fig. 9(a) combines the amplifier and feedback circuits shown in Fig. 4 and 5. Although theory predicts that an increase in the values of the feedback-network resistor R will result in increased frequency stability, the circuit performance data given in Table III show no significant improvement in this characteristic. This result indicates that the circuit instability can be attributed almost entirely to phase instabilities of the amplifier. This assumption is verified by data taken from the circuits shown in Figs. 9(b) and 9(c) in which the required feedback-network resistance is incorporated into the amplifier as a fixed value. The resistors essentially fix the amplifier phase shift so that greater stability results. As the data show, use of these resistors also results in a decrease in the total current consumption. Because of the two fixed resistors, the circuit of Fig. 9(b) shows the least current consumption and also the greatest stability.

Table III – Typical Oscillator Data

Circuit	Value of R (Ω)	V_{DD} (Volts)	Current (μA)	Frequency Stability V_{DD} = 1.45V to 1.6V
9(a)	0	1.60	4.0	2.8
"	0	1.45	3.1	
"	100K	1.60	3.1	2.6
"	"	1.45	2.4	
"	200K	1.60	2.9	2.6
"	"	1.45	2.1	
9(b)	100K	1.60	2.3	.3
"	"	1.45	2.0	
"	"	1.1	1.5	
"	150K	1.60	1.8	.2
"	"	1.45	1.6	
"	"	1.1	.95	
9(c)	200K	1.60	5.0	.6
"	"	1.45	4.4	
"	300K	1.60	3.5	.5
"	"	1.45	3.0	

As mentioned previously, the amplifier feedback resistor should not significantly load the crystal feedback network. The resistor value at which loading begins to occur can be determined from a curve of circuit operating frequency as a function of feedback resistance. Fig. 10 shows such a curve for the circuit shown in Fig. 9(b). This curve indicates that 15 megohms is a suitable value for the feedback resistor.

FREQUENCY DIVIDERS

Because of restrictions on crystal size and cost, oscillator frequencies of 8192 Hz, or higher, are generally used for electronic timing circuits. The use of such high crystal frequencies usually requires division of the oscillator frequency to a more convenient value. Synchronous motors, for example, are often driven by frequencies between 0.5 Hz and 64 Hz. Numeric readouts for digital clocks or wristwatches require pulses at least every second, minute, and hour. The necessity for frequency division becomes clear if one considers the wide variety of timing intervals that may be required for certain applications.

The basic frequency-dividing circuit, shown in Fig. 11, consists of a master-slave D-type flip-flop connected as a binary counter stage. N stages may be cascaded with the final output frequency equal to 2^{-N} times the input frequency. Division by integers other than powers of 2 can also be accomplished by use of gating techniques. For example, a divide-by-60 counter implemented as shown in Fig. 12, can be used to obtain minutes from seconds.

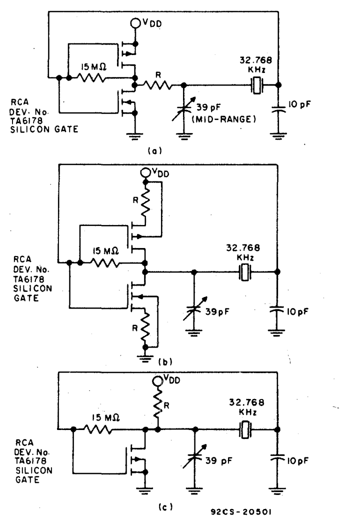


Fig. 9– Typical COS/MOS crystal-oscillator circuits.

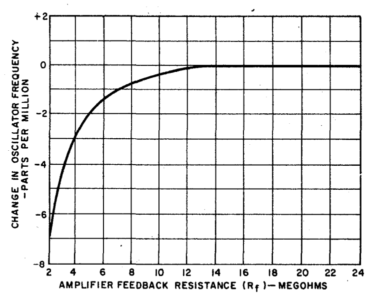


Fig. 10– Oscillator frequency as a function of amplifier feedback resistance.

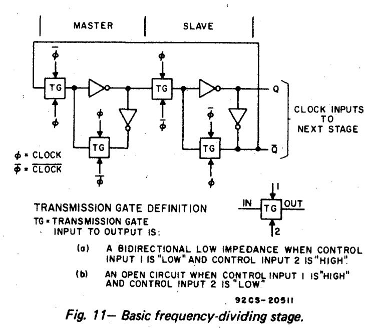


Fig. 11– Basic frequency-dividing stage.

A basic block diagram of a typical digital clock that employs divide-by-60 counters is shown in Fig. 13. The display for the clock is designed to be multiplexed in that new information is provided to only one of the six readout characters, while the eye itself holds the previous state of the other five. The multiplexing unit consists of COS/MOS transmission gates controlled by a six-stage ring counter that also addresses each character sequentially. This type of circuit is particularly applicable for driving light-emitting diode displays.

Light-emitting diodes, as well as other readout devices, require some form of driving circuitry which is often unique to the driven device. Other typical readout devices include stepping motors, balance-wheel motors, tuning-fork motors, and liquid-crystal displays.

Motors are frequently driven by low-impedance MOS transistor drivers. The waveforms required depend upon the particular type of motor. Rotary stepping motors require a pulsed waveform such as that shown in Fig. 14(a). The motor advances one position (for example 180 degrees) on each pulse. Fig. 14(b) shows a COS/MOS circuit that may be used to generate this type of waveform. The crystal frequency and the number of countdown stages for this circuit determine the pulse frequency. The duty factor is controlled by two resettable flip-flops that are clocked inversely by the last counting stage and reset by an intermediate stage. The output waveform from this circuit will have a duty factor that is exactly given by 2^{I-1-N} where I is the number of the intermediate stage used to reset the shaping flip-flops and N is the total number of frequency-divider stages.

A tuning-fork motor consists of two coils wired in series and wound on either side of the fork. A subdivision of the crystal frequency drives the coils which electromagnetically vibrate the fork. The fork can be linked to an index wheel that, in turn, can drive the hands of a watch.

A balance-wheel motor consists of a coil fixed near the periphery of a pivoted balance wheel. Permanent magnets are attached to one side of the wheel and counterweights to the other. The coil can be energized by pulses supplied to the gate of an n-channel MOS transistor with the coil connected between the drain and the supply voltage of the transistor. When the coil is energized, the balance wheel swings toward the coil. The momentum of the wheel moves it beyond the coil, and spring action then forces it back. Repeated cycles generate a back-and-forth type motion which can be linked to a wheel for driving the hands of a watch or clock.

Seven-segment liquid-crystal numerals can be driven as shown in Fig. 15. An ac voltage is required across each segment of the display to assure long life. For this purpose, a 60-Hz square wave is applied to one input of each of seven exclusive-OR gates. The logic state present at the other input determines whether the segment will transmit or scatter light.

Liquid-crystal displays can be made for operation in either transmissive or reflective modes. The transmissive-mode type requires a light source behind the display. The light will either be transmitted or not depending upon the voltage across the segment. In the reflective-mode type, ambient light can be scattered by the liquid crystal material, or reflected from a mirrored surface placed behind the numeral. If displayed correctly, excellent contrast between "on" and "off" segments can be obtained when reflecting or scattering only ambient light.

The light scattering property of liquid-crystal displays offers two major advantages. First, the problem of washout in high intensity light is prevented. Washout has always been a problem with light generating displays. Second, because the displays do not generate light, they require negligible power. In fact, liquid crystals require the least amount of power of any currently available type of display.[4]

Light-emitting diodes are somewhat simpler to drive than liquid crystals because signals to individual segment and/or numerals can be easily multiplexed. Fig. 16 shows a typical multiplexed driving circuit. The n-p-n transistor, which is common to the cathode of all segments in each numeral, can be turned on to address only one particular numeral. The eye will hold the reading from all off segments long enough for at least six numerals to be multiplexed.

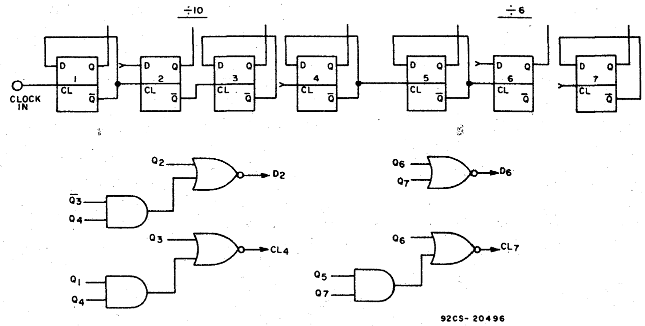


Fig. 12– COS/MOS divide-by-60 counter.

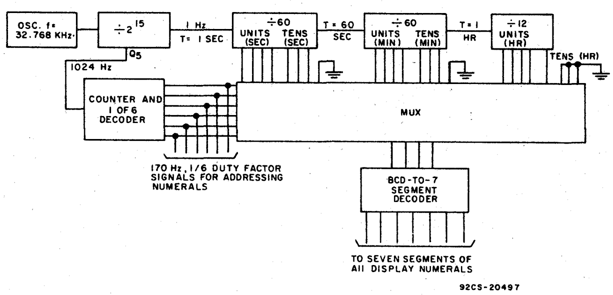


Fig. 13– Typical COS/MOS digital clock.

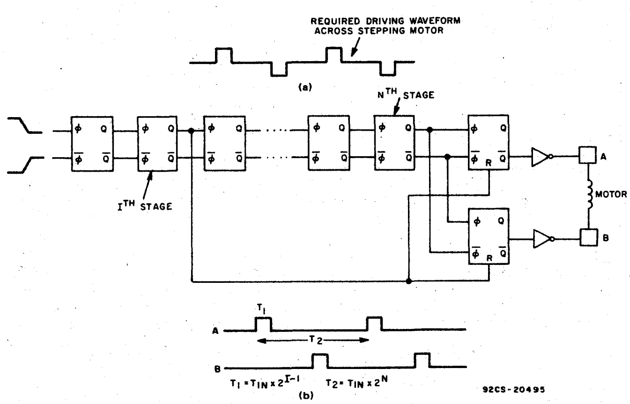


Fig. 14– Generation of required stepping-motor waveforms: (a) required driving waveform across stepping motor; (b) COS/MOS driving circuit and output waveforms applied to motor control winding.

COS/MOS TIMING-CIRCUIT APPLICATIONS

The choice of a readout device depends, of course, upon the application involved and to a certain extent upon the individual characteristics of the device itself. Special considerations for readout devices are perhaps best treated in a discussion of special requirements for three important timing-circuit applications, namely, wristwatches, wall clocks, and automobile clocks.

Wristwatches

In any wristwatch application, size and total operating current are perhaps the two most important considerations. The total timing circuitry, together with the battery and readout device, must fit into a relatively fixed size and have a current consumption small enough to allow at least one year of life. Size and power considerations also become important in crystal selection. The size and cost of a crystal decreases with increases in frequency up to about 1 MHz. The power consumption of the oscillator and counter increases with frequency. On the basis of these considerations, the most popular crystal frequency for wristwatches at present is 32.768 kHz. Typical packaged sizes for this crystal and various available crystal oscillator circuits were discussed in an earlier section of this Note.

The choice of a readout device also involves considerations of size and power as well as, of course, marketing considerations. If conventional-hand movements are chosen, a motor type of drive must be selected. No great size advantage exists over any of the various motor types used in this type of application. In addition, all types can be designed to operate from 1.1 to 1.6 volts with average current consumptions of about 10 microamperes. Sensitivity to vibration, however, is one separating characteristic. Although balance-wheel motors can be designed to compensate to a certain extent for speed variations produced by vibrations, the stepping motor, which is insensitive to vibration, remains superior in this respect. At present, however, the stepping motor is the more expensive of the two types.

Light-emitting diodes require a minimum of two battery cells for proper operation. The required current can be kept to about 2 milliamperes per segment when the diodes are pulsed from a six-stage ring counter, as shown in Fig. 13. A duty factor of 16 per cent is achieved with this arrangement. Because of the high current, however, a continuously operating battery-powered display is not possible, and a "readout on demand" watch is then necessary.

Continuously operating liquid-crystal displays are possible and practical. RCA wristwatch displays employ liquid-crystal material having resistivities of about 5 x 10^9 ohms per centimeter, which at a 0.5-mil spacing results in a resistance of 6.3 megohms per square centimer. With all segments energized, the display consumes only about 1 microampere of current at 15 volts. Liquid crystals, however, require a minimum supply of 12 volts to assure good contrast between on and off segments. For single-cell operation, a dc-to-dc converter must be used to step the voltage up to the required 12-to-15-volt level. Transformer and capacitor voltage-doubling circuits with conversion efficiencies of about 75 per cent are typically used for this purpose.

Because current consumption is such an important consideration for wristwatch circuits, the careful consideration given to the choice of a battery is easily understood. Small silver-oxide and mercury cells are presently popular for wristwatch use. Pertinent information on these types of

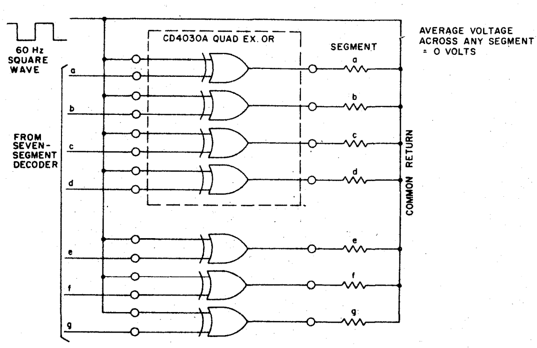


Fig. 15– COS/MOS liquid-crystal driving circuit.

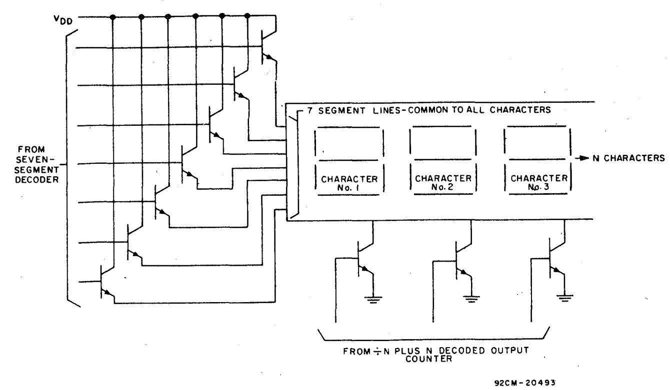


Fig. 16– Multiplexing driving circuit for light-emitting diodes.

Mallory cells is shown in Table IV. Most of the cells listed will last at least one year with a motor current of 10 microamperes and a total oscillator and divider current less than 5 microamperes at an oscillator frequency of 32.768 kHz. The voltage for both types of cells is relatively constant during the active life listed and falls off rapidly thereafter. Typical end-of-life voltages at 1.1 volts for mercury cells and 1.45 volts for silver-oxide cells. Either type of cell works equally well with RCA silicon-gate COS/MOS circuits which operate from supply voltages as low as 1.1 volts.

Wall Clocks

Size and power limitations for clocks are not as restrictive as those for wristwatches. For this reason, lower-cost, higher-frequency crystals may be used. The optimum range of crystal frequencies presently appears to be from 131 kHz to 524 kHz. All the oscillator considerations given previously for operation at 32 kHz apply equally well to this higher frequency range. The oscillator circuit configuration shown in Fig. 9(b) is still the optimum type; however, the value of the source resistors must be decreased to assure adequate gain at the higher frequencies. Source resistors are often best chosen experimentally by gradually increasing the resistance until an output voltage swing of 30 to 70 per cent of the supply voltage V_{DD} is reached. Data taken from a typical 262-kHz oscillator circuit that employs two 10-kilohm source resistors and a DT-cut, 262-kHz crystal are shown in Table V. The table also shows typical counter current.

The most popular readout devices for clocks are conventional-hand movements and liquid-crystal displays. Continuously operating light-emitting-diode numerals consume too much current even for long life of C- and D-size batteries. In contrast, a typical RCA four-digit liquid-crystal

Table IV – Typical Data for Mallory Watch Cells

Type	Voltage	Capacity µA yrs.	Height (in.)	Diameter (in.)
WH3	1.35	25	0.208	0.455
WS 14 Type A	1.55	19	0.210	0.455
W4	1.35	11	0.139	0.455
WS11	1.55	11	0.164	0.455
10 R 101 (EXP)	1.35	36	0.190	0.610
10 L 19 (EXP)	1.55	27	0.190	0.610
WD4	1.36	14	0.149	0.594
WD5	1.36	23	0.110	1.003

display having a 0.4-inch-by-0.6-inch numeral consumes only 100 microamperes of current with all segments energized.

Motors for driving the clock hands are typically of the balance-wheel or continuously rotating synchronous types. Sensitivity to vibration is usually not a restriction; hence, the balance wheel motor can be successfully used in place of the more expensive stepping motor. Clock motors typically require about 300 to 450 microwatts of power, or average currents of 200 to 300 microamperes at 1.5 volts.

These currents, together with the oscillator and counter currents given in Table V, can now be compared with typical battery capacities. Battery information extrapolated from published Eveready data on popular AA-, C-, and D-size cells is listed in Table VI.[5] Most of the battery current is consumed by the motor, and if a total current of 250 microamperes is assumed, the data show a carbon-zinc C cell as the minimum size battery required for one year of life.

Auto Clocks

Auto clock circuits are somewhat unique in that power considerations are not nearly as restrictive as in other portable applications. Although the low-power feature of COS/MOS circuits is helpful, the main advantages obtained

Table V – Typical Data for 262-kHz Oscillator and Counter Circuits

Product	V_{DD} (Volts)	Oscillator Current (µA)	Counter Current (µA)	Freq. Stability (ppm)
Silicon-Gate	1.1V	7	7	2.0 ppm
"	1.3V	9.5	9	1.4
"	1.5V	11.5	10	1.2
"	1.6V	12.5	11	
Low-Voltage	2.2V	21	10	1.8
"	3.0V	35	13	

from the use of COS/MOS in automobile clocks, or in any automotive application, are those of wide operating voltage and temperature range and high noise immunity.

With little restriction on power, the choice of a crystal depends mainly on cost. Crystals typically used for automobile timing applications are AT-cut types that operate at frequencies between 1 MHz and 4.2 MHz. The oscillator considerations discussed earlier also apply to these frequencies; however, as the frequency increases, it becomes increasingly difficult to maintain a low starting voltage at a low current. At high frequencies, the starting voltage and current are inversely proportional and are controlled mainly by the values of the capacitors on the pi-type feedback network and the size of the COS/MOS amplifier transistors.

Table VI – Life Data for Typical Batteries

Eveready Type #	Mallory Type #	Size	Type	Life (Days)
915	M15F	AA	Carbon-Zinc	150
E91	MN1500	AA	Alkaline	200
935	M14F	C	Carbon-Zinc	385
E93	MN1400	C	Alkaline	575
950	M13F	D	Carbon-Zinc	800
E95	MN1300	D	Alkaline	1100

All life data assumes a continuous drain of 250 µA and an end-of-life voltage of 1.1V.

For minimum starting voltage, relatively small capacitors should be used in the pi-feedback network, and no source resistors should be added to the amplifier. As indicated by data taken on the circuit shown in Fig. 9(b) and shown in Table VII, low power can still be maintained even when the source resistors are not used.

Table VII – Typical High-Frequency Data for COS/MOS Oscillator and Counter Circuits (Low-Voltage Product)

V_{DD} (Volts)	Freq. (MHz)	Oscillator Current (mA)	Counter Current (mA)	Motor Current (mA)
5	1	0.28	0.125	5V
12	1	1.3	0.275	2-5 mA
5	2	0.37	0.250	12V
12	2	1.5	0.550	5-10 mA
5	3	0.40	0.375	5V
12	3	1.9	0.825	3-8 mA
5	4	0.43	0.500	12V
12	4	2.3	1.1	8-20 mA

The upper limit of the crystal frequency depends not so much on power consumption as on the minimum supply voltage allowed for circuit operation. The minimum automobile battery voltage is generally considered to be 5 volts; however, the supply voltage for the timing circuit can be considerably less than this value depending upon the design of the transient protection circuit, as discussed later. Table VIII lists minimum COS/MOS supply voltages for typical oscillator circuits. The values shown permit design at two temperatures. The lower temperature is often considered adequate by auto companies with the opinion that the minimum battery voltage of 5 volts rarely, if ever, occurs at high temperatures.

The oscillator in a typical auto clock circuit is followed by a number of frequency-dividing stages, the last stage of which is frequently used to drive a motor. Long counter chains are required because of the high oscillator frequency; however, the power dissipation of COS/MOS circuits is so low that the number of stages is only restricted by chip size limitations. Because COS/MOS circuits consume current only during switching transitions, each counter stage averages one-half the current of the previous stage. The first counter stage, therefore, consumes as much current as all of the following stages combined for a counter of infinite length. Little difference, then, exists between the power consumption of a ten-stage or thirty-stage COS/MOS counter. Table VII lists, in addition to the oscillator current, typical values of counter current, as well as some typical ranges of peak and average motor currents.

Current data, such as that shown in Table VII, are necessary for a proper design of the transient protection circuit, an essential part of any automobile digital logic system. Automobile manufacturers disagree on the maximum amplitude and decay of transient voltage; however, values often used are maximum transients of +120 volts and −90 volts, each decaying exponentially with a maximum time constant of 45 milliseconds. Because standard COS/MOS circuits are rated for a maximum supply of 15 volts, a protection circuit must be included between the battery and the COS/MOS logic.

Table VIII – Minimum Operating Voltages for COS/MOS Integrated Circuits

	Low-Voltage Product				Silicon-Gate Product			
Freq. (MHz)	1	2	3	4	1	2	3	4
Min. Voltage at 25°C	2.9	3.1	3.5	4.0	1.6	2.0	2.6	3.0
Min. Voltage at 82°C 180°F	3.0	3.3	4.0	5.0	1.8	2.6	3.4	4.0

Fig. 17 shows a transient-voltage protection circuit that is frequently used. The zener diode regulates the voltage supply for the clock circuits, and the capacitor and series diode prevent timing losses during negative transients. For minimum zener current during transients, the maximum value of R should be based on the minimum circuit operating voltage and the peak current drawn by the logic circuit and motor at the minimum battery voltage. The minimum zener breakdown voltage is then determined by subtraction of the product of the minimum current drain at the normal battery voltage and the value of R just chosen from the battery voltage. A zener breakdown greater than this voltage assures that no unnecessary current will be drawn by the zener during normal automobile operation.

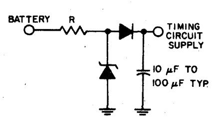


Fig. 17– Automobile transient-protection circuit.

Another important zener characteristic is dynamic impedance. During a current surge, the voltage across the zener must not rise to a damaging level. A value of 22 volts for the 45-millisecond time constant appears safe for standard COS/MOS circuits.

In the design of a typical transient-voltage protection circuit, it is assumed that the minimum battery voltage is 5 volts, that the minimum circuit operating voltage is 3.5 volts at a crystal frequency of 3.145728 MHz, and that a peak current of 3 milliamperes is obtained at 5 volts. The value of the resistance R is then found as $(5 - 3.5 + 0.7)/3 \approx 250$ ohms. With a minimum current of 5 milliamperes at 12 volts, the minimum zener voltage becomes $12 - 5(0.250) = 11.75$ volts. For a +120-volt transient, the zener could then consume a peak current of $(120 - 11.8)/250 = 0.4$ ampere. For a maximum zener voltage of 13 volts, the dynamic impedance of the zener must be less than $(22V - 13V)/.4A = 22$ ohms. Components chosen in this manner will provide adequate protection for anticipated transients.

Both protection-circuit diodes can be integrated onto the COS/MOS chip. When located as shown in Fig. 17, the series diode need only have a breakdown rating of about 12 volts. Zener diodes that have breakdown ratings of 4.5 to 6.0 volts or any multiple thereof can also be integrated onto the COS/MOS chip. The breakdown rating can also be increased in 0.7-volt steps by addition of forward-biased diodes in series. Characteristics of two typical zener diodes integrated in series are shown in Fig. 18. Fig. 18(a) shows the area around the "knee" of the breakdown region, and Fig. 18(b) shows the higher-current region useful for determining the dynamic resistance. From the slope of the line, the typical dynamic resistance for two diodes is found to be 17.6 ohms total, or 8.8 ohms per diode. The diodes are rated to withstand a 0.5-ampere surge current that decays with an 80-millisecond time constant. The zener diode, then, is compatible with present automobile protection requirements, and integration of this component should represent a considerable cost saving, especially when integrated with the series diode.

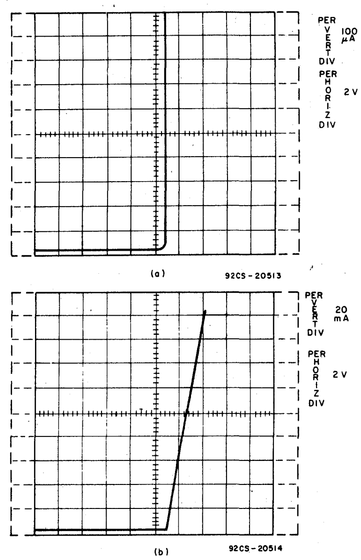


Fig. 18– Oscillograph tracings showing characteristics of an integrated zener diode: (a) low-current region; (b) high-current region.

Other Applications

Although wristwatches and clocks of various types are important applications of COS/MOS timing circuits, they are certainly not the only timing applications which can benefit from the unique features of COS/MOS logic. Applications such as fuze timers, feeding systems, automatic sprinklers, incubator timers, and other similar systems can be designed from information provided on the oscillator and counter with only the output device unique to the particular application. Automobile applications for COS/MOS circuits are almost endless. One can think of speed controllers, digital speedometers, miles per gallon indicators, and perhaps even estimated-time-of-arrival indicators that, on the basis of the given total mileage, would update the time on a dynamic basis from information provided by the speedometer, odometer, and clock.

CONCLUSIONS

The primary advantage of electronic timing circuits over conventional mechanical methods of timekeeping lies in the greatly increased accuracy permitted by the highly stable crystal-controlled oscillator circuit. Although crystal oscillator circuits have existed for some time, their usefulness in portable applications has been somewhat limited because of the high current consumption required by the following digital logic. The advent of COS/MOS integrated circuits now permits the design of complete low-power timing systems. The impact of COS/MOS on timing applications is perhaps equalled by the recent development of liquid-crystal displays and dc-to-dc converters that allow low-power continuously operating digital displays. Certainly, no great technological barriers now exist for the use of electronic timing circuits in a wide variety of applications. The search, no doubt, will always continue for the ideal timekeeping device; however, it should be apparent from the information presented that the ideal timekeeping unit can now be more closely approached than ever before.

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ICAN-6101

The RCA COS/MOS Phase-Locked-Loop A Versatile Building Block for Micro-Power Digital and Analog Applications

INTRODUCTION

Phase-locked-loops (PLL's), especially in monolithic form, are finding significantly increased usage in signal-processing and digital systems. FM demodulation, FSK demodulation, tone decoding, frequency multiplication, signal conditioning, clock synchronization, and frequency synthesis are some of the many applications of a PLL. The PLL described in this Note is the COS/MOS CD4046A, which consumes only 600 microwatts of power at 10 kHz, a reduction in power consumption of 160 times when compared to the 100 milliwatts required by similar monolithic bipolar PLL's. This power reduction has particular significance for portable battery-operated equipment. This Note discusses the basic fundamentals of phase-locked-loops, and presents a detailed technical description of the COS/MOS PLL as well as some of its applications.

REVIEW OF PLL FUNDAMENTALS

The basic phase-locked-loop system is shown in Fig. 1; it consists of three parts: phase comparator, low-pass filter, and voltage-controlled oscillator (VCO); all are connected to form a closed-loop frequency-feedback system.

With no signal input applied to the PLL system, the error voltage at the output of the phase comparator is zero. The voltage, Vd(t), from the low-pass filter is also zero, which causes the VCO to operate at a set frequency, fo, called the center frequency. When an input signal is applied to the PLL, the phase comparator compares the phase and frequency of the signal input with the VCO frequency and generates an error voltage proportional to the phase and frequency difference of the input signal and the VCO. The error voltage, Ve(t), is filtered and applied to the control input of the VCO; Vd(t) varies in a direction that reduces the frequency difference between the VCO and signal-input frequency. When the input frequency is sufficiently close to the VCO frequency, the closed-loop nature of the PLL forces the VCO to *lock* in frequency with the signal input; i.e., when the PLL is in lock, the VCO frequency is identical to the signal input except for a finite phase difference. The range of frequencies over which the PLL can maintain this locked condition is defined as the *lock range* of the system. The lock range is always larger than the band of frequencies over which the PLL can acquire a locked condition with the signal input. This latter band of frequencies is defined as the *capture range* of the PLL system.

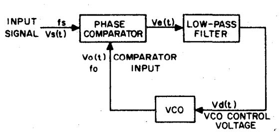


Fig. 1— Block diagram of PLL.

TECHNICAL DESCRIPTION OF COS/MOS PLL

Fig. 2 shows a block diagram of the COS/MOS CD4046A, which has been implemented on a single monolithic integrated circuit. The PLL structure consists of a low-power, linear, voltage-controlled oscillator (VCO), and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2-volt zener is provided for supply regulation if necessary. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. The low-pass filter is implemented through external parts because of the radical configuration changes from application to application and because some of the components are non-integrable. The CD4046A is supplied in a 16-lead, dual-in-line, ceramic package (CD4046AD); a 16-lead, dual-in-line, plastic package (CD4046AE); or a 16-lead flat-pack (CD4046AK). It is also available in chip form (CD4046AH).

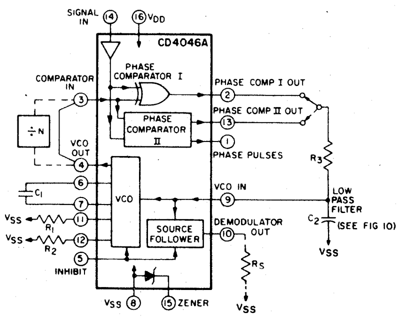


Fig. 2— COS/MOS PLL block diagram.

Phase Comparators

Most PLL systems utilize a balanced mixer composed of well-controlled analog amplifiers for the phase-comparator section. Analog amplifiers with well-controlled gain characteristics cannot easily be realized using COS/MOS technology. Hence, the COS/MOS design shown in Fig. 3 employs digital-type phase comparators. Both phase comparators are driven by a common-input amplifier configuration composed of a bias stage and four inverting-amplifier stages. The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within COS/MOS logic levels [logic 0 ≤ 30% (VDD-VSS), logic 1 ≥ 70% (VDD-VSS)]. For smaller input signal swings, the signal must be capacitively coupled to the self-biasing amplifier at the signal input to insure an over-driven digital signal into the phase comparators.

Phase-comparator I is an exclusive-OR network; it operates analagously to an over-driven balanced mixer. To maximize the lock range, the signal and comparator input frequencies must have 50-percent duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to VDD/2. The low-pass filter connected to the output of phase-comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_o). With phase-comparator I, the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

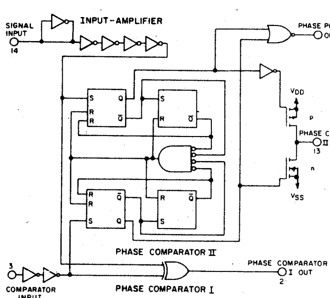


Fig. 3— Schematic of COS/MOS PLL phase-comparator section.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. 4 shows the typical, triangular, phase-to-output, response characteristic of phase-comparator I. Typical waveforms for a COS/MOS phase-locked-loop employing phase-comparator I in locked condition of f_o is shown in Fig. 5.

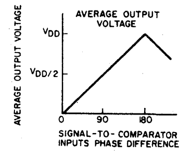


Fig. 4— Phase-comparator I characteristics at low-pass filter output.

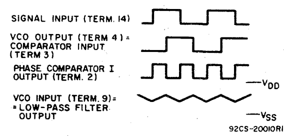


Fig. 5— Typical waveforms for COS/MOS phase-locked loop employing phase-comparator I in locked condition of f_o.

Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p and n drivers having a common output node as shown in Fig. 3. When the p-MOS or n-MOS drivers are ON, they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal- and comparator-input signals. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-MOS output driver is maintained ON continuously. If the signal-input frequency is lower than the comparator-input frequency, the n-MOS output driver is maintained ON continuously. If the signal- and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-MOS output driver is maintained ON for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but the signal input leads the comparator input in phase, the p-MOS output driver is maintained ON for time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this type of phase comparator is adjusted until the signal and comparator input are equal in both phase and frequency. At this stable operating point, both p- and n-MOS output drivers remain OFF, and thus the phase-comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover, the signal at the "phase pulses" output is at a high level, and can be used for indicating a locked condition. Thus, for phase-comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-MOS output drivers are OFF for most of the signal-input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase-comparator II. Fig. 6 shows typical waveforms for a COS/MOS PLL employing phase-comparator II in a locked condition.

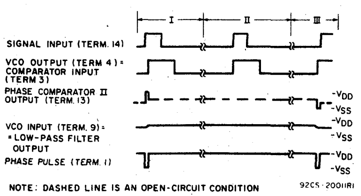


Fig.6 – Typical waveforms for COS/MOS phase-locked loop employing phase-comparator II in locked condition.

Fig. 7 shows the state diagram for phase-comparator II; each circle represents a state of the comparator. The number at the top inside each circle represents the state of the comparator, while the logic state of the signal and comparator inputs, represented by a 0 or a 1, are given by the left and right numbers, respectively, at the bottom of each circle. The transitions from one state to another result from either a logic change on the signal input (I) or the comparator input (C). A positive transition and a negative transition are shown by an arrow pointing up or down, respectively. The state diagram assumes that only one transition on either the signal input or the comparator input occurs at any instant. States 3, 5, 9, and 11 represent the condition at the output of phase-comparator II when the p-MOS driver is ON, while states 2, 4, 10, and 12 determine the condition when the n-MOS driver is ON. States 1, 6, 7, and 8 represent the condition when the output of phase-comparator II is in its high impedance state; i.e., both p- and n-devices are OFF, and the phase-pulses output (terminal 1) is high. The condition at the phase-pulses output for all other states is low.

As an example of how one may use the state diagram shown in Fig. 7, consider the operation of phase-comparator II in the locked condition shown in Fig. 6. The waveforms shown in Fig. 6 are broken up into three sections: section I corresponds to the condition in which the signal input leads the comparator input in phase, while section II corresponds to a finite phase difference. Section III depicts the condition when the comparator input leads the signal input in phase. These three sections all correspond to a locked condition for the COS/MOS PLL; i.e., both signal- and comparator-input signals are of the same frequency but differ slightly in phase. Assume that both the signal inputs begin in the 0 state, and that phase-comparator II is initially in its high-impedance output condition (state 1), as shown in Figs. 7 and 6, respectively. The signal input makes a positive transition

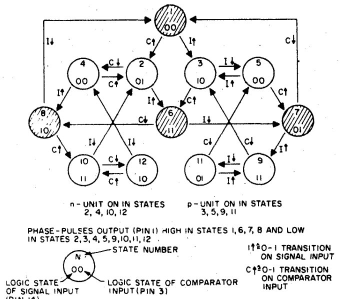


Fig. 7– State diagram of phase-comparator II.

first, which brings phase-comparator II to state 3. State 3 corresponds to the condition of the comparator in which the signal input is a 1, the comparator input is a 0, and the output p-device is ON. The comparator input goes high next, while the signal input is high, thus bringing the comparator to state 6, a high-impedance output condition. The signal input goes to zero next, while the comparator input is high, which corresponds to state 7. The comparator input goes low next, bringing phase-comparator II back to state 1. As shown for section I, the p-device stays on for a time corresponding to the phase difference between the signal input and the comparator input. Starting in state 1 at the beginning of section III, the comparator input goes high first, while the signal input is low, bringing the comparator to state 2. Following the example given for section I, the comparator proceeds from state 2 to states 6 and 8 and then back to 1. The output of phase-comparator II for section III corresponds to the n-device being on for a time corresponding to the phase difference between the signal and comparator inputs.

The state diagram of phase-comparator II completely describes all modes of operation of the comparator for any input condition in a phase-locked-loop.

Voltage-Controlled Oscillator

Fig. 8 shows the schematic diagram of the voltage-controlled oscillator (VCO). To assure low system-power dissipation, it is desirable that the low-pass filter consume little power. For example, in an RC filter, this requirement dictates that a high-value R and a low-value C be utilized. The VCO input must not, however, load down or modify the characteristics of the low-pass filter. Since the VCO design shown utilizes an n-MOS input configuration having practically infinite input resistance, a great degree of freedom is allowed in selection of the low-pass filter components.

The VCO circuit shown in Fig. 8 operates as follows: when the inhibit input is low, P_3 is turned full ON, effectively connecting the sources of P_1 and P_2 to V_{DD}; and gates 1 and 2 are permitted to function as NOR-gate flip-flops. N1 together with external-resistor R1 form a source-follower configuration. As long as the resistance of R1 is at least an order of magnitude greater than ON resistance of N_1 (greater than 10 kilohms), the current through R1 is linearly dependent on the VCO input voltage. This current flows through P_1, which, together with P2, forms a current-mirror network. External resistor R2 adds an additional constant current through P1; this current offsets the VCO operating frequency for VCO input signals of 0 volts. In the current-mirror network, the current of P2 is effectively equal to the current through P1 independent of the drain voltage at P2. (This condition is true provided P2 is maintained in saturation; in the circuit shown, P2 is saturated under all possible operating conditions and modes). The set/reset flip-flop composed of gates 1 and 2 turns ON either P4 and N3, or P5 and N2. One side of the external capacitor C1 is, therefore, held at ground, while the other side is charged by the constant current supplied by P2. As soon as C1 charges to the point at which the transfer point of inverters 1 or 5 is reached, the flip-flop changes state. The

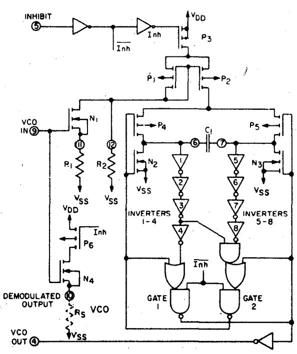


Fig. 8– Schematic of COS/MOS VCO section.

charged side of the capacitor is now pulled to ground. The other side of the capacitor goes negative, and discharges rapidly through the drain diode of the OFF n-device. Subsequently, a new half-cycle starts. Since inverters 1 and 5 have the same transfer points, the VCO has a 50-percent duty-cycle. Inverters 1 through 4 and 5 through 8 serve several purposes: (1) they shape the slow-input ramp from capacitor C1 to a fast waveform at the flip-flop input stage, (2) they maintain low power dissipation through the use of high-impedance devices at inverters 1 and 5 (slow-input wave-forms), and (3) they provide four inverter delays before removal of the set/reset flip-flop triggering pulse to assure proper toggling action.

In order not to load the low-pass filter, a source-follower ouput of the VCO input voltage is provided (demodulated output). If this output is used, a load resistor (Rs) of 10 kilohms or more should be connected from this terminal to ground. If unused, this terminal should be left open. A logic 0 on the inhibit input enables the VCO and the source follower, while a logic 1 turns off both to minimize stand-by power consumption.

Performance Summary of COS/MOS PLL

The maximum ratings for the CD4046A COS/MOS PLL, as well as its general operating-performance characteristics are outlined in Table I. The VCO and comparator characteristics are shown in Tables II and III, respectively. Table IV summarizes some useful formulas as a guide for approximating the values of external components for the CD4046A in a phase-locked-loop system. When using Table IV, one should keep in mind that frequency values are in kilohertz, resistance values are in kilohms, and capacitance values are in microfarads. The selected external components must be within the following ranges:

$$10\ K\Omega \leq R_1, R_2, R_s \leq 1\ M\Omega$$
$$C_1 \geq 100\ pF \text{ at } V_{DD} \geq 5\ V$$
$$C_1 \geq 50\ pF \text{ at } V_{DD} \geq 10\ V$$

In addition to the given design information, refer to Fig. 9 for R_1, R_2, and C_1 component selections. The use of Table IV in designing a COS/MOS PLL system for some familiar applications is discussed below.

APPLICATIONS OF THE COS/MOS PLL

The COS/MOS phase-locked-loop is a versatile building block suitable for a wide variety of applications, such as FM demodulators, frequency synthesizers, split-phase data synchronization and decoding, and phase-locked-loop lock detection.

FM Demodulation

When a phase-locked-loop is locked on an FM signal, the voltage-controlled oscillator (VCO) tracks the instantaneous frequency of that signal. The VCO input voltage, which is the filtered error voltage from the phase detector, corresponds to the demodulated output. Fig. 11 shows the connections for the COS/MOS CD4046A PLL as an FM demodulator. For this example, an FM signal consisting of a 10-kilohertz carrier frequency was modulated by a 400-Hz audio signal. The total FM signal amplitude is 500 millivolts, therefore the signal must be ac coupled to the signal input (terminal 14).

Table I– Maximum ratings and general operating characteristics

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage Temperature Range	–65°C to +150	°C
Operating Temperature Range:		
Ceramic Package Types	–55°C to +125	°C
Plastic Package Types	–40°C to +85	°C
DC Supply Voltage Range (V_{DD} – V_{SS})	–0.5 V to +15	V
Device Dissipation (Per Pkg.)	200	mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$	
Recommended DC Supply Voltage (V_{DD} – V_{SS})	5 to 15	V
Recommended Input Voltage Swing	V_{DD} to V_{SS}	

General Characteristics (Typical Values at $V_{DD} - V_{SS}$ = 10 V and T_A = 25°C)

Operating Supply Voltage (V_{DD} – V_{SS})		5 to 15 V
Operating Supply Current		
Inhibit = "0" @ C_1 = 0.0001 μF, R_1 = 1 MΩ	f_0 = 10 kHz, V_{DD} = 5 V	70 μW
	f_0 = 10 kHz, V_{DD} = 10 V	600 μW
Inhibit = "1"		25 μA

Table II – VCO electrical characteristics

VCO Characteristics (Typical Values at $V_{DD} - V_{SS}$ = 10 V and T_A = 25°C)

Maximum Frequency	1.2 MHz
Temperature Stability	600 ppm/°C
Linearity ($V_{VCO\ in}$ = 5 V ± 2.5 V)	1%
Center Frequency	Programmable with R_1 and C_1
Frequency Range	Programmable with R_1, R_2, and C_1
Input Resistance	10^{12} Ω
Output Voltage	10 $V_{p\text{-}p}$
Duty Cycle	50%
Rise & Fall Times	50 ns
Output Current Capability	
"1" Drive @ V_O = 9.5 V	−1.8 mA
"0" Sink @ V_O = 0.5 V	2.6 mA
Demodulated Output:	
Offset Voltage ($V_{VCO\ in} - V_{DEMOD\ out}$) @ 1 mA	1.5 V

Table III – Comparator electrical characteristics
Comparator Characteristics (Typical Values at $V_{DD} - V_{SS}$ = 10 V and T_A = 25°C)

Signal Input	
Input Impedance	400 KΩ
Input Sensitivity	
ac coupled	400 mV
dc coupled	"0" ≤ 30% ($V_{DD} - V_{SS}$) "1" ≥ 70% ($V_{DD} - V_{SS}$)
Comparator Input Levels (term. 3)	"0" ≤ 30% ($V_{DD} - V_{SS}$) "1" ≥ 70% ($V_{DD} - V_{SS}$)
Output Current Capability	
Comparator I (term. 2) and Comparator II (term. 13):	
"1" Drive @ V_O = 9.5 V	−1.8 mA
"0" Sink @ V_O = 0.5 V	2.6 mA
Comparator II Phase Pulses (term. 1):	
"1" Drive @ V_O = 9.5 V	−0.5 mA
"0" Sink @ V_O = 0.5 V	1.4 mA

Phase-comparator I is used for this application because a PLL system with a center frequency equal to the FM carrier frequency is needed. Phase comparator I lends itself to this application also because of its high signal-input-noise-rejection characteristics.

The formulas shown in Table IV for phase-comparator I with $R_2 = \infty$ are used in the following considerations. The center frequency of the VCO is designed to be equal to the carrier frequency, 10 kHz. The value of capacitor C_1, 500 pF, was found by assuming an R_1 = 100 KΩ for a supply voltage V_{DD} = 5 volts.

These values determined the center frequency:

$$f_o = 10\ \text{kHz}$$

The PLL was set for a capture-range of

$$f_c \approx \pm \frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{R_3 C_2}} = \pm 0.4\ \text{kHz}$$

to allow for the deviation of the carrier frequency due to the audio signal. The components shown in Fig. 10 for the low-pass filter (R_3 = 100 kΩ, C_2 = 0.1 μF) determine the above capture frequency.

The total current drain at a supply voltage of 5 volts for this FM-demodulator application is 132 microamperes for a 4 dB S/N-ratio on the signal input, and 90 microamperes for a 10dB S/N ratio. The power consumption decreases because the signal-input amplifier goes into saturation at higher input levels.

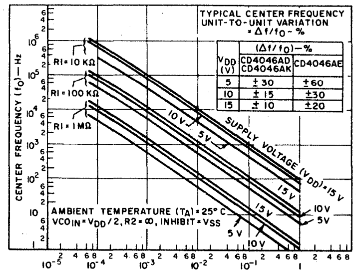


Fig. 9(a)– Typical center frequency vs. C_1 for R_1 = 10 KΩ, 100 KΩ, and 1 MΩ.

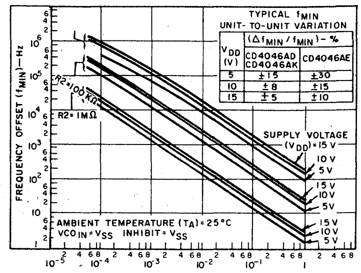


Fig. 9(b)– Typical frequency offset vs. C_1 for R_2 = 10 KΩ, 100 KΩ, and 1 MΩ.

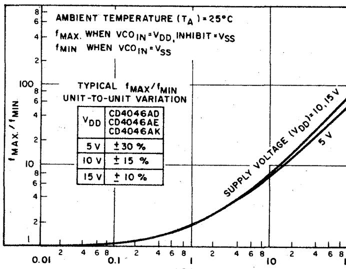
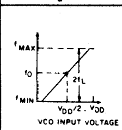
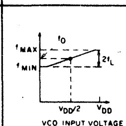
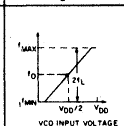
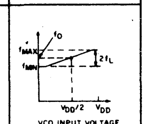
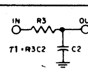
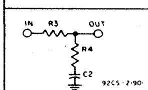


Fig. 9(c)– Typical f_{max}/f_{min} vs. R_2/R_1.

CHARACTERISTICS	USING PHASE COMPARATOR I: VCO WITHOUT OFFSET $R_2 = \infty$	USING PHASE COMPARATOR I: VCO WITH OFFSET	USING PHASE COMPARATOR II: VCO WITHOUT OFFSET $R_2 = \infty$	USING PHASE COMPARATOR II: VCO WITH OFFSET
VCO Frequency				 92CS 20012RI
For No Signal Input	VCO in PLL system will adjust to center frequency, f_o		VCO in PLL system will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2f_L$	$2f_L$ = full VCO frequency range $2f_L = f_{max} - f_{min}$			
Frequency Capture Range, $2f_C$	 $\tau 1 = R3C2$ (1),(2) $2f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau 1}}$		$f_C = f_L$	
Loop Filter Component Selection	 For $2f_C$, see Ref. (2) 92CS-21901			
Phase Angle between Signal and Comparator	90° at center frequency (f_o), approximating 0° and 180° at ends of lock range ($2f_L$)		Always 0° in lock	
Locks on Harmonics of Center Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	
VCO Component Selection	– Given: f_o – Use f_o with Fig.9a to determine R1 and C1	– Given: f_o and f_L – Calculate f_{min} from the equation $f_{min} = f_o - f_L$ – Use f_{min} with Fig.9b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1	– Given: f_{max} – Calculate f_o from the equation $f_o = \frac{f_{max}}{2}$ – Use f_o with Fig.9a to determine R1 and C1	– Given: f_{min} & f_{max} – Use f_{min} with Fig.5b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.9c to determine ratio R2/R1 to obtain R1

For further information, see
(1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York, 1966
(2) G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

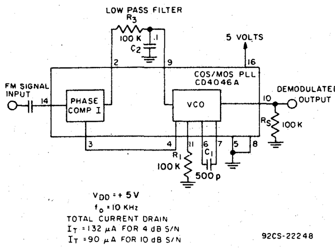


Fig. 10– FM demodulator.

Fig. 11 shows the performance of the FM/demodulator circuit of Fig. 10 at a 4 dB S/N-ratio. The demodulated output is taken off the VCO-input source follower using a resistor Rs (R_S = 100 kΩ).The demodulation gain for this circuit is 250 mV/kHz.

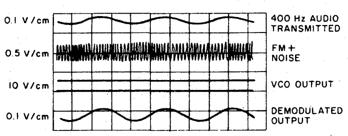


Fig. 11– Voltage waveforms of FM demodulator.

Frequency Synthesizer

The PLL system can function as a frequency-selective frequency multiplier by inserting a frequency divider into the feedback loop between the VCO output and the comparator input. Fig. 12 shows a COS/MOS low-frequency synthesizer with a programmable divider consisting of three decades. N, the frequency-divider modulus, can vary from 3 to 999 in steps of 1. When the PLL system is in lock, the signal and comparator inputs are at the same frequency and

$$f = N \times 1 \text{ kHz}$$

Therefore, the frequency range of this synthesizer is 3 to 999 kHz in 1-kHz increments, which is programmable by the switch position of the Divide-by-N counter.

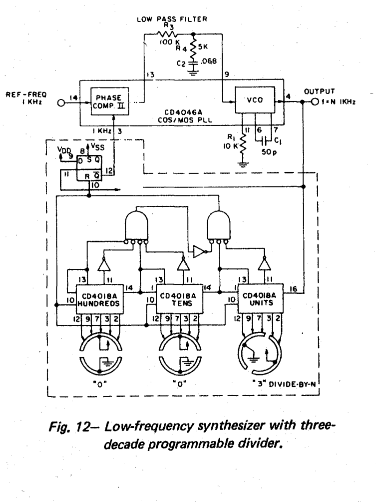


Fig. 12– Low-frequency synthesizer with three-decade programmable divider.

Phase-comparator II is used for this application because it will not lock on harmonics of the signal-input reference frequency (phase-comparator I does lock on harmonics). Since the duty cycle of the output of the Divide-by-N frequency divider is not 50 percent, phase-comparator II lends itself directly to this application.

Using the formulas for phase-comparator II shown in Table IV, the VCO is set up to cover a range of 0 to 1.1 MHz. The low-pass filter for this application is a two-pole, lag-lead filter which enables faster locking for step changes in frequency. Fig. 13 shows the waveforms during switching between output frequencies of 3 and 903 kHz. The figure shows that the transient going towards 3 kHz on the VCO control voltage is overdamped, while the transient to 903 kHz is underdamped. This condition could be improved by changing the value of R_3 in the low-pass filter by means of adjustment of the switch-position hundreds in the Divide-by-N counter.

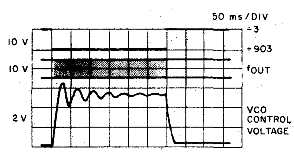


Fig. 13– Frequency-synthesizer waveforms.

Split-Phase Data Synchronization and Decoding

Fig.14 shows another application of COS/MOS PLL, split-phase data synchronization and decoding. A split-phase data signal consists of a series of binary digits that occur at a periodic rate, as shown in waveform A in Fig. 14, The weight of each bit, 0 or 1, is random, but the duration of each bit, and therefore the periodic bit-rate, is essentially constant. To detect and process the incoming signal, it is necessary to have a clock that is synchronous with the data-bit rate. This clock signal must be derived from the incoming data signal. Phase-lock techniques can be utilized to recover the clock and the data. Timing information is contained in the data transitions, which can be positive or negative in direction, but both polarities have the same meaning for timing recovery. The phase of the signal determines the binary bit weight. A binary 0 or 1 is a positive or negative transition, respectively, during a bit interval in split-phase data signals.

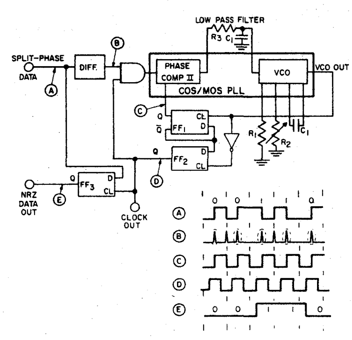


Fig. 14– Split-phase data synchronization and decoding.

As shown in Fig. 14, the split-phase data-input (A) is first differentiated to mark the locations of the data transitions. The differentiated signal, (B), which is twice the bit rate, is gated into the COS/MOS PLL. Phase-comparator II in the PLL is used because of its insensitivity to duty cycle on both the signal and comparator inputs. The VCO output is fed into the clock input of FF1 which divides the VCO frequency by two. During the ON intervals, the PLL tracks the differentiated signal (B); during the OFF intervals the PLL remembers the last frequency present and still provides a clock output. The VCO output is inverted and fed into the clock input of FF2 whose data input is the inverted output of FF1. FF2 provides the necessary phase shift in signal (C) to obtain signal (D), the recovered clock signal from the split-phase data transmission. The output of FF3, (E), is the recovered binary information from the phase information contained in the split-phase data. Initial synchronization of this PLL system is accomplished by a string of alternating 0's and 1's that precede the data transmission.

Phase-Locked-Loop Lock Detection

In some applications that utilize a PLL, it is sometimes necessary to have an output indication of when the PLL is in lock. One of the simplest forms of lock-condition indicator is a binary signal. For example, a 1 or a 0 output from a lock-detection circuit would correspond to a locked or unlocked condition, respectively. This signal could, in turn, activate circuitry utilizing a locked PLL signal. This detection could also be used in frequency-shift-keyed (FSK) data transmissions in which digital information is transmitted by switching the input frequency between either of two discrete input frequencies, one corresponding to a digital 1 and the other to a digital 0.

Fig. 15 shows a lock-detection scheme for the COS/MOS PLL. The signal input is switched between two discrete frequencies of 20 kHz and 10 kHz. The PLL system uses

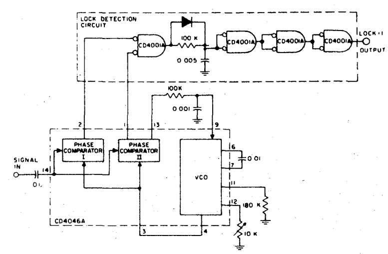


Fig. 15– Lock-detection circuit.

phase-comparator II; the VCO bandwidth is set up for an f_{min} of 9.5 kHz and an f_{max} of 10.5 kHz. Therefore, the PLL locks and unlocks on the 10-kHz and 20-kHz signals, respectively. When the PLL is in lock, the output of phase-comparator I is low except for some very short pulses that result from the inherent phase difference between the signal and comparator inputs; the phase-pulses output (terminal 1) is high except for some very small pulses resulting from the same phase difference. This low condition of phase comparator I is detected by the lock-detection circuit shown in Fig. 15. Fig. 16 shows the performance of this circuit when the input signal is switched between 20 and 10 kHz. It can be seen that after about five input cycles the lock detection signal goes high.

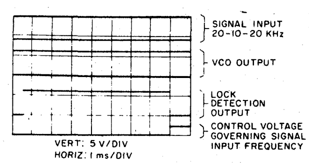


Fig. 16– Lock-detection-circuit waveforms.

ICAN-6230

Using the CD4047A in COS/MOS Timing Applications

by J. Paradise

Many applications exist today for COS/MOS multivibrators– both oscillators and one-shots–in analog and digital circuits. The requirements for these applications vary widely in such parameters as voltage range, temperature stability, power dissipation, drive capability, and external-component cost. No design is optimum for all of the above considerations. However, the RCA-CD4047A Monostable/Astable Multivibrator fulfills the needs of most applications in this timing area. It can function as either an oscillator or one-shot with many additional features, and will meet the power dissipation, stability, and speed requirements of most COS/MOS systems.

This Note compares some simpler types of oscillator circuits with the CD4047A in both theoretical and actual performance, and provides application information on the CD4047A which should prove useful to COS/MOS circuit and system designers.

COS/MOS DISCRETE RC OSCILLATOR

The simplest type of RC-oscillator is shown in Fig. 1. It consists of two inverters (which may be taken from standard

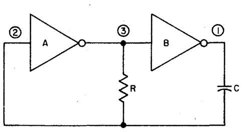


Fig. 1 – Simplest COS/MOS RC oscillator.

RCA COS/MOS parts, i.e., CD4007A, CD4001A, CD4011A, etc.) and a single resistor and capacitor. The operating waveforms for this circuit are shown in Fig. 2.

The circuit operates as follows: depending on the output levels of inverters A and B, at any instant C will be charging or discharging through R. When the waveform at point (2) in the circuit passes through the transfer voltage of inverter A, this inverter will switch and cause inverter B to switch. Subsequently, the waveform at point (2) would be exponentially

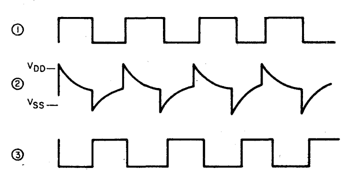


Fig. 2 – RC-oscillator operating waveforms.

increasing or decreasing with discontinuities equal in magnitude to V_{DD} during the instant of switching. However, since point (2) is protected by a standard input-protection circuit common to COS/MOS devices, the waveform is clamped at one diode voltage drop above V_{DD} and below V_{SS}. (Refer to waveforms in Figs. 2 and A1). The calculations for the period of this multivibrator circuit are shown in Appendix A; the final equation for the period T is

$$T = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_D)^2} \qquad (1)$$

where V_{TR} is the switching or transfer point of the inverter, and V_D is the diode forward voltage drop.

Equation (1) shows that the period of the multivibrator, T, is sensitive to changes in V_{DD}, as illustrated by the graph of time period, T, vs transfer voltage as a function of V_{DD} in Fig. 3. In addition to the strong dependence of actual time period on the V_{DD} chosen, the graph also illustrates that, for a given V_{DD}, a full transfer voltage spread of 30 to 70 per cent of V_{DD} (unit-to-unit worst-case variations) yields a change in time period of about 10 per cent from the nominal 50-per-cent transfer-voltage percentage values.

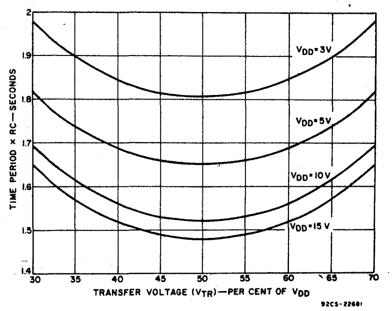


Fig. 3 – Discrete RC-oscillator time period as a function of transfer voltage.

The above analysis is valid only at low frequencies (i.e., less than 50 kHz). As the multivibrator frequency approaches this value, other considerations must be taken into account:

1. The input protection circuit has a V_{DD} diode with a finite resistance and capacitance; the diode will discharge at the rate associated with this small time constant.

2. In the negative direction, there is a diode as well as a series protection resistor (1 to 3 kilohms); the time constant of this diode is even longer than that of the V_{DD} diode.

3. The propagation delay of the inverters used is added to the time period during each charge and discharge cycle. Since the delay is a function of V_{DD}, small changes in V_{DD} at high frequencies will cause the time period to vary.

4. There is a finite output impedance associated with the inverter which is in series with the external timing resistor. Since this output impedance also changes with V_{DD}, at high frequencies where the external resistor becomes small, the multivibrator stability decreases with small variations in V_{DD}.

The negative features of the input protection circuit can be partially compensated for by the addition of a resistor, R_S, in series with the input protection circuit, as shown in Fig. 4. Although the input inverter A is still clamped at one diode drop above V_{DD} or one diode drop below V_{SS}, the waveform at point (4) is allowed to swing well above V_{DD} and below V_{SS}. The larger swing reduces the dependency of transfer-voltage variations upon stability; the variable characteristics of the input protection circuit and their effect upon stability are greatly reduced. An analysis of this circuit is presented in

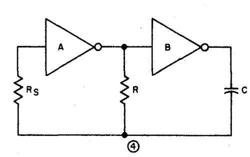


Fig. 4 – RC-oscillator with the addition of R_S.

Appendix B; the equation for the period, T, for this circuit is shown in Eq. 2.

When $K = \frac{R_S}{R}$, T is:

$$T = \left\{ \begin{array}{l} -RC \ln \dfrac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_D)^2} \\ -\dfrac{(K\ \ )}{(K+1)} RC \ln \dfrac{K\,[V_{DD} + V_D]}{K\,[V_{DD} + V_{TR}] + [V_{TR} - V_D]} \\ -\dfrac{(K\ \ )}{(K+1)} RC \ln \dfrac{K\,[V_{DD} + V_D]}{K\,[2\,V_{DD} - V_{TR}] + [V_{DD} - V_{TR} - V_D]} \end{array} \right\} \qquad (2)$$

In this form it is easy to see that when K approaches zero, the circuit and associated waveforms are equivalent to those of Fig. A-1. On the other hand, as K approaches infinity, the variation in period as a function of V_{DD} is reduced to zero. This result is shown in Fig. 5, where period as a function of trans-

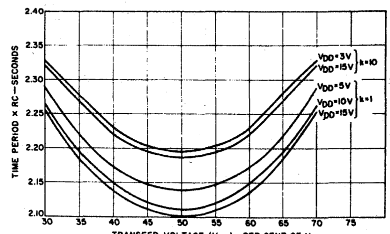


Fig. 5 – Discrete RC-oscillator time period as a function of transfer voltage.

fer voltage is plotted for different value of V_{DD} and K, and Fig. 6, which shows period as a function of K for different values of V_{DD}. Variation in period with transfer voltage is also reduced as K increases. This variation decreases from 10 per cent for K = 0 to about 5 per cent as K gets large.

There are some obvious limitations in the value of R_S that can be used. Besides the disadvantages in this circuit if R is to

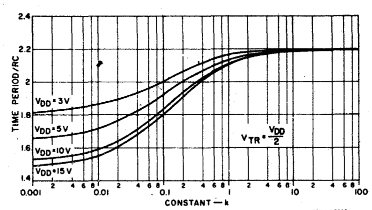


Fig. 6 – Discrete RC-oscillator time period as a function of constant, k.

be made adjustable, the user must be careful with component layout, if R_S is made very large, to take advantage of the improvement in stability. A time constant and phase shift is produced by R_S and stray wiring and breadboard capacitance, see Fig. 7. This shift creates a switching delay in the circuit which changes the time period and, in addition, may cause spurious oscillations and glitches in the multivibrator circuit. A reasonable value for K would be anywhere from 2 to 10, with maximum and minimum values for R_S determined by the above considerations.

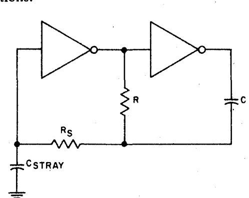


Fig. 7 – RC-oscillator circuit with stray capacitance.

COS/MOS INTEGRATED RC OSCILLATORS

The RCA-CD4047A is an integrated RC oscillator that eliminates most of the disadvantages of the discrete circuits previously discussed. The primary reason for this improved performance is the special input-protection circuit which allows the capacitor charging waveform to swing above V_{DD} and below V_{SS} without the need for an external resistor. This circuit, shown in Fig. 8, has the same time period and stability as the circuit in Fig. 4 for the case where the value of R_S is infinite. However, a resistor is eliminated, as well as the disadvantages of a time constant caused by the resistor.

There are two additional reasons for expected improvement with the CD4047A. First, the transfer-voltage point of the input inverter, A, is tested between 33 and 67 per cent of V_{DD} instead of between 30 and 70 per cent; this narrower test range improves stability by reducing unit-to-unit variations. In addition, large buffers are used for inverters D and E; this practice

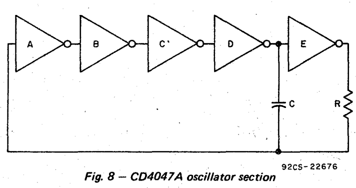


Fig. 8 – CD4047A oscillator section

reduces the effect of changes of device output impedance with period stability. A derivation of period, T, for this circuit is presented in the Appendix C; the final equation for T becomes:

$$T = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2\,V_{DD} - V_{TR})} \quad (3)$$

Figure 9 shows a graph of stability as a function of transfer voltage based on this equation.

The graph of Fig. 9 shows a maximum variation of 5 per cent between minimum (2.197 RC) and maximum (2.307 RC) time periods. A value of 2.25 RC yields a ± 2.5 per-cent variation. Typical values of period variations at high frequencies and temperature extremes are included in the published data for the CD4047A.[1]

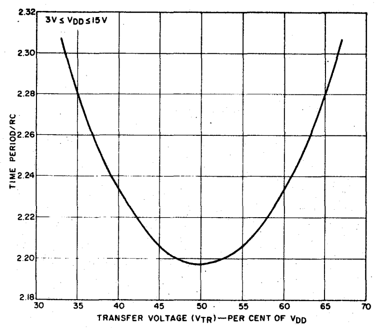


Fig. 9 – CD4047 time period as a function of transfer voltage.

An additional advantage of the CD4047A is a reduction in power dissipation as compared to the discrete multivibrators discussed previously. Inverter A in Fig. 8 is designed with high-impedance components that limit power dissipation during the time that the inverter operates in the middle of its transfer region. Four additional inverters are used to gradually shift from a very-high-impedance inverter at the input to a very-low-impedance driver in series with the external timing resistor. Calculations for power dissipation and a comparison of P_{diss} for the CD4047A and a discrete oscillator are presented in Appendix D; the result is

$$P_{diss} = 2\,CV^2 f \quad (4)$$

This equation specifies the power dissipated in the external components only. At low frequencies, where most of the power will be dissipated in R, power can be minimized by using a small value of C, since the formula shows the power is a function of C and not R.

Additional power is consumed in the CD4047A chip as a function of frequency. Fig. 10 shows curves for theoretical minimum power dissipation, actual CD4047A oscillator-power dissipation, and discrete oscillator-power dissipation as a function of frequency.

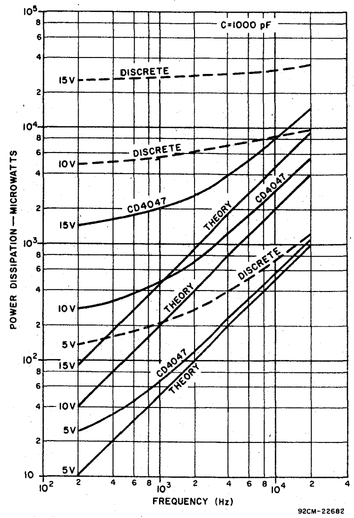


Fig. 10 – Comparison of P_{diss} for discrete oscillator and CD4047 with theory.

CMOS DISCRETE ONE-SHOTS

Fig. 11 illustrates one of several simple monostable circuits which can be employed in non-critical timing circuits.[2] The

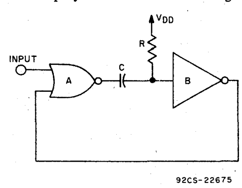


Fig. 11 – COS/MOS monostable circuit.

circuit pulse width is dependent upon the transfer voltage of inverter B as time constant RC charges to V_{DD} from V_{SS}. The pulse width is defined as

$$T = -RC \ln \frac{(V_{DD} - V_{TR})}{(\;V_{DD}\;)} \quad (5)$$

Fig. 12 shows the variation in pulse width as a function of transfer voltage for this device.

There are several alternatives to the circuit shown in Fig. 12.[2] These alternatives have the advantage of greater stability, but at the expense of two time constants required in circuit and, in some cases, the addition of a diode.

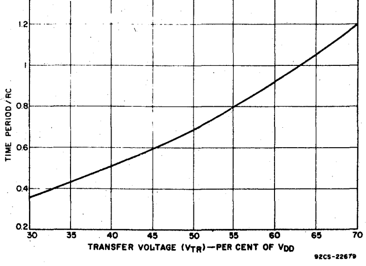


Fig. 12 – Simple one-shot time period as a function of transfer voltage.

COS/MOS INTEGRATED ONE-SHOTS

The CD4047A, when used in the monostable mode, again has several advantages over discrete designs. A high degree of accuracy can be achieved with one time constant, and power dissipation is lower than with discrete designs. Fig. 13 shows that many functions can be achieved with the CD4047A, including leading and trailing-edge triggering, and retriggering.

The pulse width, T_M, is expressed below: its derivation is given in Appendix E.

$$T_M = -RC \ln \frac{(V_{TR})(V_{DD}) - V_{TR})}{(2\,V_{DD})(2\,V_{DD} - V_{TR})} \quad (6)$$

Fig. 14 is a graph of pulse width versus transfer voltage based on the above equation.

The equations for monostable-mode power dissipation are also derived in Appendix E. For a repetitive output on the CD4047A, power dissipation can be expressed by the following equation:

$$P_{diss} = \frac{2.875\,CV_{DD}^2}{T_M} \times (\text{duty cycle}) \quad (7)$$

USING THE CD4047A – SPECIAL CONSIDERATIONS

A number of circuit considerations are explained below which will aid the user of the CD4047A.

A clamping circuit is provided on the chip to reduce the recovery time (tr) that would normally exist in other monostable circuits; see Figs. 15 and 16. Fig. 17 shows a plot of monostable-pulse-width stability as a function of duty cycle for specific R and C external components. Note that there is no appreciable change in pulse width until the duty cycle approaches 100 per cent. A disadvantage to the clamping circuit is that it introduces additional capacitance at the RC common node (Fig. 16), which may be noticeable for short pulse widths in the monostable mode only. Some diffusion capacitance present at the base of the n-p-n transistor is used to quickly charge C to V_{DD} after the one-shot cycle has terminated. This capacitance is multiplied by the beta of the transistor, and is in parallel with the external C during the time interval that the transistor is on ($V_{DD} - V_{BE} < t < V_{BE}$). Thus, when values of C less than 1000 picofarads are used, the actual width will be longer than that predicted by the formula. Fig. 18 is a graph of actual, typical pulse widths as a function of external C used under these conditions. Note that the minimum values of C used in the graph are the smallest that can be used in the CD4047A to assure proper operation of the circuit.

The waveform in Fig. 15 shows that two positive transitions are encountered by the control circuitry in the CD4047A. These transitions are necessary to make the output flip-flop at pin 10 toggle properly to produce the single pulse needed in monostable operation. However, at pin 13, the waveform of Fig. 19 results; the pulse width of the spike is equivalent to the propagation delay of the circuit. This spike will normally prevent the user from using pin 13 in the monostable mode. In the astable mode, however, pin 13 can be used whenever a 50-per-cent duty cycle and higher drive capability are not required. The advantage to the use of pin 13 under these conditions is that the frequency of the waveform at pin 13 is twice that of pin 10 for the same external timing components.

When the CD4047A is used in the retrigger mode, the retrigger input is connected directly to the set input of FF4, as shown in Fig. 13. This connection means that the output at pin 10 will be high during the time that a high level is present on pin 12. Thus, if normal one-shot operation is required at any time that the circuit is in the retrigger mode, the input pulse should be shorter than the expected pulse at the output. Note that in the retrigger mode the output pulse width is not referenced to the last positive-going edge produced at the input because of the asynchronous nature of the circuit. The output actually terminates when two internal-oscillator leading edges have been received by FF4, after the high level present on pin 12 has been removed. The output width variation will then be between one and two time constants referenced to the trailing edge of the input at pin 12, see Fig. 20.

A section on timing-component limitations is presented in the CD4047A data sheet.[1] It should be emphasized that it is desirable to use a small value of capacitance wherever possible.

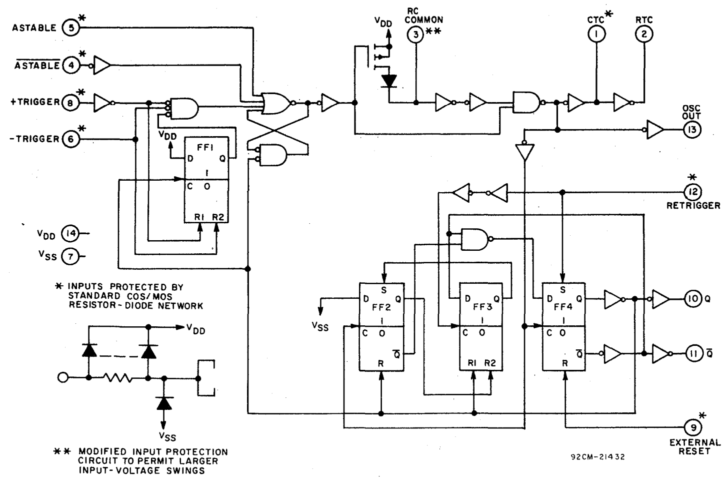


Fig. 13 – CD4047A logic diagram.

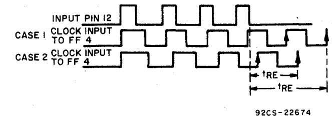


Fig. 20 – CD4047A retrigger-mode waveforms.

The circuit will work well even when the value of R approaches or exceeds 1 megohm. For very low frequencies, where a large value of capacitance is needed, the selection of the capacitor is very important. It must be nonpolarized because there is no reference ground at either of the two pins to which C is connected. The capacitor parallel resistance (i.e., leakage) must also be at least an order of magnitude higher than the external R used. This criterion generally eliminates electrolytic capacitors and those made of materials which could produce greater leakage current than that permitted for proper circuit operation.

Because of the internal circuit construction, there is no guarantee as to what dc level will be present on the output at pin 10 or 11 when power is first turned on. If this condition must be guaranteed, a system-power on pulse input to pin 9 can be made to assure that pin 10 will initially be at a low logic level. The pulse can be generated from one of the circuits shown in Fig. 21.

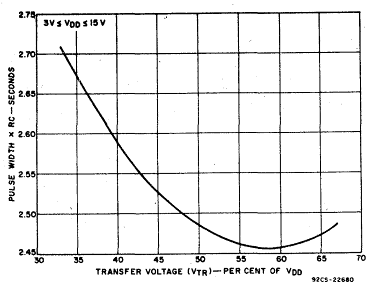


Fig. 14 – CD4047A one-shot pulse width as a function of transfer voltage.

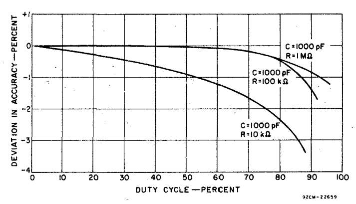


Fig. 17 – CD4047A monostable accuracy as a function of duty cycle.

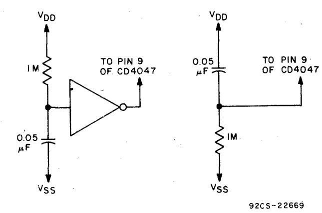


Fig. 21 – CD4047A power-up reset circuits.

Although the CD4047A data sheet calls for a minimum input pulse duration of 200 nanoseconds at 10 volts and 500 nanoseconds at 5 volts, shorter pulses (due to transients, etc.) occur frequently in system applications where the CD4047A is used. Such narrow pulses may not be ignored by the CD4047A, but may instead cause Q to go high permanently or until a reset input occurs. The circuit shown in Fig. 22 eliminates this problem by essentially "lengthening" the trigger pulse by feeding back through R_A and C_A a current pulse when Q goes from 0 to a 1. The particular values shown have been tried and found to work well, even for extremely short input pulses (less than 20 nanoseconds).

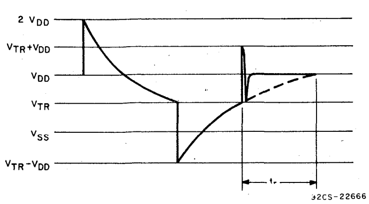


Fig. 15 – CD4047A one-shot RC waveform.

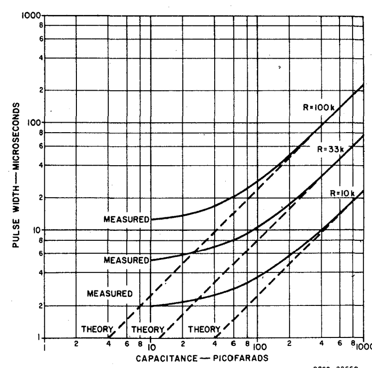


Fig. 18 – CD4047A pulse width as a function of capacitance.

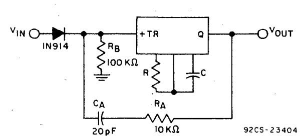


Fig. 22 – Input-pulse stretcher circuit.

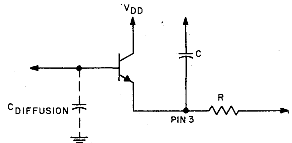


Fig. 16 – CD4047A clamping circuit.

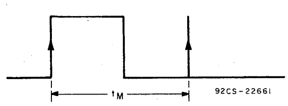


Fig. 19 – CD4047A one-shot output at pin 13.

APPLICATIONS

NOISE DISCRIMINATOR

Fig. 23 illustrates an application of the CD4047A in a noise-discriminator circuit. By adjusting the external time constant, a pulse width narrower than that determined by the time constant will be rejected by the circuit. The output pulse will

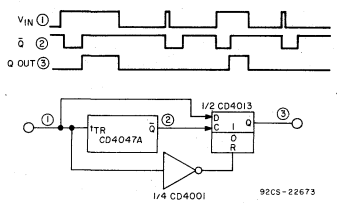


Fig. 23 – Noise-discriminator circuit.

follow the desired input, but the leading edge will be delayed by the selected time constant. Fig. 24 shows typical waveforms with the circuit in operation.

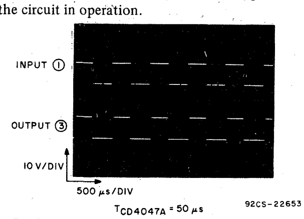


Fig. 24 – Noise-discriminator circuit waveforms.

FREQUENCY DISCRIMINATOR

The CD4047A can be used as a frequency-to-voltage converter, as shown in Fig. 25. A waveform of varying frequency is applied to the +TR input. The one-shot will produce a pulse of constant width for each positive transition on the input. The

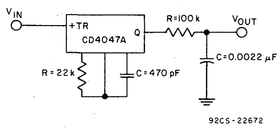


Fig. 25 – Frequency-discriminator circuit.

resultant pulse train is integrated to produce a waveform whose amplitude is proportional to the input frequency. The waveforms of Fig. 26 were taken with the circuit in operation.

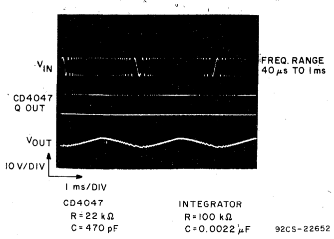


Fig. 26 – Frequency-discriminator-circuit waveforms.

LOW-PASS FILTER

A simple circuit using the CD4047A as a low-pass filter is shown in Fig. 27. The time constant chosen for the multivibrator will determine the upper cutoff frequency for the filter. The circuit essentially compares the input frequency

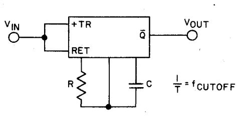


Fig. 27 – Low-pass filter circuit.

with its own reference, and produces an output which follows the input for frequencies less than f_{cutoff}, and a low output for frequencies greater than f_{cutoff}. Figs. 28 and 29 show waveforms with the low-pass filter circuit in operation.

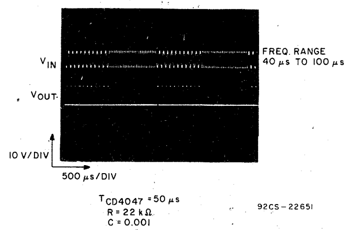


Fig. 28 – Low-pass filter-circuit waveforms.

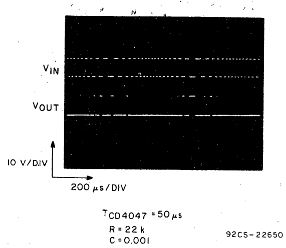


Fig. 29 – Low-pass-circuit waveforms.

BANDPASS FILTER

Two CD4047A low-pass filters can be employed to construct a bandpass filter, as illustrated by the circuit in Fig. 30. The pass band is determined by the time constants of the two filters. If the output of filter No. 2 is delayed by C_1, the CD4013A flip-flop will clock high only when the cutoff frequency of filter No. 2 has been exceeded; this point is illustrated in the timing diagram in Fig. 30. The Q̄ output of the CD4013A is gated with the output of filter No. 1 to produce

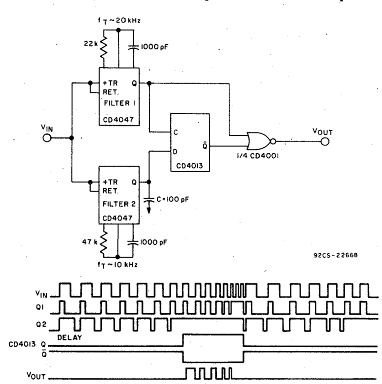


Fig. 30 – Bandpass filter circuit and waveforms.

the desired output. Typical operation of the circuit is shown in Fig. 31, where the input frequency is swept through the pass band.

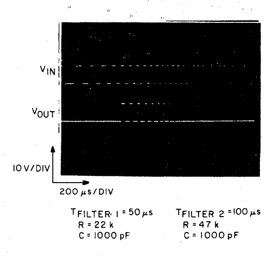


Fig. 31 – Bandpass-filter-circuit waveforms.

ENVELOPE DETECTOR

The CD4047A can be used as an envelope detector by employing it in the retrigger mode, as shown in Fig. 32. The time constant is selected so that the circuit will retrigger at the

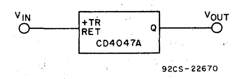


Fig. 32 – Envelope-detector circuit.

frequency of the input pulse burst. A dc level appears at the output for the duration of the input pulse train. Fig. 33 shows waveforms taken with the circuit in operation.

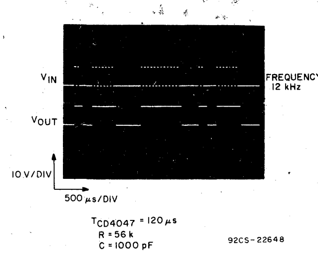


Fig. 33 – Envelope-detector-circuit waveforms.

PULSE GENERATOR

Several CD4047A units can be connected together to produce a general-purpose laboratory pulse generator, as shown in Fig. 34. The circuit shown has variable-frequency and pulse-width control, as well as gating and delayed sync capability. Gating can be controlled from a high- or low-level input. Automatic 50-per-cent duty-cycle capability is included, as normal or inverted output.

CD4047A No. 1 is connected as a gated, astable multivibrator, and, with the RC values shown, can produce overlapping ranges of frequencies from 2 Hz to 1 MHz. For free-running operation, the Gate/Free-Run switch is closed, and the Gate Level switch is placed in the **high-level** position. Standby operation can be achieved with the Gate Level switch in the **low-level** position. When gating, the Gate/Free-Run switch is open, and the Gate Level switch is set to the appropriate position. The gate signal is applied to the Gate In jack.

CD4047A No. 2 is triggered from the gated, astable multivibrator, and produces a narrow sync pulse which can trigger an oscilloscope or generator. The sync pulse is obtained from the Sync Out jack.

If a 50-per-cent duty cycle is desired, the Duty Cycle switch is set in the 50-per-cent position, and the output is obtained from CD4047A No. 1. The Signal Polarity switch determines whether the Q and Q̄ output is used.

CD4047A No. 3 produces a variable, delayed (from 1.5 microseconds to 250 milliseconds) output with respect to the sync pulse when the Delay switch is in the IN position. This one-shot is bypassed when the Delay switch is in the OUT position (the inherent delay is approximately 400 nanoseconds).

CD4047A No. 4 is a monostable multivibrator which receives trigger pulses from CD4047A No. 1 or No. 3. It can produce overlapping ranges of pulse widths from 1.5 microseconds to 200 milliseconds with the values shown.

The signal output is buffered with the CD4041A to allow the pulse generator to drive any required load. The circuit shown has the advantages of being compact, battery-powered, and COS/MOS compatible. In addition, it is capable of being run from the same power supply as the device under test to assure that the input levels are the same as V_{DD} when the power-supply voltage is varied.

MISCELLANEOUS APPLICATIONS

The basic properties of good stability in the astable mode, and stable pulse delay and width control in the monostable mode, make the CD4047A a useful building block in many systems, such as PMOS clock generation, audio tone gener-

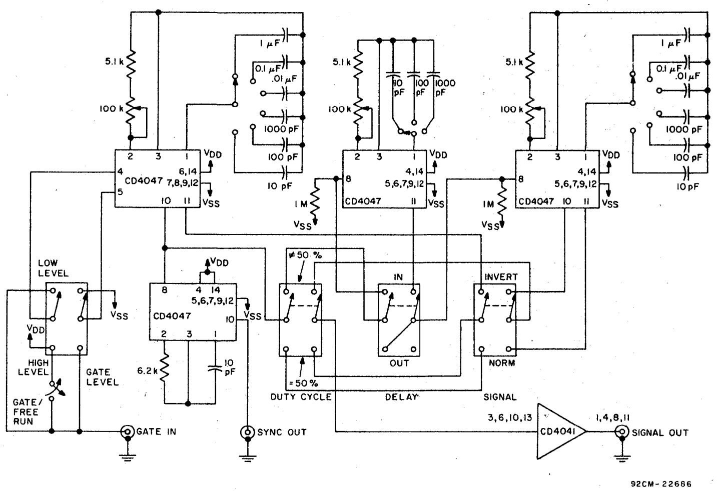


Fig. 34 – Pulse-generator circuit.

ation, semiconductor memory systems, semiconductor memory exercisers, and general-purpose functional-testing systems. This Application Note will serve as a guideline in incorporating the CD4047A in a system design.

REFERENCES

1. **"CD4047A COS/MOS Low-Power Monostable/Astable Multivibrator,"** RCA Data Bulletin, File No. 623
2. **"Astable and Monostable Oscillators Using RCA COS/MOS Digital Integrated Circuits,"** by J. A. Dean and J. P. Rupley, RCA Application Note ICAN-6267

ACKNOWLEDGMENTS

The assistance of R. Vaccarella in the designing of some of the application circuits shown and in obtaining laboratory measurements used in plotting the curves shown in this Note is acknowledged.

Appendix A – Calculation of the Period of an Astable Multivibrator Using a Single RC Time Constant

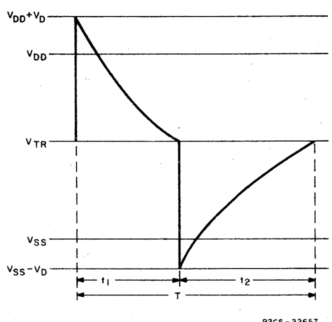


Fig. A-1 – RC oscillator waveform for the circuit of Fig. 1.

In Fig. A-1:

$$t_1: V_{TR} = (V_{DD} + V_D)\, e^{-t_1/RC}$$

$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_D}$$

$$t_2: V_{DD} - V_{TR} = (V_{DD} + V_D)\, e^{-t_2/RC}$$

$$t_2 = RC \ln \frac{V_{DD} - V_{TR}}{V_{DD} + V_D}$$

And the period of an astable multivibrator using a single RC time constant is:

$$T = t_1 + t_2 = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_D)^2}$$

Appendix B – Analysis of Circuit Shown in Fig. 4

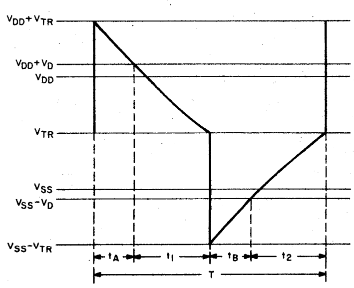


Fig. B-1 – RC waveform for the circuit of Fig. 4.

In Fig. B-1:

$$t_1: V_{TR} = (V_{DD} + V_D)\, e^{-t_1/RC}$$

$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_D}$$

$$t_2: V_{DD} - V_{TR} = (V_{DD} + V_D)\, e^{-t_2/RC}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{V_{DD} + V_D}$$

t_A

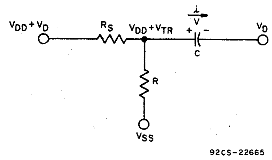


Fig. B-2 – Initial conditions for solving period t_A.

Circuit initial conditions are shown in Fig. B-2. In the figure

$$-C\frac{dv}{dt}=\frac{V+V_{DD}}{R}+\frac{V+V_{DD}-(V_{DD}+V_D)}{R_S} \qquad \text{(B–1)}$$

Eq. (B-1) is solved for V; the final voltage across the capacitor is

$$V=C_1\,e^{-K_1t_A}+\frac{K_2}{K_1} \qquad \text{(B–2)}$$

where $C_1 = V_{TR}$ = initial voltage across capacitor

$$K_1=\frac{R_S+R}{R_SRC}$$

$$K_2=\frac{V_DR-R_SV_{DD}}{R_SRC}$$

By inserting these values into Eq. (B-2) and setting the final voltage across the capacitor, V, to V_D, t_A becomes

$$t_A=-\left[\frac{R_SRC}{R_S+R}\right]\ln\frac{R_S\,[V_{DD}+V_D]}{R_S\,[V_{DD}+V_{TR}]+R\,[V_{TR}-V_D]}$$

t_B

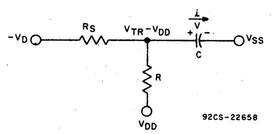


Fig. B-3 – Initial conditions for solving period t_B.

Circuit initial conditions as shown in Fig. B-3. In the figure

$$C\frac{dv}{dt}=\frac{V_{DD}-V}{R}-\frac{V_D+V}{R_S} \qquad \text{(B–3)}$$

Solving Eq. (B-3) for V the final voltage across the capacitor, yields

$$V=C_2\,e^{-K_1t_B}-\frac{K_2}{K_1} \qquad \text{(B–4)}$$

where $C_2 = V_{TR} - V_{DD}$ = initial voltage across capacitor
K_1, K_2 are same values as for above for t_A.

Insertion of these values into Eq. (B-4), with $V = -V_D$ yields

$$t_B=-\left[\frac{R_SRC}{R_S+R}\right]\ln\frac{R_S\,[V_{DD}+V_D]}{R_S\,[2\,V_{DD}-V_{TR}]+R\,[V_{DD}-V_{TR}-V_D]}$$

and $T = t_1 + t_2 + t_A + t_B$.

The equations for t_A, t_B, and T can be simplified by expressing R_S as a multiple of R. Let $K=\frac{R_S}{R}$ and combining the expressions for t_1 and t_2. The resulting expression for T is

$$T=-RC\ln\frac{(V_{TR})(V_{DD}-V_{TR})}{(V_{DD}+V_D)^2}$$

$$-\left(\frac{K}{K+1}\right)RC\ln\frac{K\,[V_{DD}+V_D]}{K\,[V_{DD}+V_{TR}]+[V_{TR}-V_D]}$$

$$-\left(\frac{K}{K+1}\right)RC\ln\frac{K\,[V_{DD}+V_D]}{K\,[2\,V_{DD}-V_{TR}]+[V_{DD}-V_{TR}-V_D]}$$

Appendix C – Calculation for Period of Astable Multivibrator Using Integrated Techniques

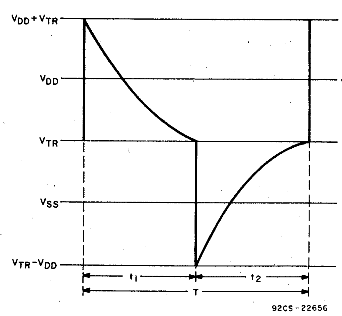


Fig. C-1 – CD4047A RC oscillator waveform.

In Fig. C-1

$$t_1:\ V_{TR}=(V_{DD}+V_{TR})\,e^{-t_1/RC}$$

$$t_1=RC\ln\frac{V_{TR}}{V_{DD}+V_{TR}}$$

$$t_2:\ V_{DD}-V_{TR}=(2\,V_{DD}-V_{TR})e^{-t_2/RC}$$

$$t_2=-RC\ln\frac{V_{DD}-V_{TR}}{2\,V_{DD}-V_{TR}}$$

And the period of the astable multivibrator using integrated techniques is

$$T=-RC\ln\frac{(V_{TR})(V_{DD}-V_{TR})}{(V_{DD}+V_{TR})(2\,V_{DD}-V_{TR})}$$

Appendix D – Power Needed for Charge and Discharge of an External Capacitor During One Cycle

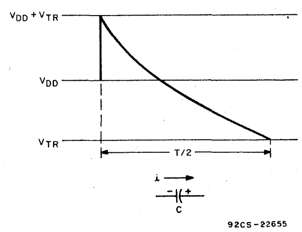


Fig. D-1 – Waveform for calculating power dissipation.

Assume for this calculation that V_{TR} = 50-per-cent V_{DD}, and that T = 2.2 RC. Since charge and discharge cycles are symmetrical, the calculation can be performed by analyzing a discharge cycle only. See Fig. D-1.

$$V = 1.5\, V_{DD}\, e^{-t/RC}$$

$$\frac{dv}{dt} = -\left(\frac{1}{RC}\right)(1.5\, V_{DD})\left(e^{-t/RC}\right)$$

$$P = \frac{1}{(T/2)} \int_o^{T/2} CV \frac{dv}{dt}\, dt$$

$$= \frac{2C}{T} \int_o^{T/2} \left(1.5\, V_{DD}\, e^{-t/RC}\right) \left(\frac{1}{RC}\right)(1.5\, V_{DD})\, e^{-t/RC}\, dt$$

$$= \frac{4.5C}{T} \frac{V_{DD}^2}{RC} \int_o^{T/2} e^{-2t/RC}\, dt$$

$$= -\frac{2.25C\, V_{DD}^2}{T}\, e^{-2t/RC} \Big|_o^{T/2}$$

Substituting T = 2.2 RC

$$P = -\frac{C}{T}(2.25)\, V_{DD}^2\, [e^{-2.2} - 1] = \frac{2.0\, C}{T} V_{DD}^2$$

$$P = 2\, CV^2 f$$

Appendix E – Equations for Pulse Width T_M of CD4047A in Monostable Mode

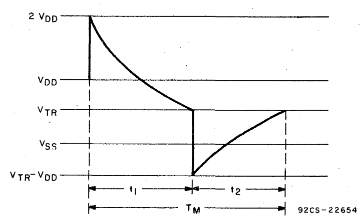


Fig. E-1 – CD4047A RC waveform, monostable mode.

Note that the waveform in Fig. E-1 is not symmetrical because the timing capacitor is initially charged to V_{DD}. In the monostable mode, the circuit goes through one cycle only.

t_1: $V_{TR} = 2\, V_{DD}\, e^{-t_1/RC}$

$$t_1 = -RC \ln \frac{V_{TR}}{2\, V_{DD}}$$

t_2: $V_{DD} - V_{TR} = (2\, V_{DD} - V_{TR})\, e^{-t_2/RC}$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2\, V_{DD} - V_{TR}}$$

And the equation for the pulse width, T_M, of a CD4047A in the monostable mode is:

$$T_M = t_1 + t_2 = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2\, V_{DD})(2\, V_{DD} - V_{TR})}$$

Monostable Power Dissipation

To calculate the power dissipation for the circuit in the monostable mode, refer to Fig. E-1. If it is assumed that V_{TR} = 50-per-cent V_{DD}, Fig. 14 shows that T_M = 2.485 RC. t_2 is the same as in the astable calculation, i.e., t_2 = 1.10 RC and $P_{t2} = CV^2 f$ for V_{TR} = 50-per-cent V_{DD}. Thus, t_1 in the monostable mode = 2.485 RC – 1.10 RC = 1.385 RC.

$$P = \frac{1}{T_M}\left[\int_o^{t_1} CV \frac{dv}{dt}\, dt + \int_{t_1}^{t_2} CV \frac{dv}{dt}\, dv\right]$$

$$= \frac{1}{T_M} \int_o^{t_1} CV \frac{dv}{dt}\, dt + \frac{1}{T_M} CV^2$$

where $V = 2\, V_{DD}\, e^{-t/RC}$ and

$$\frac{dv}{dt} = -\left(\frac{1}{RC}\right)(2\, V_{DD})\, e^{-t/RC}$$

$$P_{t1} = \frac{C}{T_M} \int_o^{t_1} \left(2\, V_{dd}\, e^{-t/RC}\right)\left(\frac{1}{RC}\right)\left(2\, V_{dd}\, e^{-t/RC}\right) dt$$

$$= \frac{C}{T_M} \frac{4\, V_{dd}^2}{RC} \int_o^{t_1} e^{-2t/RC}\, dt$$

$$= -\frac{C}{T_M}\, 2\, V_{dd}^2\, e^{-2t/RC} \Big|_o^{t_1}$$

Substituting t_1 = 1.385 RC

$$P_{t1} = -\frac{C}{T_M}\, 2\, Vdd^2\, [e^{-2.77} - 1] = \frac{1.875\, C\, Vdd^2}{T_M}$$

$$P = P_{t1} + P_{t2} = (1.875 + 1)\frac{C\, Vdd^2}{T_M} = 2.875 \frac{C\, Vdd^2}{T_M}$$

For a repetitive output from the CD4047A

$$P = \frac{2.875\, C\, Vdd^2}{T_M} \text{x duty cycle}$$

COS/MOS Interfacing Simplified

by D. Blandford and A. Bishop

COS/MOS with its wide range of operating supply voltages, low input current, and low power consumption, interfaces easily with many electronic devices. In addition, COS/MOS circuitry can easily be added to a system and can often be operated from the existing power supply. Examples of practical circuits for a wide variety of interfacing situations are given in this Note; design constraints are included in each case.

Note that the CD4000 Series type numbers are followed by a suffix letter, A or B, which specifies the maximum operating voltage for the device: A, 3 to 15 volts; B, 3 to 18 volts. The outputs of all B-type devices are buffered and have the same output drive current and equal source and sink capabilities. Table I shows some characteristics of B-type devices.

Table I — Output Drive Current—B-Type Devices

Output Drive Current	Symbol	V_{DD} Volt	V_O Volt	BD, BK, BF, BH −55°C Min.	+25°C Min.	+125°C Min.	BE −40°C Min.	+25°C Min.	+85°C Min.	+25°C Typ.	Units
Sink	I_{DN}	5	0.4	0.5	0.4	0.3	0.45	0.4	0.36	0.8	mA
		10	0.5	1.1	0.9	0.65	1.0	0.9	0.75	1.8	mA
Source	I_{DP}	5	4.6	−0.5	−0.4	−0.3	−0.45	−0.4	−0.36	−0.8	mA
		5	2.5	−2.0	−1.6	−1.15	−1.8	−1.6	−1.3	−3.2	mA
		10	9.5	−1.1	−0.9	−0.65	−1.0	−0.9	−0.75	−1.8	mA

COS/MOS to TTL

In interfacing TTL with COS/MOS with a common power supply of between 4.5 and 5.5 volts, the guaranteed active-pull-up TTL output voltage of 2.4 volts is lower than the minimum COS/MOS input voltage required to guarantee switching, 3.5 volts, Fig. 1. This difference is overcome by the use of an external resistor, R_X in Fig. 2, which is also the resistor to be used for open-collector-output TTL at a V_{DD} of 5 volts. The minimum value of R_X is fixed by the maximum sink current, e.g., 1.6 milliamperes for 74-series TTL, its maximum value by I_{OH}, the off leakage of the output sink transistor. As shown in Table II, the values of R_X between 1.5 and 4.7 kilohms are suitable for all the TTL families under worst-case conditions. The COS/MOS input impedance is essentially "capacitive", which means that many COS/MOS inputs may be driven by a single TTL output. The actual number depends on the frequency of operation.

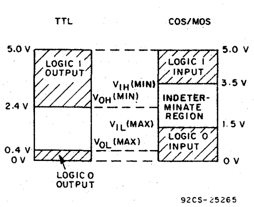


Fig. 1—TTL to COS/MOS voltage levels.

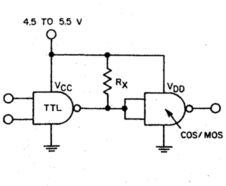


Fig. 2—TTL to COS/MOS interface.

Table II—Values of R_X for TTL—COS/MOS Interface

Characteristic	74	74H	74L	74LS	74S
R_X min. (ohms)	390	270	1.5k	820	270
R_X max. (kilohms)	4.7	4.7	27	12	4.7

In the COS/MOS to TTL interface, Fig. 3, the requirement is to sink sufficient current in the low output state at a maximum output voltage of 0.4 volt. Table III gives the current sinking capability of some CD4000-series devices. Note that all B-type devices have the same standard output drive and are capable of sinking two low-power TTL loads, worst case. For the higher power types of TTL, the CD4049A and CD4050A buffers may be used. Table IV shows the minimum and typical fanout for each TTL family. The buffer takes its power from the 5-volt TTL supply and has an additional advantage in that it can accept input voltage swings of 5 to 15 volts from the preceding COS/MOS system.

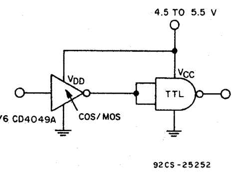


Fig. 3—COS/MOS to TTL interface.

To gain improvements in speed and noise immunity in a system using a COS/MOS supply voltage greater than +5 volts, high-voltage open-collector TTL circuits such as the 7416, 7417 or 7426 may be used, as shown in Fig. 4. The value of the pull-up resistor R_X will depend on the actual value of V_{DD}; at 10 volts, 39 kilohms would be suitable.

COS/MOS to HNIL

The wide operating-voltage range and low power consumption of COS/MOS circuitry enables it to operate from the HNIL power supply. Most CD4000A circuits will drive the HNIL input directly; for example, in Fig. 5, the CD4081B output sinks the required 1.4 milliamperes at an output voltage typically less than 0.5 volt. The HNIL output-voltage levels, 0.8 volt and 10 volts, enable it to interface directly with the COS/MOS input with good noise immunity.

Table IV—Fanout of CD4049A and CD4050A Buffers to TTL

Buffer Fanout	TTL Family 74	74H	74L	74LS	74S
Minimum	1	1	14	7	1
Typical	3	2	28	14	2

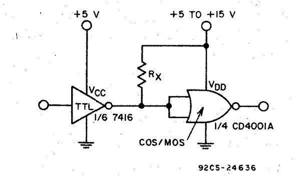


Fig. 4—TTL to COS/MOS at a V_{DD} greater than 5 volts.

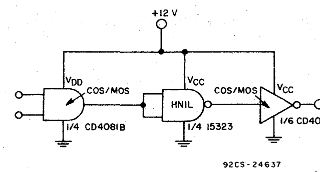


Fig. 5—COS/MOS to HNIL to COS/MOS interface.

COS/MOS to DTL

The COS/MOS to DTL interface requires a buffer, such as the CD4049A shown in Fig. 6, to sink the DTL input current of 1.5 milliamperes at 0.4 volt. Fanout to DTL circuits depends on the sink-current capability of the COS/MOS buffer used. For the CD4049A and CD4050A, typical fanout is 3.

The DTL to COS/MOS interface requires no special consideration because the internal pull-up resistor in DTL circuits and the extremely low input current of COS/MOS circuits ensures a high logic level almost equal to the power-supply voltage.

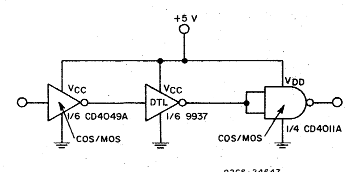


Fig. 6—COS/MOS to DTL to COS/MOS interface.

Table III—Minimum Current-Sinking Capability of COS/MOS Devices

COS/MOS Type	Description	Sink Current (mA at 25°C V_O = 0.4 Volt, V_{DD} = 5 Volt) Ceramic	Plastic
CD4000A	Dual 3-Input NOR Gate Plus Inverter	0.4	0.3
CD4001A	Quad 2-Input NOR Gate	0.4	0.3
CD4002A	Dual 4-Input NOR Gate	0.4	0.3
CD4007A	Dual Complementary Pair Plus Inverter	0.6	0.3
CD4009A/49A	Inverting Hex Buffer	3.0	3.0
CD4010A/50A	Non-Inverting Hex Buffer	3.0	3.0
CD4011A	Quad 2-Input NAND Gate	0.2	0.1
CD4012A	Dual 4-Input NAND Gate	0.1	0.05
CD4041A	Quad True/Complement Buffer	0.4	0.2
CD4031A	64-Stage Static Shift Register	1.3	1.3
CD4048A	Expandable 8-Input Gate	1.6	1.6
CD4XXXB	Any B-Type Device Output	0.4	0.4

COS/MOS to 10k ECL

COS/MOS and 10k ECL are not normally interfaced, but they can be readily by using the 10124 and 10125 devices which are intended for conversion between ECL and TTL. This interface requires that the COS/MOS device be operated at a 5-volt V_{DD}, as shown in Fig. 7. Where greater speed is required of the COS/MOS system, it can be operated with V_{DD} at the ECL ground and V_{SS} at −12 volts. In the latter case, a 1N914 diode clamps the COS/MOS output to V_{EE} as shown in Fig. 8. At supply voltages greater than 6 volts, a COS/MOS buffer should not be used, as over-dissipation will occur in the buffer.

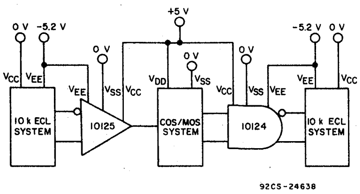


Fig. 7–10k ECL to COS/MOS and COS/MOS to 10k-ECL interface.

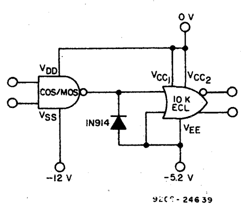


Fig. 8–COS/MOS at 12 volts to 10k-ECL interface.

COS/MOS to NMOS

The increasing use of n-channel MOS memories means that interfaces between COS/MOS and NMOS are now common. In a system of 1k memories, such as the type 2102, which employ peripheral COS/MOS circuitry for address, read/write, chip select and data handling, the COS/MOS circuitry can be supplied from the 5-volt power supply of the memory. Inputs to the memory are then COS/MOS compatible, and direct interface is permitted. The data output requires only a single pull-up resistor, R_X, as shown in Fig. 9, to ensure an acceptable high-state output voltage.

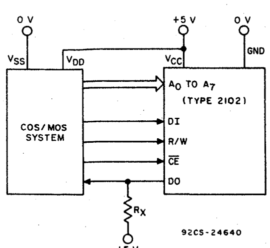


Fig. 9–Direct interface between COS/MOS and a 1k memory, type 2102.

A 4k-bit, dynamic, n-channel RAM, such as the 2107A, has +12-volt and −5-volt supplies as well as the +5-volt V_{CC} supply, as shown in Fig. 10. The COS/MOS peripheral circuitry in this system is probably best operated from the +12-volt supply, ensuring good speed characteristics and noise immunity. The 5-volt input signals to the memory are provided by CD4050A buffers powered by the 5-volt V_{CC} supply. The 12-volt-swing chip-enable signal is directly compatible with the 12-volt COS/MOS system. The data output uses a single transistor to generate the required 12-volt logic swing; memories added to provide an increase in word capacity are wire-OR'ed at the data output pin of the memory.

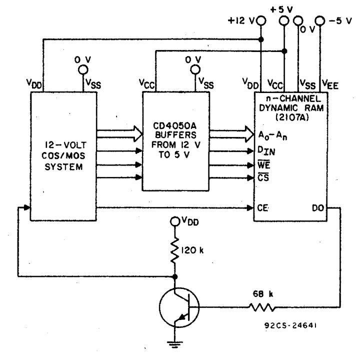


Fig. 10–COS/MOS to n-channel dynamic-RAM interface.

COS/MOS to PMOS

Silicon-gate PMOS static shift registers operating from +5-volt and −12-volt supplies are directly compatible with a COS/MOS system operating from the +5-volt supply with V_{SS} at zero volts. The only additional component required is a clamp diode to V_{SS} on the data output, as shown in Fig. 11, because the unloaded PMOS output voltage will go negative in the low output state.

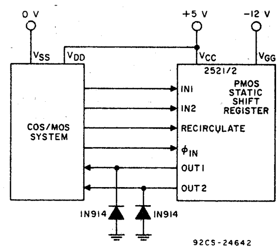


Fig. 11–COS/MOS to PMOS static-shift-register interface.

COS/MOS to Industrial and Power-Control Circuits

Industrial control systems employ greater logic swings than IC logic systems, such as COS/MOS, to achieve high noise immunity and to enable them to operate from readily available high-voltage supplies and to interface with electromechanical equipment.

Fig. 12 shows a simple, resistive-divider circuit used to interface a system with a 24-volt logic swing to COS/MOS; the circuit could readily be modified for even higher voltage swings. The capacitor filter enhances the excellent noise

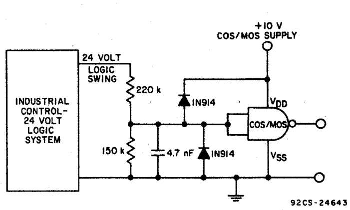


Fig. 12–Industrial control to COS/MOS interface.

immunity of the COS/MOS logic, and the two clamp diodes ensure that the input signal voltage is between V_{DD} and V_{SS}. An alternative circuit using a zener diode is shown in Fig. 13.

A single-transistor level-converter interfaces a COS/MOS device to an industrial control system, as shown in Fig. 14. The transistor is driven directly from the COS/MOS device output (Fig. 23 describes the method of calculating the values of the resistors needed in Fig. 14).

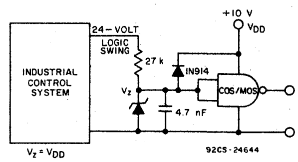


Fig. 13–Zener diode industrial control interface.

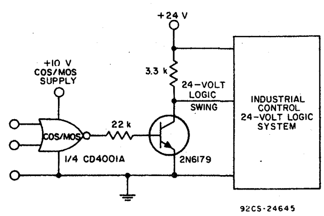


Fig. 14–COS/MOS to industrial-control interface.

The slow pulse edges typically found in an industrial control system can be speeded up in the COS/MOS system by a Schmitt-trigger circuit, the CD4093B, Fig. 15(a). At a V_{DD} of 5 volts, V_H is typically 0.6 volt, Fig. 15(b).

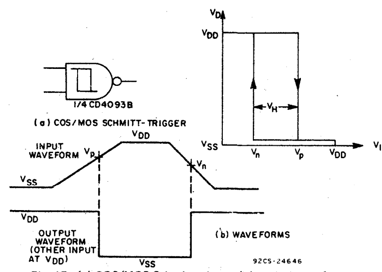


Fig. 15–(a) COS/MOS Schmitt-trigger, (b) typical waveforms for Schmitt-trigger.

A high-power coil, such as the solenoid of a printer hammer, which requires about 1 ampere at 70 volts, may be driven from a COS/MOS system by using a Darlington transistor as shown in Fig. 16. A typical value of V_{BE} for a type 2N6385 transistor is 1.5 volts at a collector current of 1 ampere and a minimum gain of 1000, so that the output source transistor of the CD4073B has to supply 1.5 milliamperes. The value of resistor R is chosen so that V_{DS} is sufficient to guarantee this output current. Suitable values of R for use with a B-type device are given in Fig. 16 for a V_{DD} of 5, 10, and 15 volts.

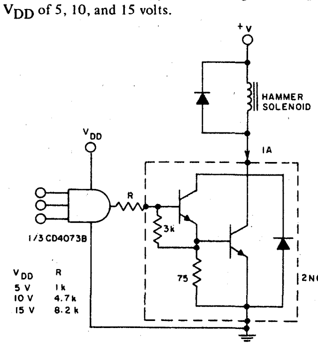


Fig. 16–COS/MOS system driving a printer-hammer solenoid with the aid of a Darlington transistor.

Power-control SCR's and triacs may also be driven directly by COS/MOS outputs. A sensitive-gate SCR, such as the 106B1, may be controlled directly by a COS/MOS gate, such as the CD4069B, and thus be able to control directly 2.5 amperes at reverse voltages up to 600 volts, as shown in Fig. 17.

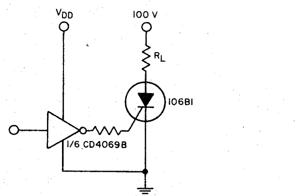


Fig. 17—COS/MOS directly driving a sensitive-gate SCR.

SCR's and triacs with gate currents in the milliampere region may be controlled by a buffer, such as the CD4049A. This buffer could, in turn, be controlled by a COS/MOS system or, as in Fig. 18, by an opto-coupler to provide greater isolation.

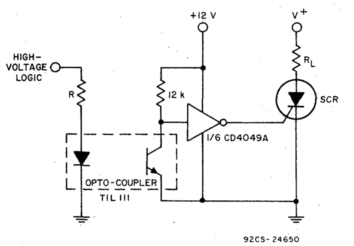


Fig. 18—High-voltage logic to COS/MOS driving an SCR.

In cases where a single-gate output source or sink current proves insufficient, it is possible to parallel the inputs and outputs of gates on the same chip, as in Fig. 19. Gates not on the same chip and buffer circuits should not be operated in parallel as over-dissipation may result.

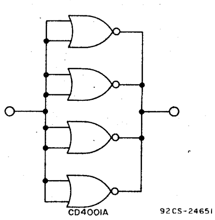


Fig. 19—Paralleling inputs and outputs.

Interfacing Op-Amps to COS/MOS

COS/MOS circuits may be connected directly to the output of an op-amp operating between the normal ±15-volt supply rails, as in Fig. 20, provided clamp diodes to V_{DD} and V_{SS} are used to ensure that the COS/MOS input voltage does not go outside the range V_{SS} to V_{DD}. Resistor R3 limits the op-amp output current should the op-amp output voltage tend toward the negative rail.

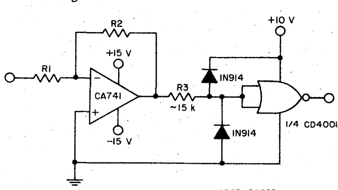


Fig. 20—Split-rail op-amp to COS/MOS interface.

Fig. 21 shows a CA741-type op-amp operated between V_{DD} and V_{SS} with a resistive divider on the non-inverting op-amp input.

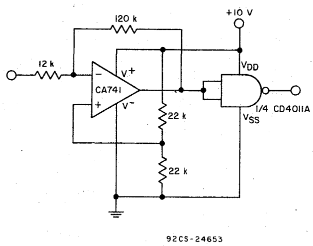


Fig. 21—Interface of op-amp and COS/MOS with common supply rail.

COS/MOS Driving Displays

Digital systems now employ a great variety of digital displays, so that their interface to COS/MOS is a common requirement.

COS/MOS TO LED'S

LED's may be driven directly from a COS/MOS buffer, such as the CD4050A shown in Fig. 22, at a drive current of 15 milliamperes if a power supply of approximately 10 volts is available.

Seven-segment LED displays connected in either common anode or common cathode configurations may be driven at supply voltages as low as +5 volts by the seven-transistor

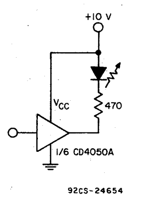
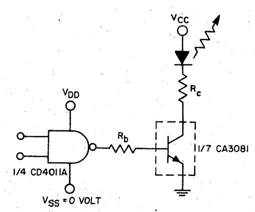


Fig. 22—COS/MOS buffer driving an LED.

arrays CA3081 and CA3082. Fig. 23 shows one of the seven transistors of the CA3081 with an LED load. The figure also shows the method of calculating R_b and R_c. The base drive current available depends on the CD4000A Series device used and the values of V_{DD} and V_{DS}. As shown in Fig. 24, the base drive current increases with both V_{DD} and V_{DS}. Fig. 25 shows one of the seven transistors of the CA3082 driving a common-cathode LED. The method of calculating the value of emitter resistor R_e is also shown in Fig. 25.



$$R_b \le \frac{V_{DD(MIN)} - V_{DS(MAX)} - V_{BE(MAX)}}{I_C\,(MAX)/\beta(MIN)}$$

$$R_c = \frac{V_{CC} - V_{LED} - V_{CE(SAT)}}{I_{LED}}$$

92CS-24655

Fig. 23—COS/MOS driving a transistor that has an LED load.

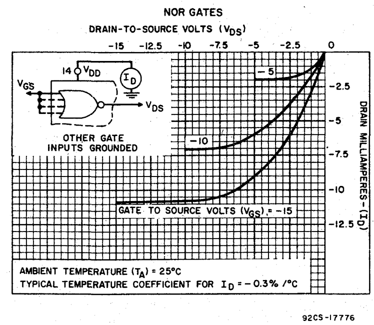
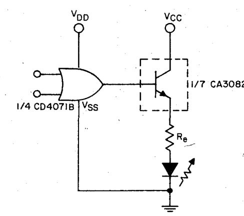


Fig. 24—CD4001A—typical p-channel drain characteristics.



$$R_e = \frac{V_{DD} - V_{DS} - V_{BE} - V_{LED}}{I_{LED}}$$

92CS-24656

Fig. 25—COS/MOS driving a transistor with a common-cathode-connected LED load.

COS/MOS TO LCD

Seven-segment liquid-crystal displays may be driven directly by COS/MOS circuits CD4054A, CD4055A or CD4056A, as shown in Fig. 26. These circuits contain the internal level-shifting circuitry needed to convert the typically 5-volt input logic-level swing to the 30-volt peak ac signal required to drive the dynamic-scattering LCD.

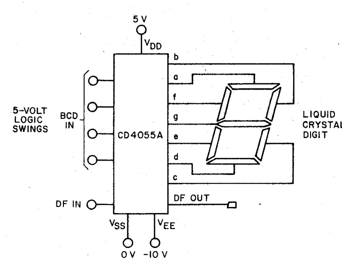


Fig. 26—Using the CD4055A to drive a liquid crystal.

COS/MOS TO GAS-DISCHARGE DISPLAY

The popular seven-segment gas-discharge display requires a cathode drive current that varies from segment to segment. Manufacturers supply drivers which are COS/MOS compatible at their inputs so that they can interface a COS/MOS system to the gas-discharge display without additional circuitry.

REFERENCE

1. "COS/MOS Digital Integrated Circuits", RCA DATABOOK Series SSD-203B, 1975.

ICAN-6346

Applications of the RCA-CD4093B COS/MOS Schmitt Trigger

by D. J. Blandford

This Note describes the characteristics and some typical applications of the CD4093B COS/MOS quad two-input NAND Schmitt Trigger. The CD4093B may be used in all applications in which the logical NAND function is required and, in addition, in a whole range of timing, waveshaping, and interfacing applications in which the Schmitt Trigger action on the inputs is utilized.

CHARACTERISTICS

The CD4093B consists of four Schmitt triggers in a fourteen-pin package. Each of the four devices is a two-input NAND gate with Schmitt action on each input, yielding a typical hysteresis voltage of 2.0 volts with a 10-volt supply without the need for any external components. In addition, the CD4093B is compatible, pin for pin, with the popular CD4011A quad NAND gate, has the balanced and standardized output drive of the 18-volt COS/MOS "B" series types, and has low propagation delay and very low power dissipation. Table I summarizes these characteristics.

If now the input voltage is reduced, the output stays low (V_{SS}) until Vn is reached. At this point the output goes high (V_{DD}) and remains high as the input voltage is reduced to zero (V_{SS}). The hysteresis voltage is the difference between V_p and Vn and is typically 0.6 volt for a 5-volt V_{DD} and 2.0 volts for a 10-volt V_{DD}.

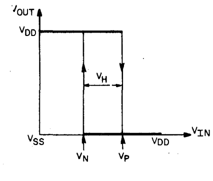


Fig.2 – Transfer characteristic of the CD4093B.

TABLE I

Static and Dynamic Electrical Characteristics at 25°C

CHARACTERISTIC	SYMBOL	VO VOLTS	VDD VOLTS	TYPICAL VALUES	UNITS
QUIESCENT DEVICE CURRENT	I_L		5	0.001	µA
			10	0.001	µA
OUTPUT VOLTAGE LOW LEVEL	V_{OL}		5	0	V
			10	0	V
HIGH LEVEL	V_{OH}		5	5	V
			10	10	V
NOISE IMMUNITY	V_{NL}	5	5	2.6	V
		10	10	5.2	V
	V_{NH}	0	5	3.0	V
		0	10	6.5	V
OUTPUT DRIVE CURRENT SINK	I_{DN}	0.4	5	0.8	mA
		0.5	10	1.8	mA
SOURCE	I_{DP}	4.6	5	−0.8	mA
		2.5	5	−1.8	mA
		9.5	10	−1.8	mA
POSITIVE THRESHOLD VOLTAGE	V_p		5	2.6	V
			10	5.2	V
NEGATIVE THRESHOLD VOLTAGE	V_n		5	2.0	V
			10	3.5	V
HYSTERESIS VOLTAGE	V_h		5	0.6	V
			10	1.7	V
PROPAGATION DELAY TIME	t_{PHL},		5	190	ns
C_L = 50 pF	t_{PLH}		10	100	ns
TRANSITION TIME	t_{TLH},		5	100	ns
C_L = 50 pF	t_{THL}		10	50	ns

Fig.1 shows the functional diagram of the Schmitt trigger; note that each input has the standard COS/MOS input protection network and that each output is double buffered.

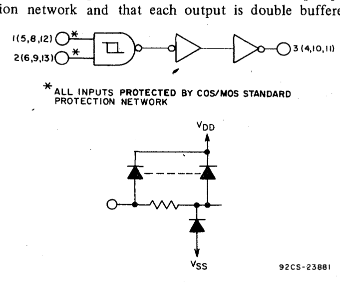


Fig.1 – Functional diagram of the CD4093B, COS/MOS Schmitt trigger. One of four Schmitt triggers is shown.

Fig.2 shows the transfer characteristic of the Schmitt trigger. The general shape of this characteristic is the same for all values of V_{DD}, but the relative values of V_p,Vn and V_H change with V_{DD} as shown in the data sheet. As the input voltage is increased from zero (V_{SS}), the output remains high (V_{DD}) until V_p is reached. At this point the output goes low (V_{SS}) and remains low as the input voltage is raised to V_{DD}.

Fig.3 shows a graph of the typical hysteresis voltage V_H as a function of supply voltage V_{DD}.

Fig.4 shows the input/output characteristics of the CD-4093B; the output characteristic shown is the same for any COS/MOS output, including the Schmitt trigger. The input characteristic is unique to the Schmitt trigger and shows that, when driven by another COS/MOS device, the Schmitt trigger has more than 50-percent noise immunity in each state.

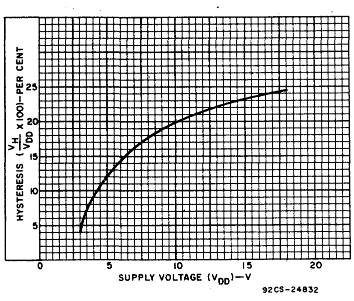


Fig.3 – Typical percent hysteresis vs supply voltage.

Figs.5 and 6 show measurements of voltage and energy noise immunity for the Schmitt trigger. Fig.5 shows, for example, that for a V_{DD} of 5 volts, the noise immunity in each

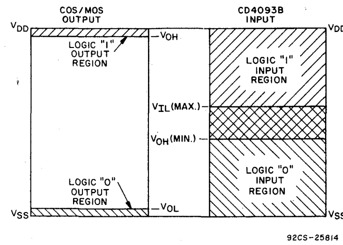


Fig.4 – Input and output characteristics.

state exceeds the supply voltage (5 volts) for pulses shorter than 200 nanoseconds. The energy noise immunity plotted in Fig.6 against pulse width is the product of noise-pulse voltage, noise-pulse time, and the appropriate value of the output drive current for the device under test. The units of energy are nanojoules (10^{-9} Joule). At each value of the supply voltage the curve has a minimum value. Inspection of Fig.6 shows that the value of the minimum energy noise immunity increases with increasing V_{DD}, and occurs at a lower value of noise-pulse width.

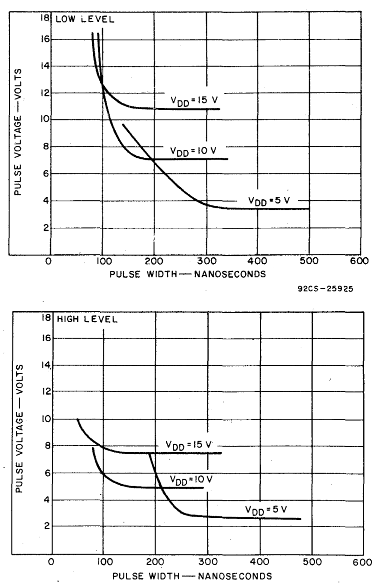


Fig.5 – Voltage noise immunity of the CD4093B.

Another important property of the Schmitt trigger is illustrated in Fig.7, which compares the supply current taken by the CD4093B with that of the CD4011A, with a long rise- and fall-time input. The power dissipated by the Schmitt trigger is clearly much less than that dissipated by the quad NAND gate, so that the Schmitt trigger should be used in applications in which slow input edges are anticipated.

APPLICATIONS

The application of the CD4093B COS/MOS Schmitt trigger in situations which require the logical NAND function and in timing, waveshaping, and interfacing applications in which the Schmitt trigger action on the inputs is utilized are discussed below.

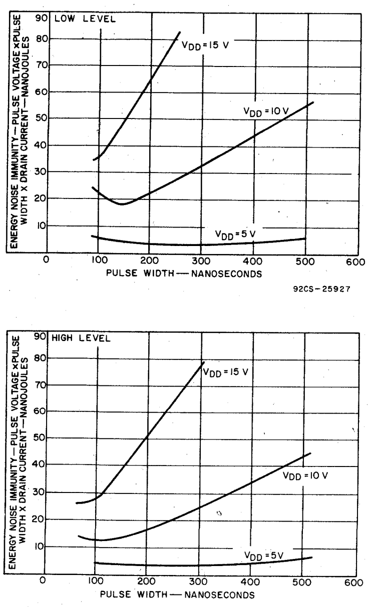
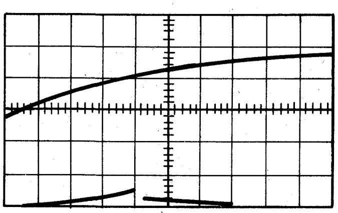
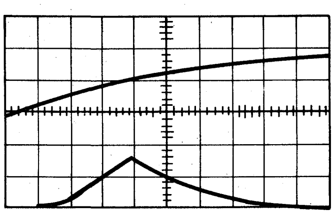


Fig.6 – Energy noise immunity of the CD4093B.



(a) CD4093BE:
Top vertical – 5V/Division
Lower vertical – 2mA/Division
Horizontal – 0.2/Division



(b) CD4011AE:
Top vertical – 5V/Division
Lower vertical – 2mA/Division
Horizontal – 200ms/Division

92CS-26636

Fig.7 – Power consumption with slow input edge; a comparison of the CD4093B with the CD4011A.

Waveshaping

Sine Wave to Square-Wave Converter – Fig.8 shows a typical application of the Schmitt trigger, the sine-wave to square-wave converter. The sine input is ac coupled by capacitor

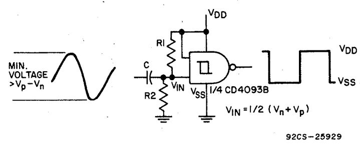
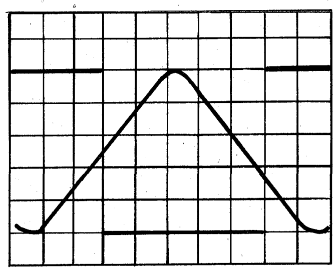


Fig.8 – Sine-wave to square-wave converter.

C; R_1 and R_2 bias the input midway between Vn and V_p, the input threshold voltages, to provide a square wave at the output.

Slow Edges – Slow edges are a common phenomenon in digital systems; for example, at the output from a transducer, at the end of a long line, or an output with large capacitive load, or on the output of a filter. The Schmitt trigger is particularly useful in generating a waveform with fast edges in these applications, see Fig.9.



CD4093BE:
2V/Division
2ms/Division

92CS-26635

Fig.9 – Sharpening up a slow edge.

With an input edge time of 1 second and an output transition time of 100 nanoseconds, the improvement in edge time is a factor of 10^7. With longer input edge times the improvement is even greater.

Timing – In general, timing circuits use external resistors and capacitors to provide time constants. The advantage of the CD4093B COS/MOS Schmitt trigger in these applications is that the very high input impedance permits the designer to use high values of timing resistance. Therefore, long delay times may be produced with moderate values of capacitance, and small, low-cost capacitors may be used for short and medium time delays.

Edge Delays – In the circuit of Fig.10, the output falling edge is delayed with respect to the input leading edge by a time td_+ given by:

$$td_+ = RC \ln \frac{V_{DD}}{V_{DD} - V_p}$$

When the input goes high (V_{DD}) the capacitor charges up towards V_{DD} through R. When input B reaches Vp, the output goes low (V_{SS}). As soon as input A goes low, the output goes high.

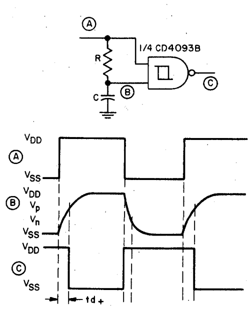


Fig.10 – Delay on leading edge.

By connecting one input to V_{DD}, as in Fig.11, both edges are delayed, because now, when input A goes low, output C remains low until capacitor C discharges to Vn. At this time, the output goes high. td_- is given by:

$$td_- = RC \ln \frac{V_{DD}}{V_n}$$

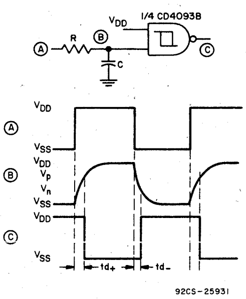


Fig.11 – Delayed pulse.

Both edges may be separately delayed by connecting different RC timing components to each input, as in Fig.12. Now td_+ and td_- are given by:

$$td_+ = R_2C_2 \ln \frac{V_{DD}}{V_{DD} - V_p}$$

$$td_- = R_1 C_1 \ln \frac{V_{DD}}{V_n}$$

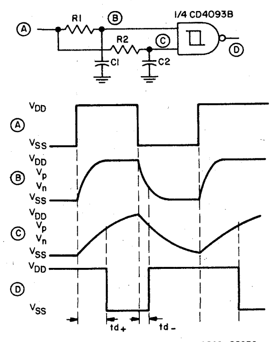


Fig.12 – Separate delay to each edge.

Edge Detector – Fig.13 shows a circuit that provides a short negative-going output pulse for every positive-going edge at the input. The input waveform is coupled to the input by capacitor C; the pulse length depends, as before, on R and C. If a negative going edge detector is required, the circuit of Fig.14 should be used.

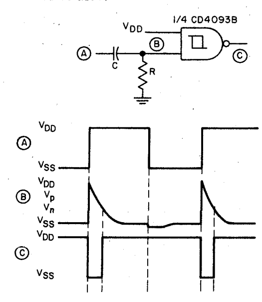


Fig.13 – Rising-edge detector.

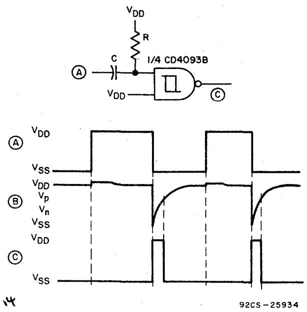


Fig.14 – Falling-edge detector.

Power-On Reset

A reset pulse is often required at power-on in a digital logic system. This type of reset pulse is ideally provided by the circuit of Fig.15(a). Because of the high input impedance of the Schmitt trigger, long reset pulse times may be achieved without the excess dissipation that results when both output devices are on simultaneously, as in an ordinary gate device, Fig.15(b).

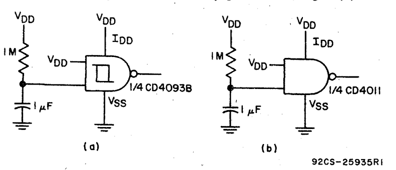


Fig.15 – Reset circuit; a comparison of the CD4093B with the CD4011.

Astable Oscillators

A range of astable oscillators may be easily constructed by using the CD4093B. Fig.16 shows the basic circuit and its associated waveforms. Before power is applied, input and output are at ground potential and capacitor C is discharged. On power-on, the output goes high (V_{DD}) and C charges through R until Vp is reached; the output then goes low (V_{SS}). C is now discharged through R until Vn is reached. The output then goes high and charges C towards Vp through R. Thus input A alternately swings between Vp and Vn as the output goes high and low. One important advantage of this circuit is that the oscillator is self-starting at power-on.

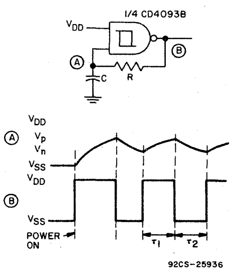


Fig.16 – Astable multivibrator.

The oscillator period is given by:

$$\tau = \tau_1 + \tau_2$$

where

$$\tau_1 = RC \ln \frac{V_{DD} - Vn}{V_{DD} - Vp}$$

and

$$\tau_2 = RC \ln \frac{Vp}{Vn}$$

In general $\tau_1 \neq \tau_2$, so that to get a 1:1 mark-to-space ratio the circuit of Fig.17(a) should be used. When the output is low in the circuit of Fig.17, C is discharged through R_1 in parallel with R_2, which shortens τ_2. If R_2 is much smaller than R_1, short, negative-going pulses are produced, as in Fig.17(b).

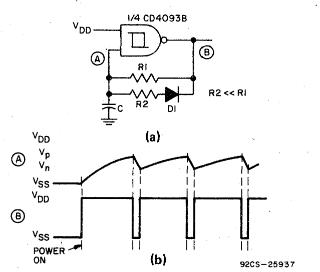


Fig.17 – Astable oscillator with controlled mark-to-space ratio.

In the circuit of Fig.18 the oscillator is gated by signal C on the second input of the CD4093B. The oscillator output is high while the gating signal is low; the oscillator then oscillates with the period τ, given above, while the gating signal is high.

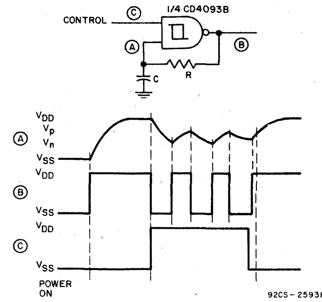
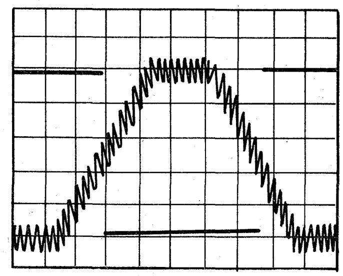


Fig.18 – Gated astable oscillator.

Interfacing

The noise immunity of the COS/MOS NAND Schmitt trigger is very high, typically greater than 50 percent of V_{DD} in each state, as shown in Fig.4. Therefore, it is ideally suited to circuitry that requires a very high noise immunity. Because of the hysteresis built into the Schmitt trigger, it can tolerate noise on a slow input edge without false switching at the output, as shown in Fig.19. This noise performance permits the construction of an ideal interface from an industrial environment to a COS/MOS logic system, as shown in Fig.20. The CD4093B will function correctly under the most severe conditions of input overvoltage and in spite of noise spikes of up to hundreds of volts. The input is kept between V_{SS} and V_{DD} by D_1 and D_2 with R_1, typically 220 kilohms, as a current-limiting resistor. Resistor R_2 ties the logic input to V_{SS} should the interface input be open-circuited by the removal of a PC board from a system, for example. Capacitor C_1, with R_1, acts as a filter and enhances the noise-rejection properties of the interface.



2V/Division
2ms/Division
92CS-26637

Fig.19 – Rejection of noise on slow input edge.

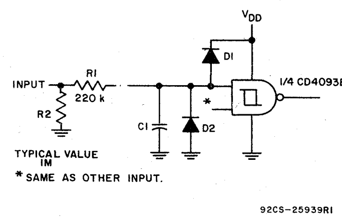


Fig.20 – Industrial-environment to COS/MOS interface.

Astable and Monostable Oscillators Using RCA COS/MOS Digital Integrated Circuits

by
D. V. DiMassimo &
A. R. Maslowski

CIRCUIT TECHNIQUES

COS/MOS integrated logic circuits are being widely used in digital and other applications because of their high noise immunity, extremely low power dissipation, and tolerance to wide variations in power-supply voltages and operating temperatures. In addition, because their high input impedance makes it possible to obtain large time constants without the use of large capacitors, COS/MOS gates can provide cost and size reductions in multivibrator circuits.[1]

This Note describes several techniques that may be used to compensate for the normal threshold variation of MOS devices in the design of stable multivibrator circuits operating at frequencies up to 1 MHz. The circuits shown can be formed by the use of COS/MOS inverters or COS/MOS NAND or NOR gates connected in an inverter configuration. NAND and NOR gates perform the inverter function when all of the gate inputs are tied together. This Note also describes various applications for COS/MOS multivibrator circuits: voltage-controlled oscillators, voltage-controlled pulse-width circuits, phase-locked voltage-controlled oscillators, frequency multipliers, and modulator/demodulators (envelope detectors).

Astable Circuits

The circuits shown in Fig. 1 are those of astable multivibrators that use two COS/MOS inverters (which may be taken from standard RCA COS/MOS parts such as the CD4069B, CD4007A, CD4001, or CD4011). Fig. 2 shows the related waveforms. This simple circuit requires only two resistors and one capacitor and operates in the following manner. Resistor R_S, connected in series with the input of the first inverter, limits the current through the input protection circuit, Fig. 3. In operation, the input to the first inverter is clamped at one diode drop above V_{DD} or one diode drop below V_{SS}. Depending on the output levels of the two inverters, at any instant C will be either charging or discharging through R. When the voltage at point 2 in the circuit passes through the transfer voltage level of the first inverter, this inverter switches and causes the second inverter to switch. The voltage at this point

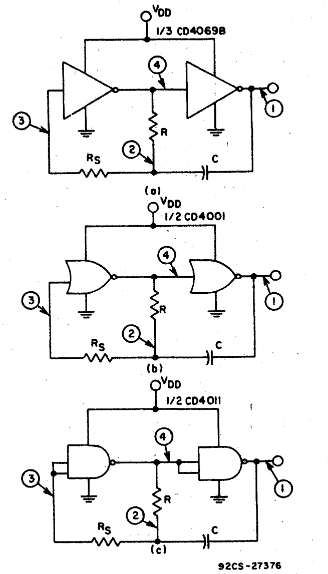


Fig. 1 – Astable multivibrator circuits that employ two COS/MOS inverters.

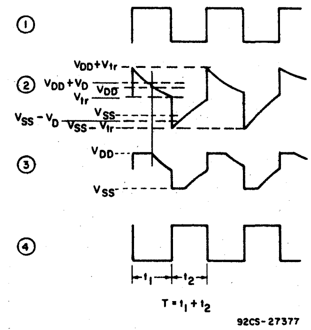


Fig. 2 – RC-oscillator operating waveforms.

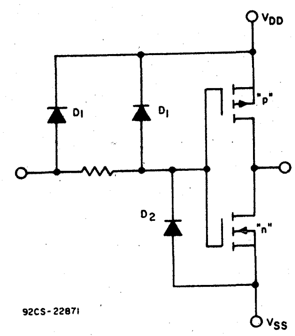


Fig. 3 – Diode protection circuit.

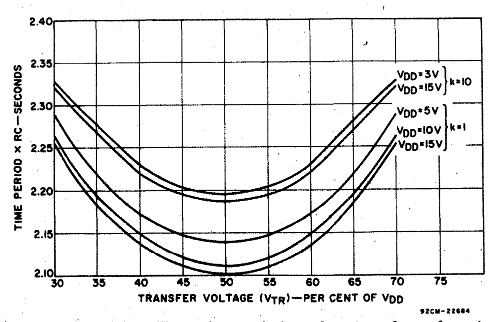


Fig. 4 – Discrete RC-oscillator time period as a function of transfer voltage.

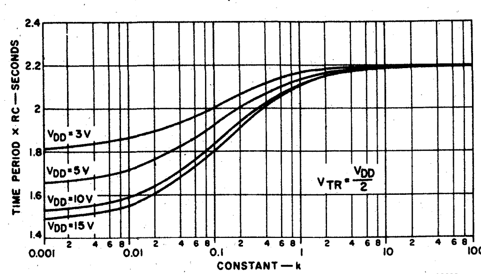


Fig. 5 – Discrete RC-oscillator time period as a function of constant, k.

is allowed to switch well above V_{DD} and below V_{SS} because of R_S. The large swing reduces the effects of variations in transition voltage (V_{TR}). The variable characteristics of the input protection circuit and their effect on stability are greatly reduced because of R_S.

The equation for the period, T, of the circuits in Fig. 1 is given by Eq. 1:[2]

$$T = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD}+V_D)^2}$$

$$-\frac{(K\ \ )}{(K+1)} RC \ln \frac{K\,[V_{DD}+V_D]}{K\,[V_{DD}+V_{TR}] + [V_{TR} - V_D]}$$

$$-\frac{(K\ \ )}{(K+1)} RC \ln \frac{K\,[V_{DD}+V_D]}{K\,[2\,V_{DD} - V_{TR}] + [V_{DD} - V_{TR} - V_D]} \quad (1)$$

where $K = \frac{R_S}{R}$.

With the equation in this form it is easy to see that as K approaches infinity the variation in period as a function of V_{DD} is reduced to zero. This result is shown in Fig. 4, where period as a function of transfer voltage is plotted for various values of V_{DD} and K, and in Fig. 5, which shows period as a function of K for various values of V_{DD}. Variation in period with transfer voltage is also reduced as K increases. This variation decreases from 10 percent for K = 0 to approximately 5 percent as K becomes large.

There are some limitations on the value of R_S. It must not be made too large since a time constant and phase shift is produced by R_S and stray wiring and breadboard capacitance. This shift creates a switching delay in the circuit that changes the time period and, in addition, may cause spurious oscillations and glitches in the multivibrator circuit. A reasonable value for K would be anywhere from 2 to 10, with maximum and minimum values for R_S determined by the above considerations.

Table I shows data measured when typical units were employed in the circuits of Fig. 1. Fig. 6 shows a typical transfer characteristic as a function of temperature. The curve shows that there is very little change in characteristic from low to high temperature. Because the oscillators can also tolerate changes in transfer characteristic without frequency instability, they require no thermal compensation. The frequency at −55°C is extremely close to that at +125°C.

TABLE I – FREQUENCY VARIATIONS OF ASTABLE MULTIVIBRATORS UNDER NORMAL CONDITIONS

UNIT NO.	V_{tr} @ V_{DD} = 10 V (V)	PERIOD (ms)		
		CD4069B		
		V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 15 V
1	5.27	0.988	1.03	1.07
2	5.19	0.988	1.04	1.06
3	5.58	0.990	1.03	1.07
4	5.26	0.990	1.03	1.07
5	5.25	0.991	1.03	1.07
UNIT NO.	V_{tr} @ V_{DD} = 10 V (V)	CD4001A		
		V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 12 V
1	4.08	0.998	1.00	1.00
2	3.92	0.982	0.986	0.990
3	4.76	0.979	1.01	1.01
4	4.07	0.974	0.962	0.962
5	4.42	0.965	0.981	0.991
UNIT NO.	V_{tr} @ V_{DD} = 10 V (V)	CD4011A		
		V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 12 V
1	5.41	1.01	1.02	1.03
2	5.08	1.00	1.03	1.04
3	5.76	0.9900	1.00	1.01
4	5.98	0.983	0.996	1.01
5	5.24	0.996	1.00	1.00

R_S = 0.82 M, R = 0.43 M, C = 910 pF, T = 25°C

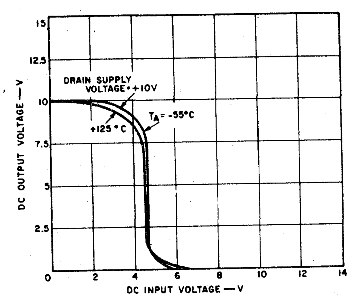


Fig. 6 – Transfer characteristic as a function of temperature.

Table II shows data measured on typical units at temperature extremes. The astable multivibrators shown in Fig. 1 can be gated on and off by use of a NOR or NAND gate as the first inverter, as shown in Fig. 7.

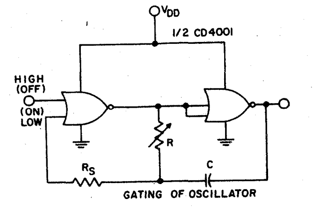


Fig. 7 – Astable multivibrator in which a NOR or NAND gate is used as the first inverter to permit gating of the multivibrator.

Compensation For 50-Percent Duty Cycles

The variation in transfer voltage described above affects the output-pulse duty cycle, as shown in Fig. 8. A true square-wave pulse is obtained only when the transfer voltage occurs at the 50-percent point. However, the duty cycle can be controlled if part of the resistance in the RC time constant is shunted out with a diode, as shown in Fig. 9. Because adjustment of this diode shunt to obtain a specific pulse duty factor causes the frequency of the circuit to vary, a frequency control, R_3, is added to compensate for this variation. It may also be necessary to reverse the diode to obtain the desired duty factor. The frequency of any of the circuits shown can be made variable by replacing the timing resistor with a potentiometer.

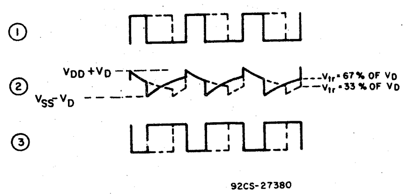


Fig. 8 – Waveforms showing effects of transfer voltage on multivibrator frequency.

Jitter In Astable Circuits

When using the astable circuits described above with other equipment and/or circuits that require off-the-board connections, some

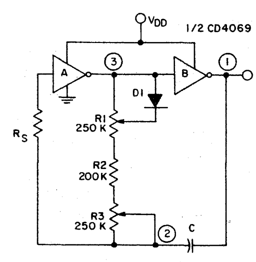


Fig. 9 – Astable multivibrator in which a duty-cycle control is added.

TABLE II – FREQUENCY VARIATIONS OF ASTABLE MULTIVIBRATORS AT TEMPERATURE EXTREMES

UNIT NO.	PERIOD (ms)																	
	CD4069BE						CD4001AF						CD4011AF					
	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 12 V		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 12 V	
	−55°C	85°C	−55°C	85°C	−55°C	85°C	−55°C	125°C	−55°C	125°C	−55°C	125°C	−55°C	125°C	−55°C	125°C	−55°C	125°C
1	0.960	0.974	0.993	1.011	1.023	1.047	0.930	0.924	0.934	0.931	0.936	0.943	0.937	0.937	0.950	0.955	0.958	0.960
2	0.961	0.974	0.997	1.011	1.033	1.045	0.926	0.929	0.947	0.947	0.953	0.956	0.931	0.934	0.942	0.944	0.951	0.956
3	0.965	0.975	0.992	1.010	1.028	1.044	0.914	0.902	0.926	0.918	0.929	0.920	0.925	0.927	0.946	0.949	0.958	0.960
4	0.961	0.973	1.000	1.011	1.033	1.045	0.914	0.903	0.929	0.923	0.936	0.935	0.933	0.931	0.948	0.943	0.950	0.949
5	0.963	0.975	0.994	1.009	1.029	1.043	0.930	0.923	0.955	0.930	0.966	0.938	0.934	0.933	0.953	0.955	0.962	0.963

R_s = 0.82 M, R = 0.43 M, C = 910 pF.

jitter in the output waveform may be encountered. This jitter is introduced into the circuit by noise picked up by the connecting cables and board capacitance and stray wiring. This problem can be corrected with the addition to the circuit of an inverter, as shown in Fig. 10, that isolates the frequency determining circuit nodes from pickup by the output node. The

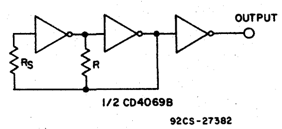


Fig. 10 – Astable multivibrator circuit with buffered output.

output to the astable circuit is then taken from the output of the added inverter.

Monostable Circuits

Fig. 11(a) shows a basic one-shot circuit that uses a single RC time constant. This circuit operates well provided it is adjusted to the COS/MOS unit used. If no adjustment is made, the period T can vary from unit to unit by –40 percent to +60 percent if the transfer voltage varies by ±33 percent, as shown by the waveforms in Fig. 11(b).

The use of some resistance r, Fig. 11, is generally advisable to limit the current if V_{DD} is greater than 5 volts.

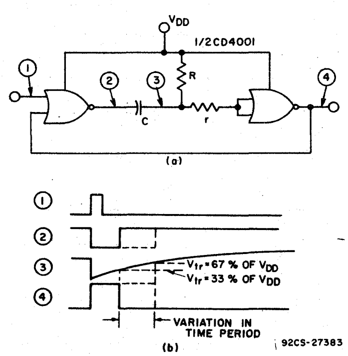


Fig. 11 – Basic one-shot multivibrator circuit: (a) circuit diagram, (b) waveforms.

Compensated Monostable Circuit

Fig. 12 shows a compensated monostable multivibrator type of circuit that can be triggered with a negative-going pulse (V_{DD} to ground). In the quiescent state, the output of inverter B is high. When a negative-going pulse or spike is introduced into the circuit, as shown in the waveforms of Fig. 13, capacitor C_1 becomes negatively charged to ground and the output of inverter A becomes high. Capacitor C_2 then charges to the value of V_{DD} through diode D_1 and

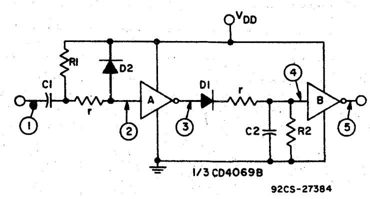


Fig. 12 – Compensated monostable multivibrator circuit.

inverter A, and the output of inverter B becomes low. As capacitor C_1 discharges negatively, it charges through resistor R_1 to the

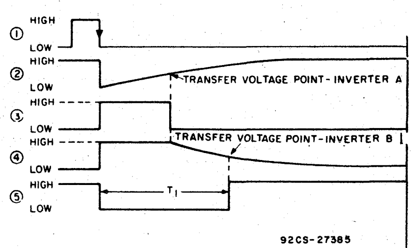


Fig. 13 – Voltage waveforms for monostable multivibrator circuit when a negative-going trigger pulse is applied.

value of V_{DD} (waveform 2). The output of inverter A remains high until the voltage generated by the charging of C_1 is equal to the transfer voltage of inverter A (i.e., until the waveform generated by the charging of C_1 passes through the transfer-voltage curve of inverter A); at that instant the output of inverter A becomes low. Diode D_1 temporarily prevents the discharge of capacitor C_2, which was charged when inverter A was high (waveform 3). Capacitor C_2 then commences to discharge to ground through resistor R_2 (waveform 4). The output of inverter B remains low until the voltage generated by the discharge of C_2 becomes equal to the voltage at the voltage transfer point of inverter B (i.e., until the waveform generated by the discharge of C_2 passes through the transfer-voltage point of inverter B); at that point the output returns to its high state (waveform 5).

The advantage of using two inverters fabricated on the same chip is that they have similar transfer voltages. When two equal RC time constants are used ($R_1C_1 = R_2C_2$), the effects of variations in transfer voltage from device to device are effectively cancelled out, as shown in Fig. 14. Eq. (1) can be used to show that the maximum variation in the time period T is less than 9 percent. The total time for one period, T_1, is approximately 1.4 times R_1C_1.

Unlike the astable circuit, which shows little variation in frequency over the temperature range from –55°C to +125°C, the monostable multivibrator shows some change in time period; the variation is less than 10

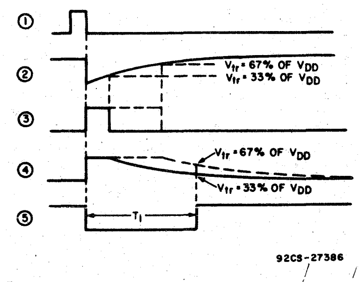


Fig. 14 – Waveforms showing the cancelling effects of transfer-voltage variations of the two COS/MOS inverters when two equal time constants are used.

percent. Table III shows data measured on five units over the temperature range cited above. At 25°C, the variation in the time period T from unit to unit is very small, usually less than 5 percent at a V_{DD} of 10 volts.

The output from inverter B can be held in the low or zero state as long as the R_2C_2 time constant is reinforced by another triggering pulse before the discharge waveform it generates passes through the transfer-voltage point of inverter B.

Diode D_2 in Fig. 12 is internal to the COS/MOS circuit. As discussed for the astable oscillator, it is part of the input protection circuit shown in Fig. 2, and clamps the input at V_{DD}.

Figs. 15 and 16 show two variations of the monostable circuit together with their associated waveforms. The circuit of Fig. 15 triggers on the negative-going excursions of the input pulse in the same manner as the circuit of Fig. 12. The output pulse is positive-going and is taken from the first inverter. This circuit does not need an external diode. The circuit of Fig. 16 triggers on the positive-going excursion of the input pulse, and then locks back on itself until the RC time constants complete their discharge. The circuits of Figs. 15 and 16 cannot be retriggered until they return to their quiescent states.

Low Power Monostable Circuit – The monostable circuits discussed thus far dissipate some power because one or both of the inverters are on during the charging or discharging of the capacitor. This power dissipation will be extremely low provided the

TABLE III – FREQUENCY VARIATION OF MONOSTABLE MULTIVIBRATORS OPERATING AT THREE TEMPERATURES

UNIT NO.	PERIOD (ms) CD4069BE								
	−55°C			+25°C			+85°C		
	V_{DD}=5 V	V_{DD}=10 V	V_{DD}=15 V	V_{DD}=5 V	V_{DD}=10 V	V_{DD}=15 V	V_{DD}=5 V	V_{DD}=10 V	V_{DD}=15 V
1	0.73	0.40	0.30	0.74	0.41	0.32	0.74	0.41	0.32
2	0.74	0.38	0.34	0.76	0.40	0.36	0.76	0.41	0.36
3	0.76	0.40	0.32	0.75	0.40	0.34	0.75	0.40	0.34
4	0.76	0.36	0.35	0.74	0.42	0.36	0.74	0.42	0.36
5	0.75	0.42	0.34	0.76	0.41	0.35	0.76	1.42	0.36
UNIT NO.	PERIOD (ms) CD4001A								
	−55°C			+25°C			+125°C		
	V_{DD}=5 V	V_{DD}=10 V	V_{DD}=12 V	V_{DD}=5 V	V_{DD}=10 V	V_{DD}=12 V	V_{DD}=5 V	V_{DD}=10 V	V_{DD}=12 V
1	0.39	0.45	0.50	0.41	0.46	0.50	0.41	0.46	0.51
2	0.40	0.46	0.50	0.42	0.46	0.50	0.43	0.47	0.50
3	0.40	0.47	0.52	0.43	0.49	0.54	0.43	0.49	0.55
4	0.42	0.46	0.50	0.44	0.47	0.53	0.43	0.48	0.54
5	0.40	0.44	0.48	0.41	0.46	0.51	0.42	0.46	0.51
UNIT NO.	PERIOD (ms) CD4011A								
	−55°C			+25°C			+125°C		
	V_{DD}=5 V	V_{DD}=10 V	V_{DD}=12 V	V_{DD}=5 V	V_{DD}=10 V	V_{DD}=12 V	V_{DD}=5 V	V_{DD}=10 V	V_{DD}=12 V
1	0.58	0.53	0.49	0.57	0.52	0.48	0.56	0.52	0.48
2	0.55	0.50	0.45	0.54	0.50	0.44	0.55	0.50	0.45
3	0.56	0.52	0.44	0.55	0.51	0.44	0.55	0.50	0.44
4	0.55	0.52	0.46	0.56	0.52	0.46	0.57	0.52	0.46
5	0.56	0.50	0.46	0.57	0.51	0.46	0.58	0.50	0.46

$R_1 = R_2 = 43$ M, $C_1 = C_2 = 910$ pF

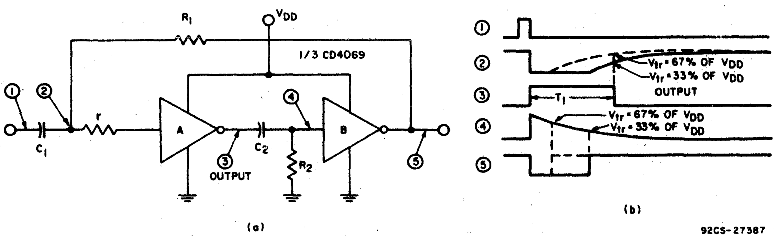


Fig. 15 – Monostable multivibrator that is triggered by a negative-going input pulse: (a) circuit diagram, (b) waveforms.

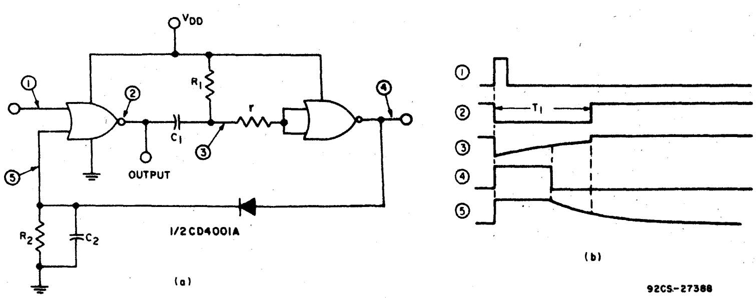


Fig. 16 – Monostable multivibrator that is triggered by a positive-going input pulse: (a) circuit diagram, (b) waveforms.

"one-shot" pulse width is short compared to the overall cycle time. Fig. 17 shows the current waveform associated with the circuit of Fig. 12. This waveform is very wide at the base, and some current flows for approximately twice the time period.

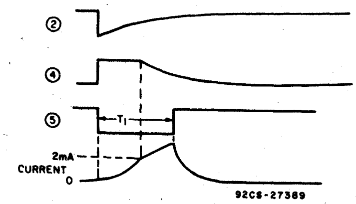


Fig. 17 – Current waveforms for the diode-compensated multivibrator shown in Fig. 12.

Fig. 18(a) shows a circuit using the CD4007A. This device dissipates much less

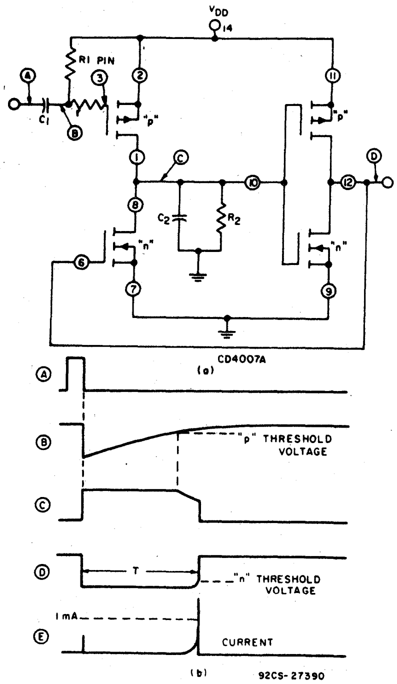


Fig. 18 – Low-power monostable multivibrator: (a) circuit diagram, (b) waveform.

power than the other circuits shown but is not as stable; circuit operation is described by the waveforms in Fig. 18(b). In the quiescent state, the p-channel transistor of the first inverter is biased off while the n-channel transistor (which derives its control from the output of the second inverter) is biased on. Therefore, the output at C is low, and that at D is high. When a negative-going pulse is introduced into the circuit through capacitor C_1, the p-channel device is turned on.

Capacitor C_2 then charges to V_{DD}, the output at D becomes low, and the n-channel device of the first inverter is turned off. Capacitor C_1 immediately begins to charge to V_{DD} through R_1 (waveform B). The p-channel transistor remains on, keeping capacitor C_2 charged to V_{DD} until the voltage generated reaches the threshold voltage level and turns the transistor off. The n-channel transistor of the first inverter is still off because the output of the second inverter (waveform D) is still low. When the p-channel device of the first inverter turns off, capacitor C_2 begins to discharge through resistor R_2 (waveform C) to ground. As C_2 discharges, the voltage passes through the threshold-voltage point of the second p-channel transistor, and that transistor begins to turn on. The voltage then begins to rise (waveform D), and the n-channel device of the first inverter turns on and provides a second discharge path for capacitor C_2. As a result, the output waveform changes state from low to high very rapidly to complete the cycle.

The major advantage of the circuit of Fig. 18 is its low power dissipation. Because the circuit depends on the p-channel transistor threshold, the time period T varies from unit to unit and with temperature variations. Some compensation can be provided if the R_2C_2 time constant is made approximately three times larger than the R_1C_1 time constant, as shown in Table IV.

TABLE IV – FREQUENCY VARIATIONS OF MONOSTABLE MULTIVIBRATORS WITH TEMPERATURE WHEN R_2C_2 TIME CONSTANT IS LARGE COMPARED TO R_1C_1

CD4007A UNIT NO.	PERIOD WITH V_{DD} = 10 V (ms)		
	–55°C	25°C	125°C
1	0.740	0.759	0.779
2	0.740	0.754	0.760
3	0.730	0.735	0.735
4	0.750	0.750	0.759

R_1 = 100K, R_2 = 1 M, r = 36K, C_1 = C_2 = 910 pF

Current in the circuit of Fig. 18 can be minimized by removing capacitor C_2 so that only stray capacitance is present at the input of the second inverter. A comparison of time-period variations under this condition is shown in Table V. Again, the variations from unit to unit are caused by differences in p-channel transistor threshold.

TABLE V – FREQUENCY VARIATIONS OF MONOSTABLE MULTIVIBRATORS WITH TEMPERATURE WHEN C_2 CONSISTS OF STRAY CAPACITANCE ONLY

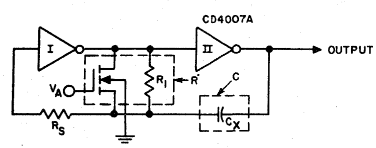
CD4007A UNIT NO.	PERIOD WITH V_{DD} = 10 V (ms)		
	–55°C	+25°C	125°C
1	0.121	0.125	0.129
2	0.110	0.115	0.118
3	0.120	0.124	0.127
4	0.103	0.105	0.108

R_1= 100K, R_2 = 1M, r = 36K, C_1 = 910 pF, C_2 = Stray

APPLICATIONS

Voltage-Controlled Oscillators

Fig. 19 shows a circuit similar to the circuit in Fig. 1. C is variable (by adjustment of C_X) and R is variable (by adjustment of V_A). The value of R varies from approximately 1 kilohm to 10 kilohms. These limits are determined by the parallel combi-



NOTE:
INVERTERS AND n–CHANNEL DEVICE ARE AVAILABLE IN A SINGLE COS/MOS PACKAGE:
1–CD4007
TYPICAL VALUES:
R_1 = 10 kΩ $\quad$ C_X = 0.001 – 0.004 μF
R_S = 100 kΩ $\quad$ 0 ≤ V_A ≤ V_{DD}

* USE PROPER SUFFIX TO DENOTE PACKAGE REQUIRED – SEE APPENDIX.

92CS-22878R1

Fig. 19 – Voltage controlled oscillator.

nation of R1 (10 kilohms) and the resistance of the n-channel device, which varies from 1 kilohm (R_{ON}) to approximately 10^9 ohms (R_{OFF}).

When $V_A = V_{SS}$, the n-channel device is off and R = R_{OFF} ‖ R1, which is approximately equal to R1 or 10 kilohms because R_{OFF} is very much greater than R1. When $V_A = V_{DD}$, the n-channel device is fully on and R = R_{ON} ‖ R1 or approximately R_{ON}, which is equal to 1 kilohm because R_{ON} is very much less than R_1.

The center frequency of the oscillator is varied by adjustment of C_X.

Voltage-Controlled Pulse-Width Circuits

Fig. 20(a) shows a further modification of the circuit of Fig. 1(a); in the modified circuit the pulse width may be modulated by varying V_A, but only if R_X is sufficiently high. As an example: if C = 0.0022 microfarads, R_X will be approximately 35 kilohms. Lower values of R_X have an adverse effect on frequency. If R_X is less than 10 kilohms, there is a value of V_A that will cause the oscillator to cut off. Table VI lists values of

TABLE VI – PULSE WIDTH AS A FUNCTION OF V_A AND V_{DD}

V_A	PULSE WIDTH μs		
	V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 12 V
0	30	28	28
0.5	30	28	28
1.0	30	28	27
1.5	28	26	27
2.0	26	24	22
2.5	26	22	20
3.0	–	21	20
3.5	–	21	20

C = 0.0015 μF, Period = 55 μs

pulse width (B in Fig. 20(b)) for various values of V_A and V_{DD}. Fig. 20(b) shows the waveform for the circuit described.

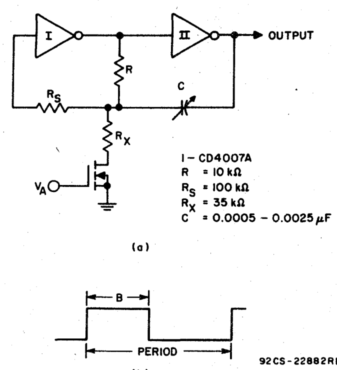


Fig. 20(a) – Voltage controlled pulse-width circuit, (b) output waveform.

Phase-Locked Voltage-Controlled Oscillator

The voltage-controlled oscillator, V_{CO}, can be operated as a phase-locked oscillator by the application of a frequency-controlled voltage to the gate of the n-channel device. Fig. 21 shows the block diagram of an FM discriminator using the phase-locked VCO. Block A is the same circuit of Fig. 19. The output of the phase comparator is fed to the gate of the n-channel device (V_A). If the two inputs to the phase comparator are different, the change of V_A causes the output frequency of the VCO to change,

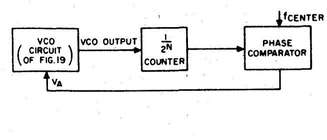


Fig. 21 – VCO used in phase-locked loop.

Fig. 22. This change is divided by 2^N and fed back to the phase comparator.

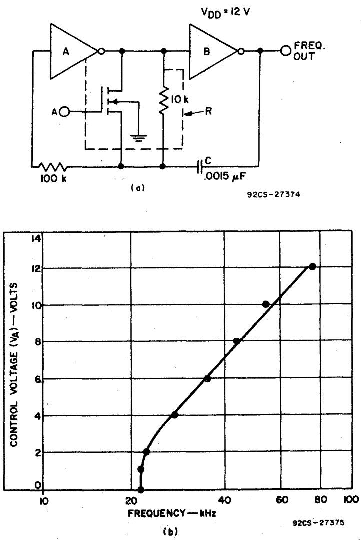


Fig. 22 – (a) VCO, (b) control voltage as a function of output frequency.

Frequency Multipliers

Fig. 23(a) shows a frequency doubler. A 2^N multiplier can be realized by cascading this circuit with N-1 other identical circuits. The leading edge of the input signal, differentiated by R1 and C1 and applied to input No. 1 and the NAND gate, produces a pulse at the output. The trailing edge of the input pulse, after having been inverted, is differentiated and applied to input No. 2 of the NAND gate; it produces the second output pulse from the NAND gate. The waveforms for five points in the circuit are shown in Fig. 23(b).

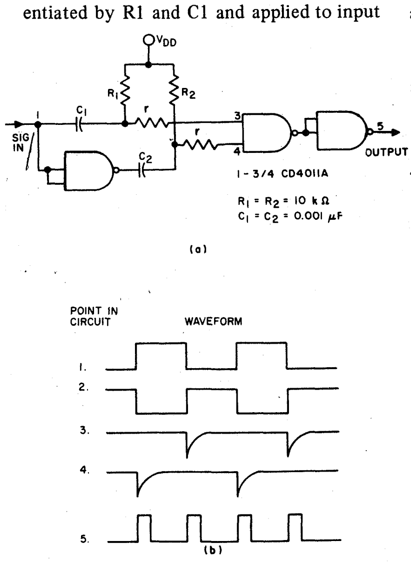


Fig. 23 – (a) Frequency-doubler schematic, (b) waveforms.

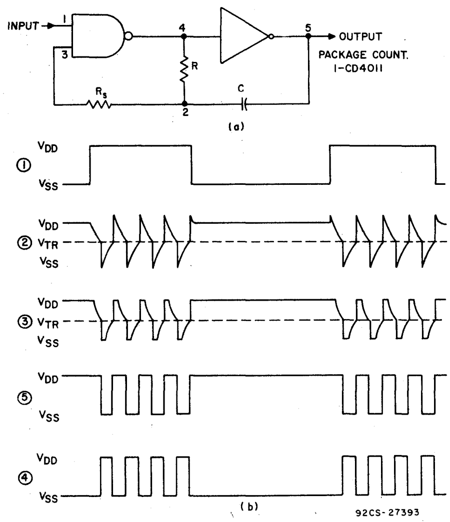


Fig. 24 – (a) Modulator circuit, (b) waveforms.

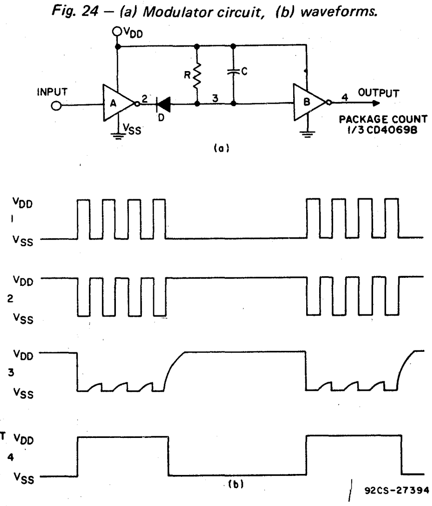


Fig. 25 – (a) Demodulator circuit, (b) waveforms.

Modulation/Demodulation (Envelope Detection)

Pulse modulation may be accomplished by use of the circuit shown in Fig. 24(a). This circuit is another variation of Fig. 1.

Modulation or envelope detection of pulse-modulation waves is performed by the circuit shown in Fig. 25(a). The carrier burst is inverted (by inverter A); its first negative transition at point 2 turns on the diode (D) to provide a charging path for C through the n-channel resistance to ground. On the positive transition of the signal (at point 2), the diode is cut off and C discharges through R. The discharge time constant (RC) is much greater than the time of the burst-signal period. Point 3, therefore, never reaches the switch point of inverter B until the burst has ended. The waveforms for 4 points in the circuit are shown in Fig. 25(b).

References

1. Further information on astable and monostable circuits using MSI devices may be found in RCA Application Note ICAN-6230, "Using the CD4047 in COS/MOS Timing Applications", and in the RCA Data Sheet for the CD4098 Dual Monostable Multivibrator.
   (Note: COS/MOS Hex Buffers CD4009A and Quad Buffer CD4041A are not recommended for use as multivibrators because of very high power consumption in the linear mode for long time constants. In addition, the hex buffers have a large imbalance between I_{source} and I_{sink} capability, which makes oscillator start-up more unpredictable.)
2. For the derivation of this equation, see RCA Application Note ICAN-6230, "Using the CD4047A in COS/MOS Timing Applications."

Guide to Better Handling and Operation of CMOS Integrated Circuits

by J. Flood and H. L. Pujol

This Note recommends specific handling and operating practices that minimize the probability of damage to CMOS integrated circuits in the manufacturing operation and the field environment.

A description of various gate-oxide networks that protect against electrostatic discharge in both A-series and B-series RCA COS/MOS product is provided. A practical explanation of the SCR latch-up mechanism and its associated failure mode is given. In addition, operating procedures that help prevent device malfunction are described.

HANDLING CONSIDERATIONS

All CMOS devices are susceptible to damage by the discharge of electrostatic energy between any two pins. The gate input is equivalent to a small, low-leakage capacitor (5 picofarads typical) in parallel with a very high resistance (10^{12} ohms typical). This extremely high input impedance lends itself readily to the buildup of electrostatic charges. Therefore, because the gate-oxide breakdown of a CMOS device is typically 80 volts, damage by high levels of electrostatic discharge can occur.

To protect the gate oxide against high levels of electrostatic discharge, protective networks are implemented on all RCA CMOS (COS/MOS) devices, as described below.

Standard Protection Networks

Fig. 1 shows the standard protection network incorporated on all A-series devices and some B-series devices. Input-diode D_2 is a distributed resistor-diode network that appears as two diodes to V_{DD}.

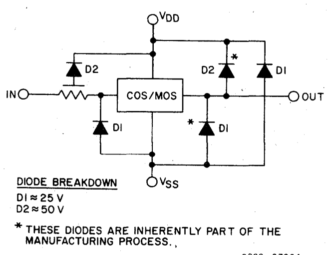


Fig. 1 – Standard protection network.

Improved Protection Network

Fig. 2 shows the improved protection network incorporated on most new B-series devices as well as on all A-series, B-converted types.

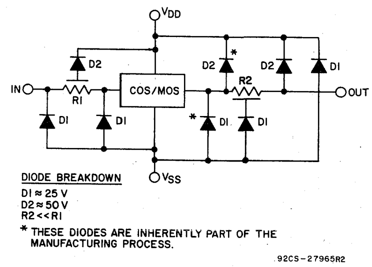


Fig. 2 – Improved protection network.

Other Protective Networks

Fig. 3 shows the modified protective network for a CD4049/4050 buffer. The input diode to V_{DD} is not incorporated so that the level-shifting function can occur.

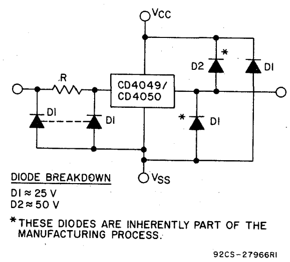


Fig. 3 – Modified protection network.

Fig. 4 shows a transmission gate with the intrinsic diodes that protect against electrostatic discharge.

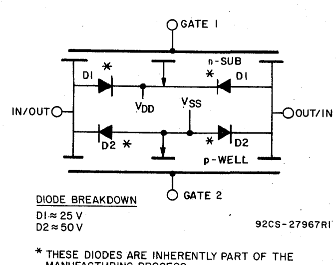


Fig. 4 – Transmission gate with intrinsic diodes that protect against electrostatic discharge.

The protection networks described in this Note were characterized by using the equivalent body discharge network of Fig. 5. There are 12 possible combinations by which a device can be damaged. A discussion of the combinations is beyond the scope of this Note; however, Table I shows worst-case protection levels for the above networks.

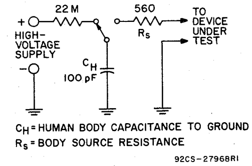


Fig. 5 – Equivalent-body discharge network.

Additional protection can be obtained by adding external series resistors at device inputs. The value of this resistance should be in the range of 10 kilohms for gate inputs and 1 kilohm for transmission gate inputs, where applicable. In addition, zener diodes at the output pins can clamp the voltage at a safe level. The zener value should not exceed the absolute maximum rating of the part.

On-chip protection resistors are not used on transmission gates so as to maintain low on resistance. Some recent designs, however, do have protection diodes to V_{DD} and V_{SS} close to the bond pads. The 800-volts worst case capability is provided by the intrinsic diodes shown in Fig. 4.

TABLE I – Worst-Case Capability of Protective Networks

Protective Network	Worst-Case Capability
Standard (inc. CD4049, CD4050)	1 kV to 2 kV
Improved	4 kV
Transmission Gate	< 800 V

General Handling Rules

Table I indicates the typical, worst-case voltage discharges from the network of Fig. 5 that the above networks can withstand. Because every manufacturing environment is different, levels above those shown in Table I should be anticipated and protected against by following the handling recommendations of Table II.

Dry weather (relative humidity less than 30 percent) tends to increase greatly the accumulation of static charges on any surface. Conversely, higher humidity levels (40 to 50 percent) tend to reduce the magnitude of the static voltage generated. In a low-humidity environment, the handling precautions listed above take on added importance and should be adhered to without exception.

HANDLING OF UNMOUNTED CHIPS

In handling unmounted chips, differences in potential should be avoided. A conductive carrier or a carrier having a conductive overlay should be used. Another important consideration is the sequence in which bonds are made; the V_{DD} (device supply) connection should always be made before the V_{SS} (ground) bond.

HANDLING OF SUBASSEMBLY BOARDS

After COS/MOS units have been mounted on circuit boards, proper handling precau-

TABLE II – General Handling Recommendations

	Should be conductive	Should be grounded to common point
Handling equipment	X	
Metal Parts of Fixtures and Tools		X
Handling Trays	X	
Soldering Irons		X
Table Tops	X	X
Transport Carts	X	
Manufacturing Operating Personnel		Utilize grounded, metal or conductive plastic wrist straps with 1-megohm series resistor
General Handling of Devices		Utilize grounded, metal or conductive plastic wrist straps with 1-megohm series resistor

tions should still be observed. Until these subassemblies are inserted into a complete system in which the proper voltages are applied, the board is no more than an extension of the leads of the device mounted on the board.

It is good practice to put conductive clips or conductive tape on the circuit-board terminals. This precaution prevents static charges from being transmitted through the board wiring to the devices mounted on it.

AUTOMATIC HANDLING EQUIPMENT

When automatic handling equipment is used, it may not always be possible to eliminate static electricity through grounding techniques alone. Automatic feed mechanisms must be insulated from the devices under test at the point where the devices are connected to the test set. The anvil transport portion of the automatic handling mechanism can generate very high levels of static electricity as a result of the continuous flow of devices over and then separating from the anvil. Total control of these static voltages is critical because of the high throughputs associated with automatic handling.

Fortunately, the resolution of this problem is simple, practical, and inexpensive. Ionized-air blowers, which supply large volumes of ionized air to objects that are to be charge neutralized, are commercially available from many supply sources. Field experience with ionized-air techniques reveals this method to be extremely effective in eliminating static electricity when grounding techniques cannot be used.

Failure Mechanisms

Electrical damage resulting from handling is usually caused by either of the two following failure mechanisms:

1. Low-level static electricity (voltage of 1 kV to 4 kV). Input diode protection may be overstressed and input leakage currents as high as 1 milliampere across diodes may cause a malfunction.
2. High-level static electricity (voltages greater than 4 kV). Gate oxides may become short-circuited. Inputs to V_{DD} or V_{SS} terminals will be low-impedance inputs.

The presence of these types of device malfunction can be detected by curve-tracer checks of the input protection diodes described above. Diode degradation resulting from static electricity is observable in the low-reverse-breakdown characteristics shown on the curve tracer. On the other hand, damage resulting from high levels of static electricity are observed as a resistive short to V_{DD} or V_{SS}.

Typical Manufacturing Area Procedure

The example below illustrates all of the above recommendations for handling CMOS devices in a typical manufacturing environment. Although existing protective networks offer a high level of protection against electrostatic discharge, this example emphasizes specific precautions that can help eliminate damage.

Receiving Area

Devices should not be removed from their conductive or antistatic carriers. If devices are not received in conductive or antistatic packing material, they should be returned to the supplier.

Incoming Inspection

Physical – Parts should be counted without removing them from their containers.

Storage – Devices should remain in carriers. Even a partial removal of IC's from a carrier should only be done by a grounded operator. Devices removed should be placed in a conductive tray.

Electrical – All testing should be performed by a grounded operator. Devices should be reinserted in conductive carriers after completion of a test.

PC Board Assembly

It is desirable that PC boards have shorting bars installed prior to assembly (soldering). Where possible, CMOS IC's should be the last component installed on the PC board.

Boards should be transported to the wave-solder area in conductive carriers. Flux removal should be done with an acceptable solvent. Examples of specific, acceptable alcohols are isopropanol, methanol and special denatured alcohols such as SDAI, SDA30, SDA34 and SDA44. The removal of flux from non-hermetic and molded-plastic devices by means of soap and water in a dishwasher is NOT recommended as this procedure will adversely affect the long-term life of the device.

OPERATING CONSIDERATIONS

Proper operating procedures are as important as proper handling techniques. A review of RCA COS/MOS A-series and B-series operating characteristics and ratings is given in Table III.

Operating Voltage

When devices are operated near the maximum supply-voltage range, power-supply turn-on or turn-off transients, power-supply ripple or regulation, and ground noise should be suppressed; any of the above conditions must not cause ($V_{DD} - V_{SS}$) to exceed the absolute maximum rating. A good practice is to use a zener protection diode in parallel with the power bus. The zener value should be above the expected maximum regulation excursion, but should not exceed the maximum supply voltage. Fig. 6 illustrates a practical zener shunt circuit. A current-limiting resistor is included if the supply-current compliance is higher than the zener power-dissipation rating for a given zener voltage. The shunt capacitor value is chosen to supply required peak-current switching transients.

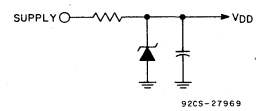


Fig.6 – Zener-diode shunt circuit.

Unused Inputs

All unused input leads must be connected to either V_{SS} or V_{DD}, whichever is appropriate for the logic circuit involved. A floating input on a high-current type (such as the CD4009A, CD4010A, CD4041A, CD4049A, CD4050A) can result not only in faulty logic operation, but can cause the maximum power dissipation of 500 milliwatts to be exceeded; the result may be damage to the device. Another consideration with high-current devices is the need for a pull-up resistor between the inputs and V_{SS} or V_{DD} should there be any possibility that the device terminals may become temporarily open or unconnected (e.g., if the printed circuit board driving the high-current types is removed from the chassis). A useful range of values for such resistors is from 0.2 to 1 megohm.

Input Signals

Signals should not be applied to the inputs while the device power supply is off unless the input current is limited to a steady-state value of typically less than 10 milliamperes. Input-signal interfaces that are the allowable 0.5 volt above V_{DD} or below V_{SS} should be current-limited to typically 10 milliamperes or less.

Whenever the possibility of exceeding 10 milliamperes of input current exists,

TABLE III – Maximum Ratings of RCA COS/MOS Devices (Voltages referenced to V_{SS})

DC Supply Voltage Range	3 to 15 V (A Series); 3 to 20 V (B Series)
Recommended Operating Voltage	3 to 12 V (A Series); 3 to 18 V (B Series)
DC Input Voltage Range	–0.5 to V_{DD} + 0.5 V
Dissipation per Package	500 mW
Device Dissipation per Output Transistor	100 mW
Storage Temperature Range	–65 to +150°C
Operating Temperature Range	
Ceramic Package Types	–55 to +125°C
Plastic Package Types	–40 to +85°C
Lead Temperature (during soldering) at a distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+ 265°C

a resistor in series with the input is recommended. The value of this resistor can be as high as 10 kilohms without affecting static electrical characteristics. However, speed will be reduced because of the added RC delay. Particular attention should be given to long input-signal lines where high inductance can increase the likelihood of large-signal pickup in noisy environments. In these cases, series resistance with shunt capacitance at the IC input terminals is recommended. The shunt capacitance should be made as large as possible consistent with the system speed requirements.

Fan-Out – COS/MOS to COS/MOS

All RCA COS/MOS devices have a dc fan-out capability of greater than 50. The reduction in COS/MOS switching speed caused by added capacitive loading should, however, be consistent with high-speed system design. The input capacitance is typically 5 picofarads for most types; the CD4009 and CD4049 buffers have a typical input capacitance of 15 picofarads.

Maximum Clock Rise and Fall Time

All COS/MOS clocked devices show maximum clock rise- and fall-time ratings (normally 5 to 15 microseconds). With longer rise or fall times, a device may not function properly.

Parallel Clocking

When two or more different CMOS devices use a common clock, the clock rise time must be kept at a value less than the sum of the propagation delay time, the output transition time, and the setup time. Most flip-flop and shift-register types are included in this rule and are so noted in the individual data sheets.

Output Short Circuits

Shorting of outputs to V_{SS} or V_{DD} can cause the device power dissipation to exceed the safe value of 500 milliwatts. In general, outputs of these types can all be safely shorted when the device is operated with $(V_{DD} - V_{SS}) \geq 5$ volts, but the 500 milliwatt dissipation ratings may be exceeded at higher power-supply voltages. For cases in which a short-circuited load, such as the base of a p-n-p or n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for safe operation below 500 milliwatts. Note that a single output transistor short must be limited to 100 milliwatts.

SCR Latch-Up

Operation above maximum ratings can force CMOS devices into a p-n-p-n SCR "latch-up" mechanism, which can be destructive. Any transients should be avoided and any large loads occurring during operation near the maximum rating should be avoided.

"Latch-up" is considered to be the creation of a low-resistance path between the power supply and ground on a circuit during an electrical pulse; the path remains a low-resistance path after the pulse. In CMOS circuits, several parasitic bipolar transistors exist, as shown in Fig. 7. The p-n-p transistor is a wide-base lateral structure whose β, normally less than 0.2, is a function of device geometry. The conditions for SCR turn-on are as follows:

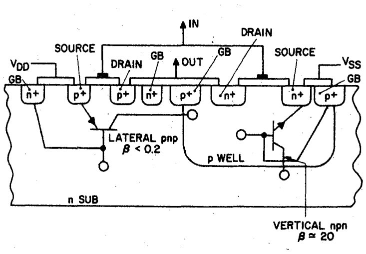


Fig.7 – Parasitic bipolar transistors in CMOS circuits.

1. β n-p-n x β p-n-p $\geq$ 1
   (vert.) (lat.)
2. The lateral p-n-p and vertical n-p-n base emitter junctions are forward biased.
3. The bias circuit that applies power to V_{DD} and to the input must be capable of supplying current equal to the holding current of potential SCR's.

Fig. 8 shows the equivalent circuit for the SCR structure present in CMOS circuits.

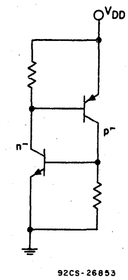


Fig.8 – Equivalent circuit for the SCR structure present in CMOS circuits.

Fig. 9 shows a curve of I_{DD} as a function of V_{DD}, which illustrates the effect of secondary breakdown and SCR latch-up.

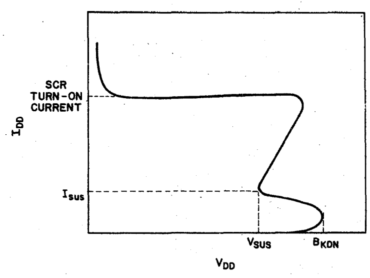


Fig.9 – Curve illustrating effect of secondary breakdown and SCR latch-up.

Table IV shows typical values of breakdown voltage and sustaining voltage and current for RCA COS/MOS A-series and and B-series devices. The table shows that B-series devices are much harder to latch than A-series types because of the higher breakdown voltage.

TABLE IV – Breakdown Voltage and Sustaining Voltage and Current Values

Characteristic	A-Series	B-Series
$V_{BKDN_{min}}$	17 V	25 V
V_{sus}	15 V	22 V
I_{sus}	Type-Dependent 2–40 mA	50–100 mA

ICAN-6532

Fundamentals of Testing COS/MOS Integrated Circuits

by J. Flood

This Note describes the techniques employed in testing RCA COS/MOS devices to assure their adherence to data-sheet specifications, and provides information useful in data-sheet interpretation and in the inspection of incoming devices. RCA COS/MOS devices are available in two basic families: A-series (3- to 15-volt product) and B-series (3- to 20-volt product).

RCA COS/MOS circuits are 100-percent tested by circuit probe in the wafer stage and are 100-percent tested again after they have been packaged. DC tests of RCA devices are performed at 5, 10, 15, and 20 volts; functionality is checked at 3, 17, and 22 volts depending on family (i.e., A or B series). Sample testing is used to assure adherence to quality requirements and ac specifications.

Static tests, high-speed functional and dc parametric tests, are performed at wafer and package stages by means of a Teradyne J283 test set. A Teradyne S157CM test set and a Macrodata MD154 test set are used in dynamic testing. Dynamic tests are performed with 15 and 50 picofarad loads. Testing at 15 picofarads is accomplished primarily by laboratory "bench-test" techniques; automatic testing at 15 picofarads is difficult because of the high input capacitance (approximately 20 to 35 picofarads) of most automatic ac test sets.

Users should follow the sequence below when testing COS/MOS devices:

1. Insert the device into the test socket.
2. Apply V_{DD}.
3. Apply the input signal.
4. Perform the test.
5. On completion of test, remove the input signal.
6. Turn off the power supply (V_{DD}).
7. Remove the device from the test socket and insert it into a conductive carrier. COS/MOS devices under test must not be exposed to electrostatic discharge or forward biasing of the intrinsic protective diodes shown in Fig. 1.

For detailed COS/MOS IC handling and operating considerations, refer to RCA Application Note, Guide to Better Handling and Operating of CMOS Integrated Circuits.[1]

STATIC TESTING

DC-Parameter Testing

DC parameters are those specified for steady-state conditions; dc testing of RCA devices is done at 5, 10, 15, and 20 volts depending on the family under test. Nonvarying forcing conditions are applied to the inputs and/or outputs of a package while the device terminals are monitored for expected voltage or current levels.

DC-parameter tests include:

Functional tests
Contact tests (diode measurement)
Leakage tests: quiescent and input
Breakdown voltage tests
Output voltage levels

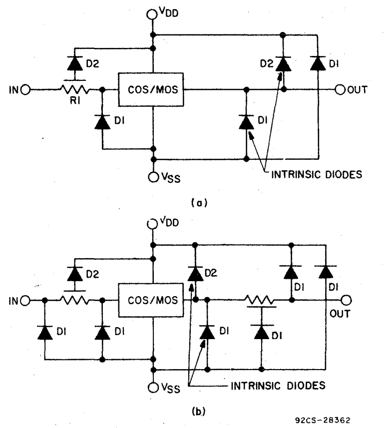


Fig. 1 – (a) Standard protection network used on all CD4000A- and some CD4000B-series devices; (b) improved protection network used on all new RCA COS/MOS devices. Diode breakdown: D1 = 25 V, D2 = 50 V, R2 << R1.

Input voltage test (includes noise-immunity and noise-margin tests)
Output drive-current measurements
Diode tests
Input-capacitance measurements
Additional tests as required

A typical CMOS IC test sequence is shown in Fig. 2.

Functional Tests

Functional tests assure that the device under test will perform its logical operations in accordance with its truth table. The operating voltages for functional tests are shown in Table I. Operation is checked against truth table values by monitoring output-voltage levels for valid logic-high and logic-low levels. Output logic levels for functional tests are:

Table I – Operating Voltage Limits For Functional Tests

	Recommended	Min.	Max.
4000A Series	3 - 12	3	15
4000B Series	3 - 18	3	20

Logic 0: $\leqslant V_{SS} + 0.5$ V

Logic 1: $\geqslant V_{DD} - 0.5$ V, V_{DD} is referenced to V_{SS}.

Fig. 3 shows an example of a CD4001 NOR gate functional test. V_{DD} is selected to cover the desired range of operation. This test is performed at a relatively low frequency ($<<f_{CL}$ max.) and with no load other than stray and probe capacitances.

When complex circuits such as the CD-4094B, Fig. 4, are tested, input signals must

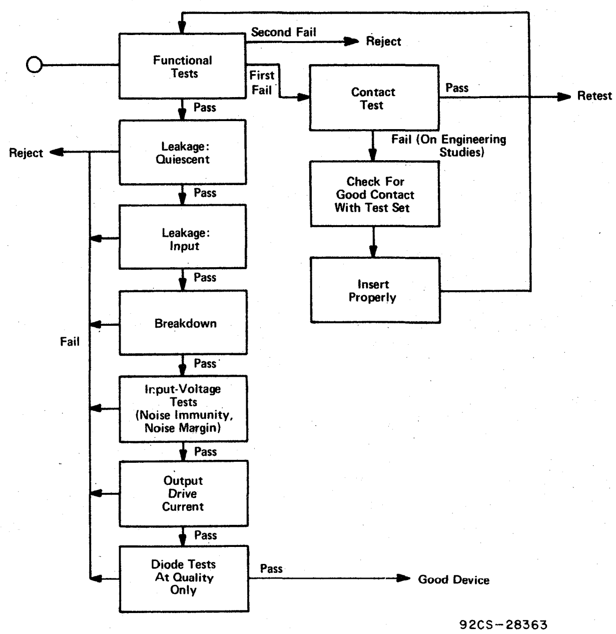


Fig. 2 – A typical COS/MOS IC test sequence.

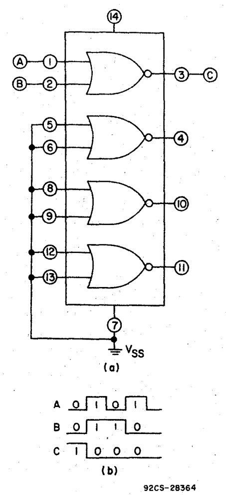


Fig. 3 – Example of CD4001 NOR-gate functional test.

be applied to control the functions being examined. The CD4094B is an 8-stage shift and store register whose eight stages are composed of D-type flip-flops connected in sequential logic form with a common clock. In addition to the flip-flop chain, the device has a latch option at each parallel output stage; the latch is controlled by the strobe input level. The parallel outputs are three-state and are controlled by the output enable level. Data stored in the register is available at the serial outputs on both the positive and negative clock transitions.

Prior to performance of the static or dc parameter tests, which reflect the data-sheet specifications, all register functions must perform 100 percent. Compliance of a device with functional test requirements is determined by monitoring all outputs for proper operation. Functional testing is performed by applying the waveforms shown in the timing diagram of Fig. 5 to the device under test, in this case the CD4094B of Fig. 4. The tests are performed at a frequency well below the maximum operating frequency of the device. Input logic 1 levels are equal to V_{DD}; input logic 0 levels are equal to V_{SS}. Again, output logic 1 and 0 levels are equal to $V_{DD} - 0.5$ V min. and $V_{SS} + 0.5$ V max., respectively. Functional tests for B-series devices are performed at a $V_{DD} - V_{SS}$ of 22 volts, 2.8 volts, and at intermediate levels depending on the device type.

The timing diagram, Fig. 5, shows 0-level data being clocked into the internal Q output of the shift register while the strobe input is maintained low. After eight positive clock transitions, all the internal Q outputs are at logic 0. Prior to the next positive clock transition, the strobe goes to a 1 state; this condition shifts the zeroes from the internal Q outputs to the external Q outputs and the serial outputs. At this time all outputs are at logic 0. The following clock pulses, those starting at time slot 1, begin shifting 1's and 0's to the parallel outputs. The alternate 1's and 0's are fed into the register up to the negative transition at time-slot 8. At this time the strobe input is sent low to check functionality of the latch. Note that a 0 data bit was transmitted to the Q1 output on the positive clock transition at time-slot 8; however, a positive transition at time-slot 9 does not shift the positive data input to the Q1 output. The Q1 output remains latched low because of the low level at the strobe input. When the strobe goes high, the 1 data bit is transmitted to the Q1 output. At this point the latch functionality plus the functions of the strobe, clock, data inputs, Q_S outputs, and Q outputs, Fig. 4, are fully tested, as shown by the timing diagram.

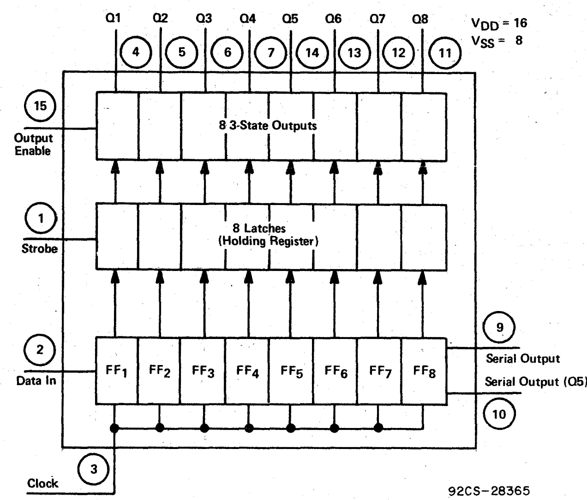


Fig. 4 – Functional diagram of the CD4094B.

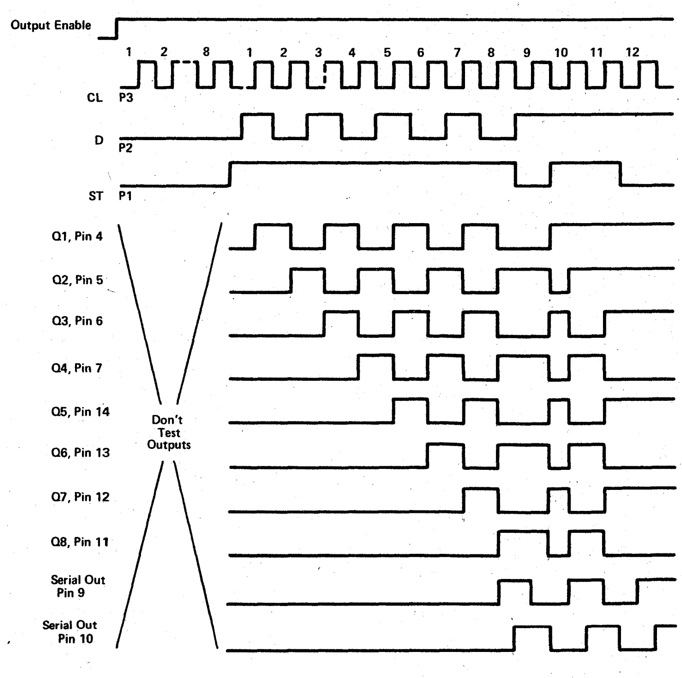


Fig. 5 – Waveforms used in functional testing.

Leakage Current Tests

Two types of static leakage currents are of concern in COS/MOS devices: Quiescent-leakage and input-leakage current.

Quiescent Leakage Current–In bipolar logic devices, such as TTL devices, the current paths that exist from the power source to ground in the quiescent state cause milliamperes of current to flow even when the device is not functioning. Quiescent leakage may be defined for a COS/MOS device as that current that flows from V_{DD} to V_{SS} when, theoretically, all paths for current flow have been opened because the MOS device is off, Fig. 6.

Typical input-leakage-current values for COS/MOS devices are in the picoampere range, hence the high input impedance. Automatic test sets cannot measure picoampere values because of test-set resolution. Input currents are measured using 100 nanoamperes as the maximum allowable leakage for a single input.

Examples of quiescent and input leakage test methods are shown in Figs. 8 and 9. In Fig. 8, the quiescent leakage current I_L (I_{DD} may be substituted for I_L) is measured by eliminating all current paths from V_{DD} to V_{SS}. This is done by turning off either the n or the p devices. The current may be measured in the V_{DD} or the V_{SS} line, whichever is more convenient. Unused inputs must be connected either high or low, depending on the channel leakage to be measured.

Input leakage current in Fig. 9 is measured by means of the gate input. Typical input impedance is 10^{12} ohms; therefore, typical input leakage currents are in the picoampere range. Figs. 8 through 14 show various test circuits for the CD4001A.

The testing of MSI and LSI parts for quiescent leakage current is more complex than that for SSI devices. However, the test is performed in a manner similar to that of the functional test described previously. The CD4090, for example, is connected as shown in Fig. 15. The device is then clocked into its various states, and the current monitored at applicable time slots.

Fig. 16 shows the intrinsic protection circuitry at each external-gate input. With S1 connected to either current source, the voltage drop from the gate input to ground will be one diode drop. A limit of 1.5 volts maximum is usually used to indicate a good diode. With S1 connected to the +100 microampere supply, the presence of the protective diode to the n substrate is tested. With S1 connected to the −100 microampere supply, the presence of the protective diode to the p well is tested. In the event of functional test failures, the above test can be used as a "contact test" to check for proper insertion of the device under test.

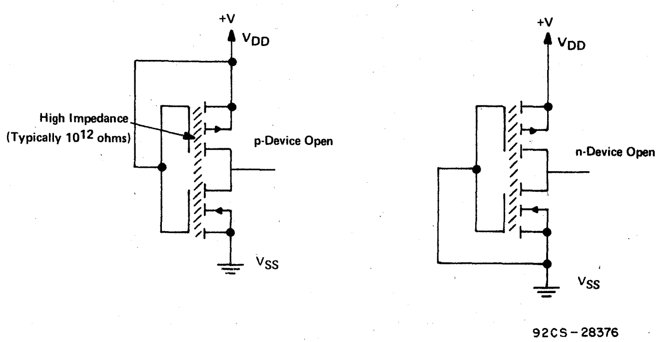


Fig. 6 – Schematic representations of p and n devices when turned off.

There is no perfect switch. However, the COS/MOS technology offers quiescent device currents that are orders of magnitude lower than in other forms of digital logic.

Quiescent-leakage tests are performed for all device states according to their respective truth tables. Voltages for quiescent leakage tests are 5, 10, and 15 volts for the CD4000A series and 5, 10, 15, and 20 volts for the CD4000B series. Power dissipation for COS/MOS devices is in the microwatt range regardless of complexity level, and is relatively stable with variations in temperature.

Input-Leakage Current–Input-leakage current is current that flows through reverse-biased diodes, whether intrinsic or diffused, and through the input-protection network connected to the gate. The diodes present in standard and improved protection networks are shown in Fig. 7.

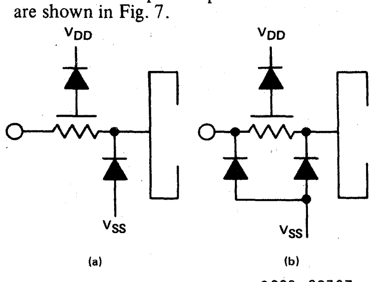


Fig. 7 – (a) Standard and (b) improved protection networks.

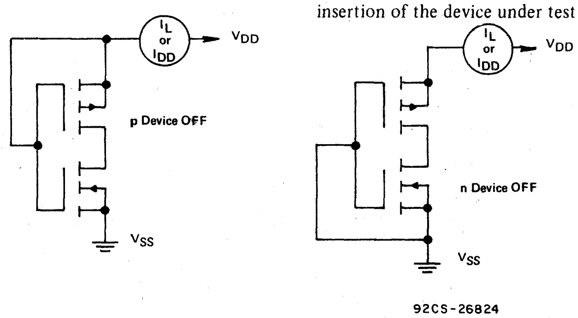


Fig. 8 – Measurement of quiescent leakage current.

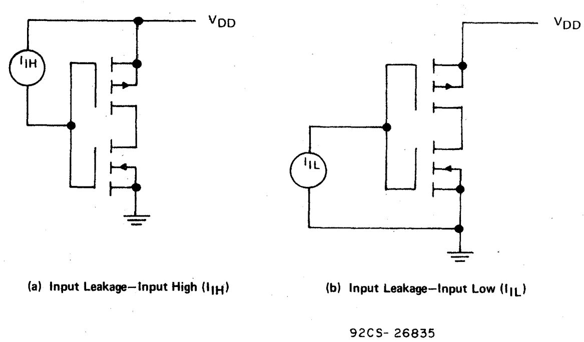


Fig. 9 – Measurement of input leakage.

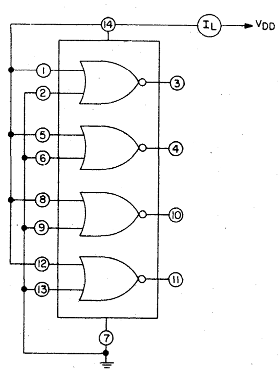


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Fig. 10 – Quiescent-device-current test circuit for the CD4001A, leakage-inputs 1 (I_L).

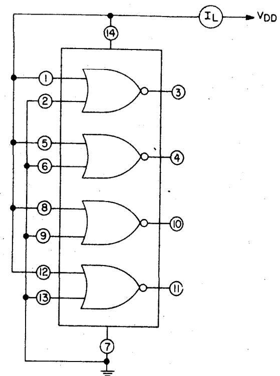

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Fig. 11 – Quiescent-device-current test circuit for the CD4001A, leakage-inputs 2 (I_L).

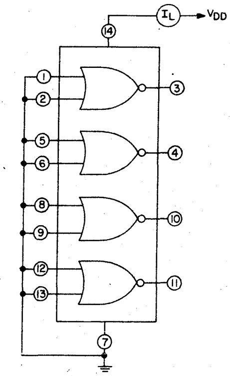

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Fig. 12 – Quiescent-device-current test circuit for the CD4001A, leakage - n-devices off (I_L).

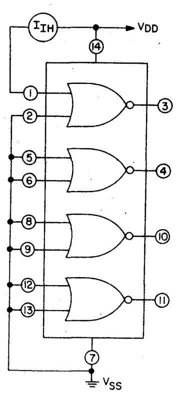

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Fig. 13 – Input-current test circuit for the CD4001A, input high (I_{IH}).

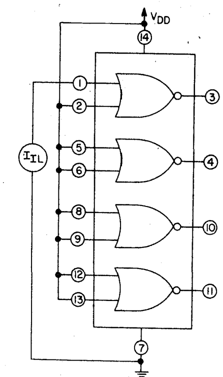

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Fig. 14 – Input-current test circuit for the CD4001A, input low (I_{IL}).

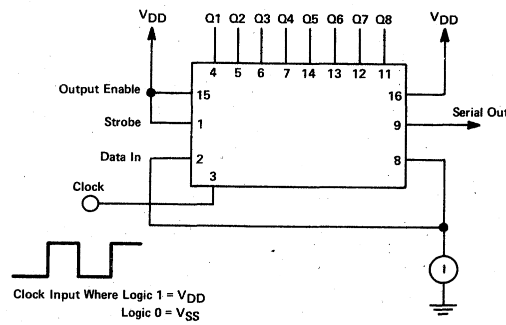

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Fig. 15 – Functional-test arrangement for the CD4090.

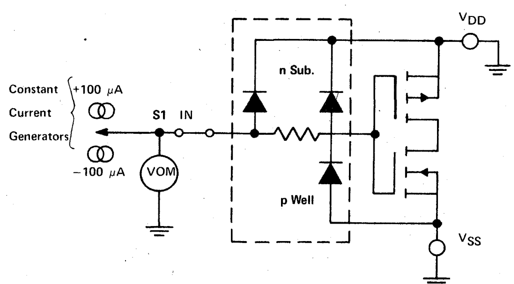

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Fig. 16 – Intrinsic protection circuitry at each external input of a COS/MOS device.

Voltage Breakdown Tests

Breakdown tests are performed on the n and p channels of COS/MOS devices in a manner similar to that of quiescent-leakage-current tests. The purpose of the breakdown test is to assure that channel breakdowns can only occur at voltages above the maximum guaranteed supply voltage; Table II gives limits by series. Voltage breakdown test circuits are shown in Fig. 17. With switch S1 in position 1, the n devices are on and the p^+-to-n-substrate diodes are stressed. With switch S1 in position 2, the p devices are on and the n^+-to-p-well diodes are stressed.

Table II – Channel-Breakdown Limits

	Test Voltage	Max. Current Limit
CD4000A Series	15 V	100 μA
CD4000B Series	20 V	100 μA

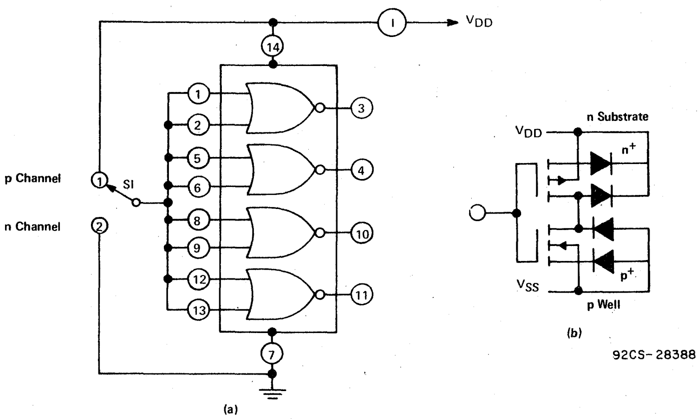

Fig. 17 – Voltage-breakdown test circuit.

Output-Voltage Levels

The output-voltage low (V_{OL}) and the output-voltage high levels (V_{OH}) of a COS/MOS device approach V_{DD} and V_{SS} within a few millivolts. Tests for V_{OL} and V_{OH} are primarily bench-type static tests performed as shown in Fig. 18. With switch S1 in position 1, one n device is turned on and the p devices are turned off. The voltage output will be at V_{SS} + 0.05 volt or V_{SS} – 0 volt. With switch S1 in position 2, all p devices will be turned on and the n devices will be turned off. The voltage output will be at V_{DD} + 0 volt or V_{DD} – 0.05 volt.

Few automatic test sets have the resolution to measure an offset of 50 millivolts from the V_{DD} and V_{SS} supply with satisfactory accuracy at reasonable test speeds.

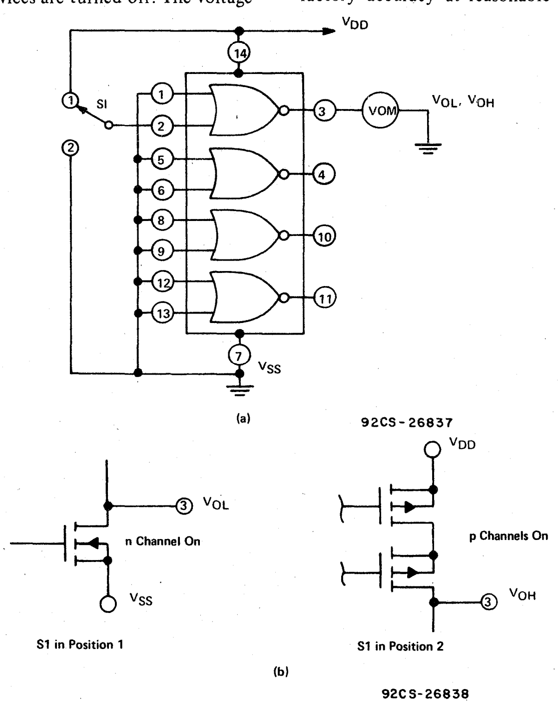

Fig. 18 – Test of output voltage levels (V_{OH} and V_{OL}) of a CD4001A.

Note that in functional testing, the pass/fail criteria for high and low output states of the device is a maximum of 500 millivolts deviation from V_{DD} and V_{SS}.

Noise Immunity

Noise immunity, V_{NL}, V_{NH}, is defined as the maximum low-level input (V_{IL}) for which an output logic level does not change state, and the minimum high-level input (V_{IH}) for which the output does not change state.

The typical noise immunity of a COS/MOS device is 45-percent of V_{DD}; i.e., the input voltage low and high levels will typically change 45-percent of their values before the output logic level changes. V_{IL} is guaranteed to be a maximum of 30 percent of V_{DD}; V_{IH} is guaranteed to be a minimum of 70 percent of V_{DD}.

Noise Margin

Noise margin is the difference between a device output voltage and V_{IL}; i.e., the magnitude of noise-margin voltage is that noise voltage that may be added to any COS/MOS input/output mode.

Noise margin and noise immunity are guaranteed to meet data-sheet specifications by the performance of input voltage tests, as shown in Fig. 19. The input voltage test is performed for each device as in functional testing. V_{IL} and V_{IH} are applied according to the device's truth table. The outputs are monitored for an expected V_{NMH} and V_{NML} state (voltage noise margin, voltage noise margin low).

$$V_{NML} = V_{OL} - V_{IL}$$
$$V_{NMH} = V_{OH} - V_{IH}$$
$$V_{IL} = V_{NL}$$
$$V_{IH} = V_{DD} - V_{NH}$$

Output Drive Current

Tests for output drive currents–I_{DN} (or I_{OL}), sink current, and I_{DP} (or I_{OH}), source current–are conducted by means of the circuits shown in Figs. 20 and 21.

The purpose of the sink-current test, Fig. 20, is to determine the amount of current that the output n device is capable of sinking (with the n channel on) at a given output-voltage level. Fig. 20(a) shows a CD4001AD device whose V_{DD} is equal to 10 volts and whose voltage output is specified at 0.5 volt. The amount of current that the output device can sink varies depending upon the voltage drop across the device (V_{DS}) for a fixed V_{GS}. n-channel drain characteristics are shown in Fig. 20(c).

The purpose of the source-current test, Fig. 21, is to determine the amount of current that the p device is capable of sourcing (with the p channel on) at a given output-voltage level. Fig. 21(a) shows a CD4001AD device whose V_{DD} is equal to 10 volts and whose voltage output is specified at 9.5 volts. Under these conditions, the

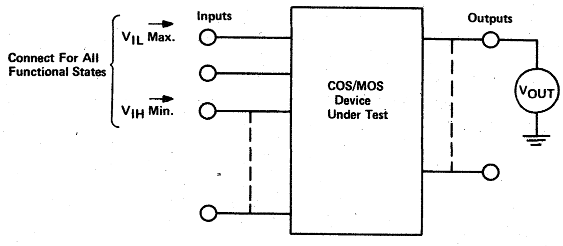

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Fig. 19 — Input-voltage-level test arrangement.

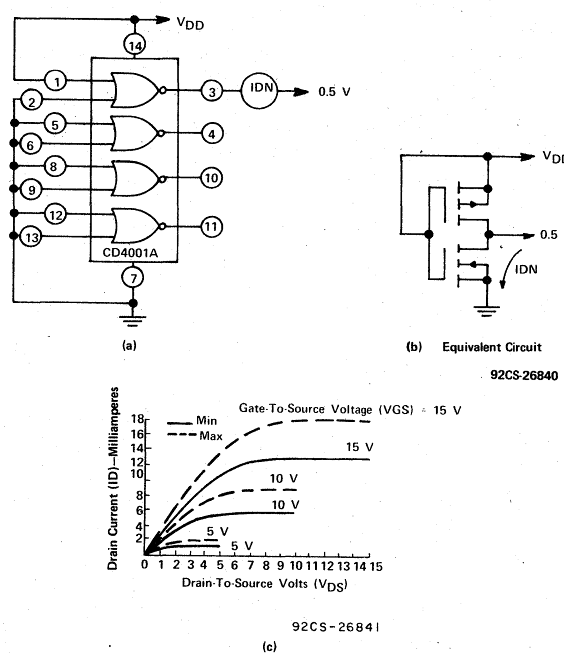


Fig. 20 — Output drive current (I_{DN}), sink-current, test arrangement.

output drive current will be a minimum of 0.25 milliampere. The amount of current that the device can source varies depending upon the voltage drop across the device (V_{DS}) for a fixed V_{GS}. p-channel drain characteristics are shown in Fig. 21 (c).

These current-voltage relationships can be verified, theoretically, by the use of the following equations.

In the triode region:

$$I_D = \frac{2K'W}{\ell}\left[V_{DS}(V_{GS}-V_{TH}) - \frac{V_{DS}^2}{2}\right] \quad 0 \leq V_{DS} \leq (V_{GS}-V_{TH})$$

In the saturated region:

$$I_D = \frac{K'W}{\ell}\left[V_{GS}-V_{TH}\right]^2 \quad 0 \leq (V_{GS}-V_{TH}) \leq V_{DS}$$

where V_{DS} = drain-to-source voltage

V_{GS} = gate-to-source voltage

V_{TH} = device threshold voltage

$K' = \frac{\mu\epsilon_o}{2t_{ox}}$ μ = effective surface mobility of the carrier in the channel

ϵ_o = permittivity of the oxide

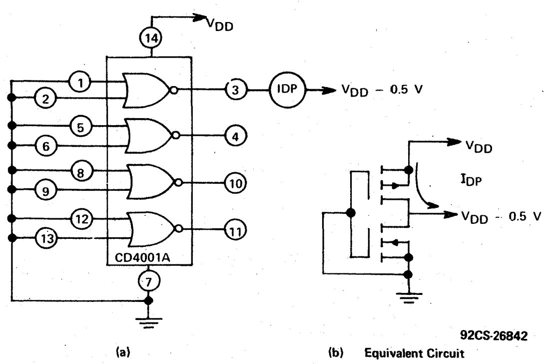
t_{ox} = oxide thickness

W = channel width

ℓ = channel length

Input Capacitance

The input capacitance of a device is measured as shown in Fig. 22. A capacitance bridge is connected between each input and V_{SS}. The capacitance is then measured after all stray capacitance has been nulled. The test is performed at a 1-MHz bridge setting. Device input capacitance is considered acceptable if the bridge reading is less than the maximum input capacitance specified on the data sheet.



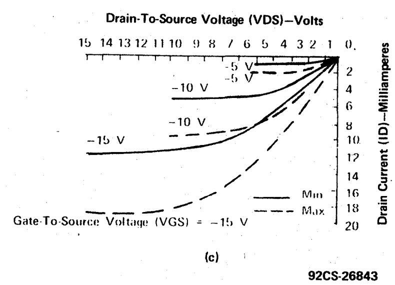


Fig. 21 — Output drive current (I_{DP}), source current, test arrangement.

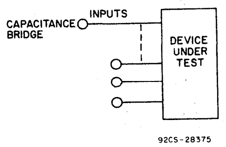


Fig. 22 – Input capacitance measurement.

DYNAMIC TESTING

Propagation Delay and Transition Times

Propagation Delay (t_{PLH}) is measured from the 50-percent point of the input pulse to the 50-percent point of the output pulse as the output goes from a low level to a high level.

Propagation Delay (t_{PHL}) is measured from the 50-percent point of the input pulse to the 50-percent point of the output pulse as the output goes from a high level to a low level.

Transition Time (t_{TLH}) is the time required for the output to make the transition from the low state to the high state (n device turns off, p device turns on). This time is measured from the 10-percent point to the 90-percent point of the output pulse.

Transition Time (t_{THL}) is the time required for the output to make the transition from the high state to the low state (p device turns off, n device turns on). This time is measured from the 10-percent point to the 90-percent point of the output pulse.

Dynamic parameters are measured at a specified load of 15 and/or 50 picofarads. The load specified is for total capacitance including stray and probe capacitance. Frequency is not a critical factor in determining switching speeds of COS/MOS devices. Testing should be done at a frequency compatible with the test set or laboratory equipment involved and must be less than the maximum operating frequency. Fig. 23 shows waveforms used in the measurement of propagation delay and transition times.

Note that certain dynamic tests, when performed on a go-no-go basis, are conducted with specified limits as test conditions and with the device outputs monitored. Parameters tested in this way include set-up times, minimum clock, reset and preset pulse widths, clock rise and fall times, maximum clock frequency, and preset and reset removal times. Parameters such as propagation delay and transition times are tested under a set of prescribed conditions so that the test yields actual characteristic data.

Maximum Operating Frequency

The maximum operating frequency, f_{CL}, is that clock input frequency above which the device will no longer perform its logical function. This frequency is determined by gradually increasing the input frequency while monitoring the output until the device no longer functions properly. The input frequency is then lowered until the device resumes correct operation. The frequency thus determined is the maximum operating frequency of the individual device.

When testing for compliance a device for which a maximum operating frequency has been specified, the maximum specified operating frequency is applied to the device while the outputs are monitored. This is a go-no-go test as opposed to a characterization test.

Fig. 24 shows a CD4013, dual D-type flip-flop, under test for maximum operating

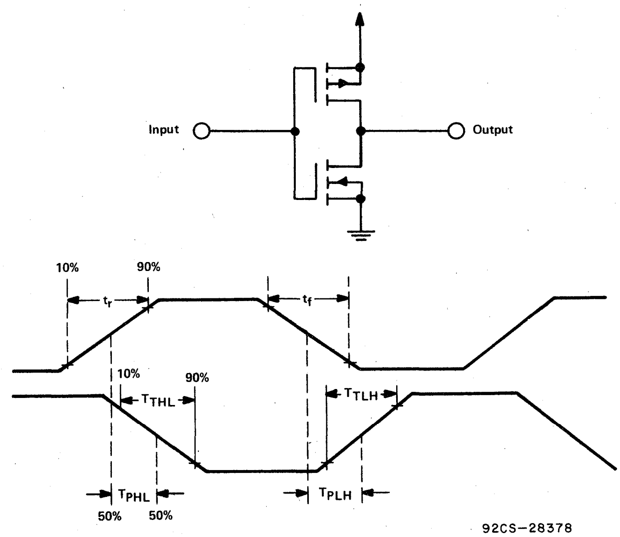
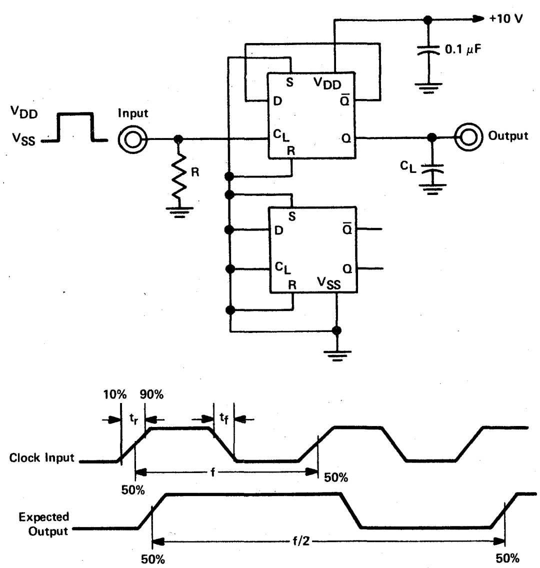


Fig. 23 – Waveforms used in the measurement of propagation delay and transition times.



Test Conditions (Per Data-Sheet Specifications*)

* Pulse-Generator Amplitude	10 V
Pulse-Generator Impedance-Matching Resistor (R)	50 ohms
*Pulse-Generator Rise and Fall Times (t_r = t_f)	20 ns
*Pulse-Generator Input Frequency (f_{CL})	7 MHz
*Load Capacity – C_L (Including Stray and Probe)	15 pF, 50 pF

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Fig. 24 – Test circuit for measuring the maximum operating frequency of a CD4013A/B.

frequency at an operating voltage of $V_{DD}-V_{SS}$ of 10 volts.

Set-Up Time

Set-up time (t_S) is the time interval during which a signal is applied and maintained at a specified input terminal before the device recognizes the presence of the specified input pulse. An example of set-up time measurement for a CD4013, Fig. 25, shows a data input which must be present for time t_S (value specified in data sheet) in order for the positive transition of the clock pulse to transmit the level at the data input to the Q output. If the data input is not present for a sufficient period of time prior to the positive transition of the clock, the previous state of the data input will be recognized and transmitted to the Q output.

When testing a device for compliance with a specified set-up time, a go-no-go test, the set-up time specified in the data sheet is used as a test condition and the output is monitored for expected operation. When characteristic data is required, the set-up time is varied until the expected output occurs.

Minimum Clock, Set, Reset, and Preset Pulse Widths

Pulse widths, t_W, are defined as the time from the point on the leading edge of the clock-pulse curve which is 50-percent of the maximum amplitude to a point on the trailing edge which is 50-percent of the maximum amplitude, Fig. 26. The minimum pulse width for the clock, set, reset, and preset inputs is that time that the pulse must be present in order for the device to recognize the presence of the pulse.

When testing a device for compliance with minimum pulse widths, a go-no-go test, the pulse width specified in the data sheet is used as a test condition and the output is monitored for expected operation. When characteristic data is required, the pulse width is varied until the expected output occurs.

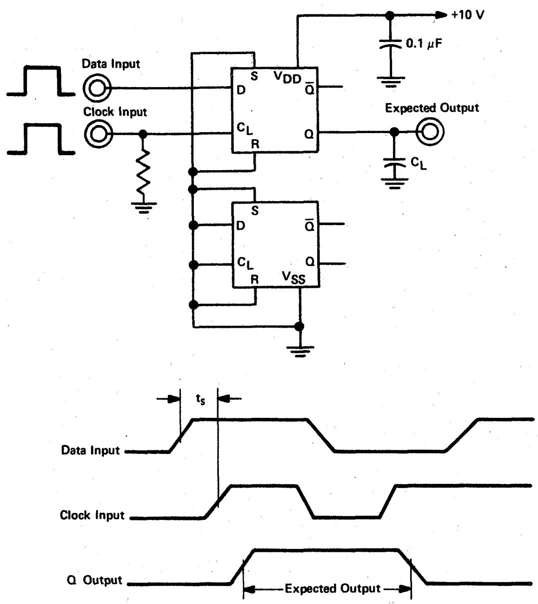
An example of minimum clock-pulse width measurement (t_{WH}) for a CD4013 at a $V_{DD}-V_{SS}$ of 10 volts, Fig. 27, shows the minimum clock-pulse width specified in the data sheet being applied to the clock input of the device under test at a frequency (f) that is less than the maximum operating frequency specified. The clock pulse is applied in one case when the data input is low and is then applied again when the data input is high. (The high and low states of the data input must be present for a time exceeding the specified set-up time.) A device that complies with the minimum clock-pulse width parameter specification will transmit the data input level to the Q output on the positive transition of the clock. Proper operation of the CD4013 can be checked by monitoring for an expected output at Q of f/2.

Maximum Clock Rise and Fall Times

The maximum clock rise and fall times (t_{rCL}, t_{fCL}) are the rise and fall times of the clock input signal (measured from 10 percent to 90 percent), above which the device is guaranteed to perform its logical function. This rise and fall time is determined by gradually increasing the clock rise/fall time while monitoring the output until the device no longer functions properly. The clock input rise and fall times are then lowered until the device resumes correct operation. The rise and fall times thus determined are the maximum clock rise and fall time of the individual device.

In testing a device for maximum clock rise and fall times to a specified limit, the maximum specified clock rise and fall times are applied to the clock input while the output is monitored. The input frequency used to perform this test must be less than the reciprocal of $2t_r$; for example, when applying the specified clock rise and fall times for a CD4013 at a $V_{DD}-V_{SS}$ of 10 volts, the maximum clock input frequency that may be used is 100 kHz.

Fig. 28 is an example of a test of maximum clock rise and fall times of a CD4013, dual flip-flop, at an operating voltage, $V_{DD}-V_{SS}$ of 10 volts.



Test Conditions (Per Data-Sheet Specifications*)

*Pulse-Generator Amplitudes	10 V
Pulse-Generator Impedance—Matching Resistor (R)	50 ohms
*Pulse-Generator Rise and Fall Times ($t_r = t_f$)	20 ns
*Load Capacitance—C_L (Including Stray and Probe)	15 pF, 50 pF
*Setup Time (t_S)	20 ns

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Fig. 25 – Set-up-time test circuit for a CD4013A.

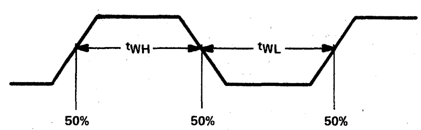

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Fig. 26 – Waveform used to define pulse widths.

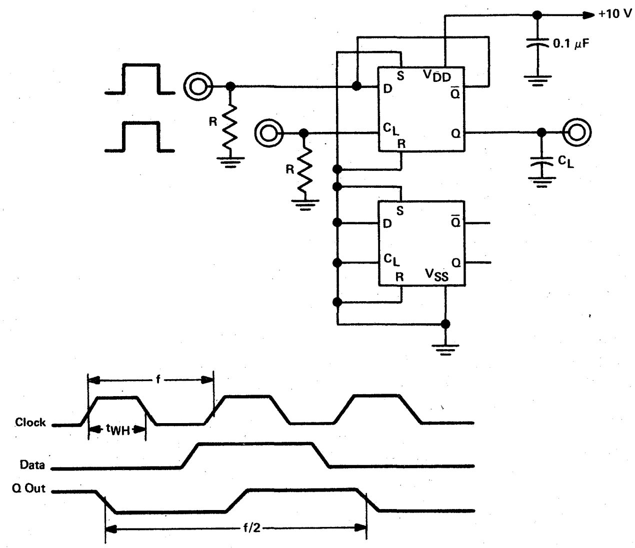
Reset, Set and Preset Removal Time

The reset, set, and preset removal time, t_{REM}, when used in reference to flip-flops, counters, and shift registers, is that time for which the reset, set, or preset pulse must be in its clock enabling state before the device can resume synchronous operation.

When a device is in the preset mode, the JAM input levels are transmitted to the Q output asynchronously. The reset state causes the Q outputs to go to a low level; the set state causes the Q outputs to go to a high level. It is generally an invalid condition to have a device in more than one asynchronous state at the same time.

In testing a device for compliance with data-sheet specifications, the removal time specified is applied at the appropriate input terminal of the device under test. When characterizing a device, the removal time is adjusted relative to the clock input such that expected operation occurs, decreased to the point where expected operation no longer occurs, and then increased until expected operation reoccurs. The time recorded at the reoccurrence of expected operations is the correct removal time (t_{REM}).

An example of a test for minimum preset-enable removal time as specified in the data sheet of a CD4029A, presettable up/down counter, is shown in Fig. 29. The JAM inputs J1, J2, J3, and J4 are hard-wired to ground (low). With the preset enable input high, the information on the JAM inputs is transmitted to the Q outputs (regardless of the state of the clock). The preset input is then set low. After a time equal to t_{REM}, the clock-pulse positive transition advances the counter and causes the Q1 output to go high. The transition of the Q1 output from the low to the high state confirms that the preset enable pulse has been removed for a sufficient time to allow the device under test to resume synchronous clocked operation.



Test Conditions (Per Data-Sheet Specifications*)

* Pulse-Generator Amplitudes	10 V
* Pulse-Generator Rise and Fall Times	20 ns
Pulse-Generator Impedance-Matching Resistor	50 ohms
* Clock-Pulse-Generator Frequency	<< Max. Operating Frequency
* Load Capacity (C_L) (Total Including Stray)	15 pF, 50 pF

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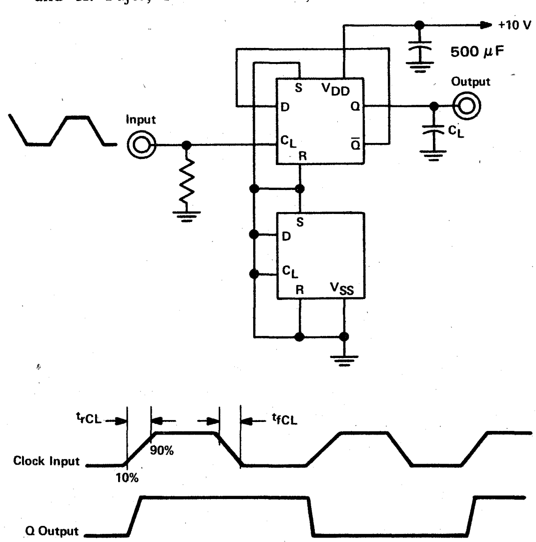
Fig. 27 – Test circuit for measuring minimum clock-pulse width in a CD4013A/B.

Reference

1. Guide to Better Handling and Operation of CMOS Devices, ICAN-6525, J. Flood and H. Pujol, RCA Solid State, 1976.



Test Conditions (Per Data-Sheet Specifications*)

* Pulse-Generator Amplitude	10 V
* Pulse-Generator Rise and Fall Times (t_{rCL}, t_{fCL})	5 µs
Pulse-Generator Impedance-Matching Resistor	50 ohms
* Pulse-Generator Frequency	100 kHz
* Load Capacity (C_L) (Total Including Stray and Probe)	15 pF, 50 pF

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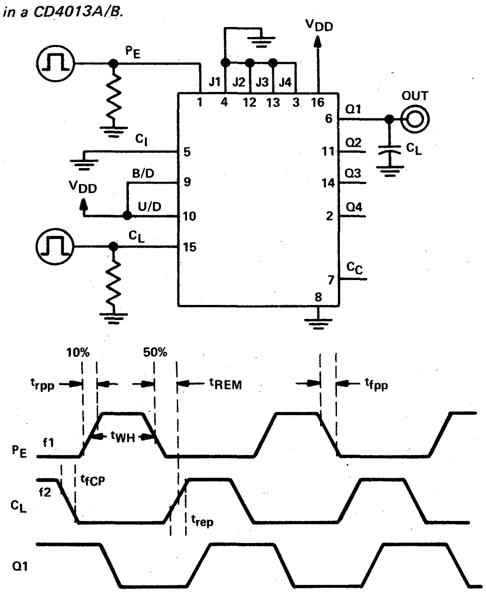
Fig.28 – Test circuit for measuring maximum clock-rise and fall time in a CD4013A/B.



Test Conditions (Per Data-Sheet Specifications)

Pulse-Generator Amplitude	V_{DD}
Pulse-Generator Rise and Fall Times ($t_{rpp} = t_{fcp}$)	20 ns
Pulse-Generator Impedance-Matching Resistor	50 ohms
Load Capacity (C_L) (Total Including Stray and Probe)	15 pF, 50 pF

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Fig. 29 – Test circuit for measuring preset-enable removal time in a CD4029A/B.

A Basic Selection Guide to Digital Counters

by J. E. Gillberg

The binary ripple counter has emerged as a major building block for today's digital circuit designs primarily because it offers a large amount of information for a set number of bits. In addition, it is simple, requiring no decoding from the counting stages, and its dynamic power consumption is small. This Note discusses these advantages, compares the binary ripple counter with the Johnson decade counter and the BCD counter, and discusses the selection of the most suitable counter for specific applications.

Design Features

The functional diagram for a COS/MOS 7-stage binary counter type CD4024 is given in Fig. 1. The CD4024 superseded the CD4004 which was the first counter available in the CMOS family of digital devices. This counter is a simple basic design, comprising a series of toggle flip-flops in which the clock input of one flip-flop is connected to the Q output of the previous flip-flop. No additional gating is necessary to perform the binary count. The buffer converter connected to the $\bar{Q}$ output of each flip-flop stage enhances the current drive without adversely affecting counter speed. Fig. 2 is a detailed diagram of a single master-slave flip-flop used as the sequential memory element in the CD4024, as well as in most static counters.

Two other counters that have found acceptance as digital building blocks are the CD4017, a decade counter/divider using the Johnson decade counter configuration, and the CD4518, a BCD up-counter. These devices provide alternatives to the digital system designer and have advantages and disadvantages, as does the binary ripple counter.

The CD4017 consists of a 5-stage Johnson decade counter and an output decoder which converts the Johnson binary code to a decimal number. Functional and logic diagrams are given in Fig. 3 for this device. The decade counter includes "anti-lock" gating to assure proper counting sequence. Because the Johnson counter does not use every available combination of outputs, it is possible for the counter to enter an "illegal" mode of operation at power turn-on or as the result of incoming noise. The anti-lock gating forces the counter back into "legal" operation. For many applications, the disadvantage of the unused logic states, necessitating the use of additional counter stages, is compensated for by its high-speed operation, 2-input decimal decode gating, and spike-free decoded outputs.

The CD4518 BCD synchronous counter requires extra gating to determine what state the counter should be clocked into at the next incoming pulse. Its functional and logic diagrams are given in Fig. 4. Its binary coded decimal output makes it a good choice for many applications where there is machine-to-person interface.

The absence of extra gating in the binary ripple counter, however, allows maximum information density and, therefore, provides a significant advantage over the other two types.

Power Consumption

The power consumption of any counter depends on the input and output capacitance of the counter, its operating voltage, and the operating frequency. This relationship is expressed by

$$P = CV^2f$$

where P is the power consumption in watts, C the load capacitance in farads, V the operating voltage in volts, and f the frequency of operation in hertz. This expression can be used as a design guide to the power consumption of a circuit when more specific data is not available. The actual power consumption of an IC, however, may vary ± 25 percent from the value calculated.

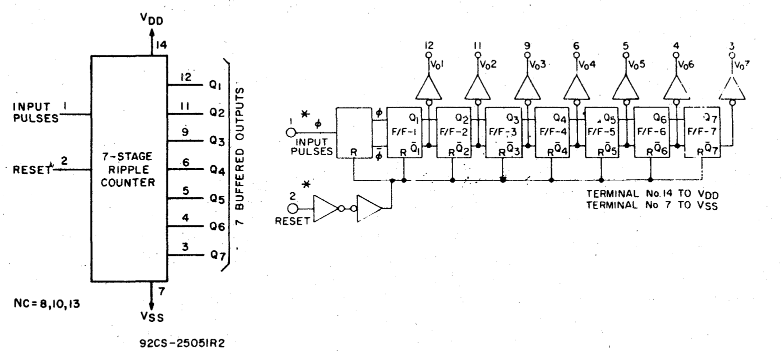


Fig. 1 - Functional and logic diagrams for a COS/MOS 7-stage binary counter type CD4024.

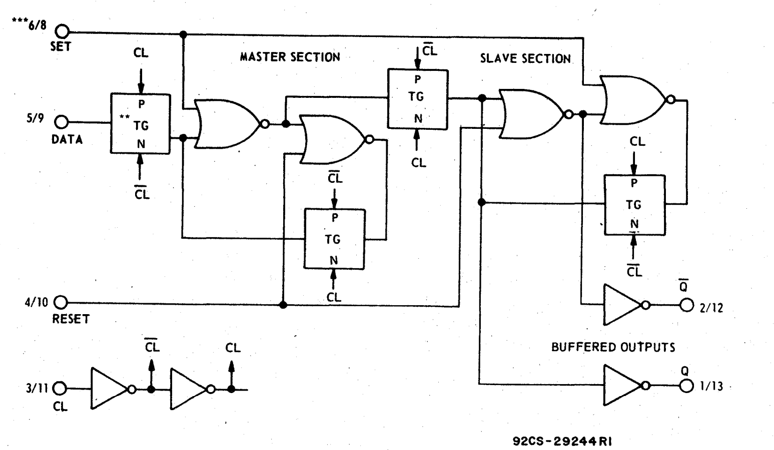


Fig. 2 - Detailed diagram of master-slave flip-flop, the sequential memory element of most static counters including the CD4024.

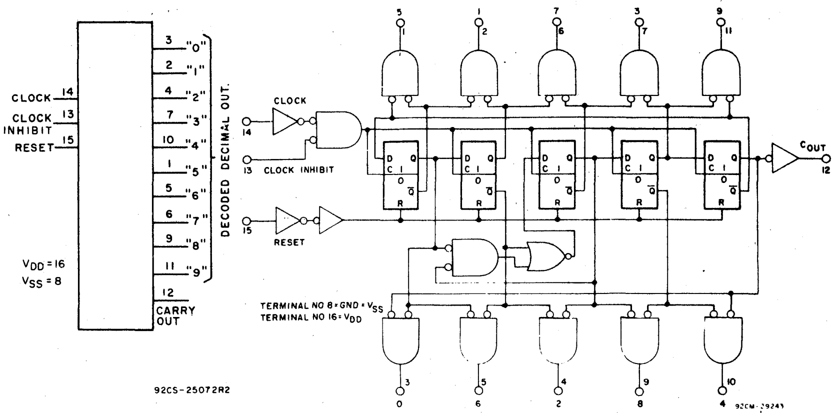


Fig. 3 - Functional and logic diagrams for 5-stage Johnson decade counter type CD4017.

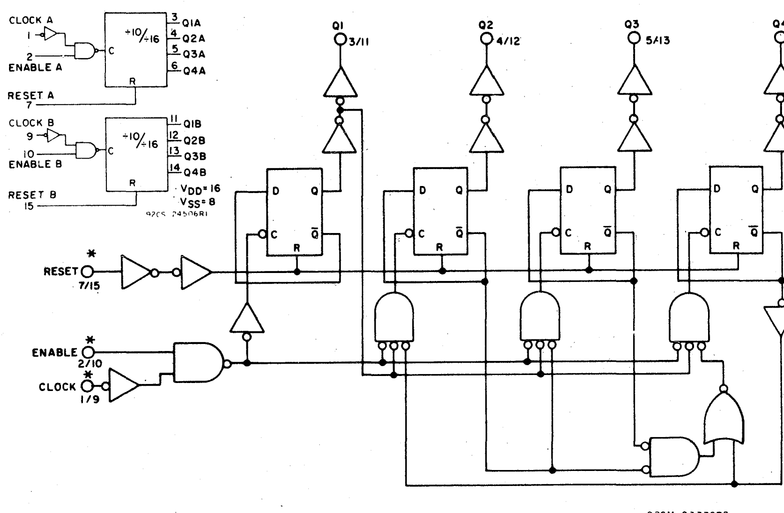


Fig. 4 - Functional and logic diagrams for BCD counter type CD4518.

If it is assumed that the input capacitance of the COS/MOS gate is small compared to the output load capacitance, it can be shown that the power consumption of the binary ripple counter is not too different from that of the other counters. With the CD4013 Quad D Flip-Flop, shown functionally in Fig. 5, used as the example and the dissipation characteristics curves for this device in Fig. 6, one can calculate the power dissipation of a divide-by-sixteen binary ripple counter and compare it to that of a Johnson counter.

The timing diagram given in Fig. 7 shows that each toggle flip-flop in a binary system is actually a divide-by-two system. The divide-by-sixteen counter would require ($16 = 2^4$) four flip-flops. At a clock frequency of 4 MHz, a V_{DD} of 10 volts, and an output capacitance of 15 pF, this 4-stage network would operate at the following frequencies and, from Fig. 6, dissipate the indicated power:

Stage 1	2×10^6 Hz	2.3×10^3 μW
Stage 2	1×10^6 Hz	1.7×10^3 μW
Stage 3	0.5×10^6 Hz	1.0×10^3 μW
Stage 4	0.25×10^6 Hz	0.5×10^3 μW

Total Power 5.5×10^3 μW = 5.5 mW

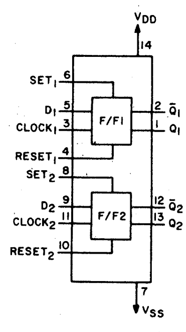


Fig. 5 - Functional diagram of dual D flip-flop type CD4013.

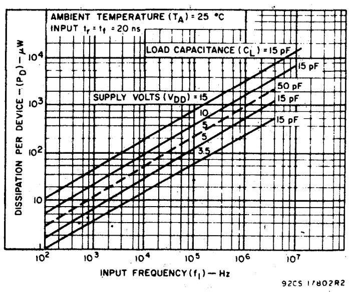


Fig. 6 - Dissipation characteristics curves for type CD4013.

For a Johnson counter, which operates by feeding back the inverted output of the final stage, the number of stages utilizing the CD4013 flip-flop needed for a divide-by-sixteen counter is eight. The outputs are changing at a rate of

$$4 \times 10^6 \text{ Hz} \div 8 = 0.5 \times 10^6 \text{ Hz}$$

Each flip-flop at this frequency and at an operating voltage of 10 volts and an output load of 15 pF would, from Fig. 6, dissipate approximately 1.0×10^3 µW. The total dissipation for the eight flip-flops, therefore, would be $8 \times 1.0 \times 10^3$ µW = 8.0 mW.

This comparison shows that the power dissipation of these two systems is fairly close in value and should not be the major deciding factor as to which system to use in a specific application.

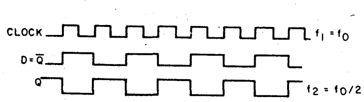


Fig. 7 - Timing diagram for divide-by-two flip-flop.

Information Density

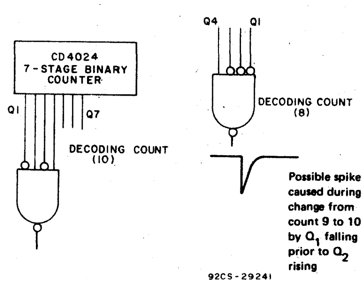
The most significant advantage of binary counters is the amount of information which can be realized from a given number of bits. A comparison of a binary 12-bit system with BCD and Johnson counter 12-bit systems shows that the binary system has 4096 separate states, the BCD system has 1000 separate stages, and the Johnson system has 24 separate states.

In a 12-bit system the binary counter is by far the most compact. In systems using a larger number of bits this advantage is even greater and is becoming increasingly important as manufacturers develop MSI and LSI devices. No longer is the constraint on a design the pellet size, but rather the number of output pins the design uses.

In a system where the goal is a specific output frequency and where the input frequency is variable, the binary ripple counter is and has been the choice of many designers. An excellent example is the design technique usually used in digital clocks and watches. An output of 1 Hz is obtained by counting down from a typical 4.194-MHz oscillator or a 32.768-kHz oscillator using the appropriate number of binary stages.

Device Selection

Although the binary counter has advantages, it does have the handicap of interfacing a non-binary world. It is difficult to decode accurately a non-binary count from a binary counter because a complex decoding scheme is needed and because the possibility of decoding spikes is increased. As shown in Fig. 8, a binary counter needs many external gates for decoding purposes. In addition, to change



	Q_4	Q_3	Q_2	Q_1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0

Fig. 8 - Typical external gate required by binary counter for decoding; spike possibility caused by non-simultaneous bit change, and, counting sequence requiring simultaneous bit change.

from count 9 to count 10, two bits must change simultaneously. Consequently, if one bit changes prior to the second, a false count of 8 or 11 could be decoded.

To avoid this kind of "glitch" possibility the Johnson counter was designed. In the Johnson counter only one bit is changing at a time, as shown in Fig. 9. Decoding of the Johnson counter with one inverter and one two-input gate can always be accomplished by decoding a 1;0 or 0;1 state between the two appropriate outputs. In addition, because only one bit is changing when the counter moves from one count to the next, no decoding glitches will develop from this decoding network.

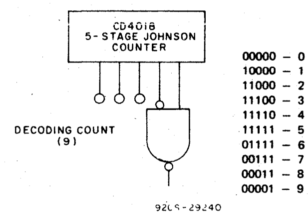


Fig. 9 - External gate required by Johnson counter; counting sequence requiring only one bit change at a time.

One disadvantage of both the binary and the Johnson counters is the difficulty of interfacing a decimal world. This difficulty instigated the development of the binary-coded decimal system. In the BCD system, by grouping four bits into each single decimal number, the actual count becomes much easier for human interface.

By way of summary, **binary counters**, because of their high information density, low power consumption, and relative simplicity, are well suited for applications such as industrial timers, watch or clock operation, binary arithmetic systems, and microprocessor systems.

Johnson counters, because of their decoding ease for any given count, are well suited for industrial controls, sequencers, low divide-by-n decoding, and programmable divide-by-n counters.

BCD counters, because of their ease of interface for human control, are well suited for programmable divide-by-n counters, counting systems for seven-segment readouts, industrial controls, and frequency synthesis.

ICAN-6558

Understanding Buffered and Unbuffered CMOS Characteristics

by R. E. Funk

INTRODUCTION

Both buffered and unbuffered CMOS B-series gates, inverters, and high-current IC products are available from RCA; each product classification has application advantages in appropriate logic-system designs. Recently, many CMOS suppliers have been concentrating on promoting buffered B-series products with applications literature focusing on the attributes and use of the buffered types. This practice has left an imbalance in the understanding and application of **both** buffered **and** unbuffered gates and, in many instances, customers are not using unbuffered products when they are the best for the intended application. This Note narrows the misunderstandings involved in this issue by presenting and discussing the relative merits of the buffered and unbuffered CMOS devices.

Background

Historically, most CMOS gates, inverters, and high-current IC products were unbuffered, and exhibited good logic-system performance, speed, noise immunity, and quasi-linear characteristics in a wide variety of applications. As the scope of CMOS products broadened and more manufacturers entered the scene, buffered gate and inverter products were brought out by RCA and others. While RCA confined initial buffered products to new OR and AND functions, other manufacturers introduced buffered NOR and NAND gates having the **same** generic 4000A-series designations as the original widely-used unbuffered gates. Many users were surprised by the non-interchangeability of the devices in applications where speed, noise immunity, output impedance, and linear gain-bandwidth characteristics were critical. It is of immense benefit to CMOS users to have available the definitions and designations of **both** buffered and unbuffered B-series CMOS devices as determined by the JEDEC CMOS Standardizing Committee under the cognizance of the JC40.2 JEDEC Committee of EIA. The official JEDEC definitions are repeated below along with detailed explanations and examples. Comparison of user-oriented characteristics and the use of buffered and unbuffered gates are also reviewed.

Definitions

Buffered CMOS–A CMOS device for which the output on impedance is independent of any and all valid input logic conditions, both preceding and present, is said to have a buffered output or to be a buffered CMOS device. All such products are designated by the suffix B.

Unbuffered CMOS–Products that meet B-series specifications except that the logical outputs are not buffered and the V_{IL} and V_{IH} specifications are 20 percent and 80 percent of V_{DD}, respectively, are marked with the UB designation, such as (including, but not limited to):

4000UB	4025UB
4001UB	4007UB
4002UB	4009UB
4011UB	4041UB
4012UB	4049UB
4023UB	4069UB

The official JEDEC definitions are primarily applicable to gates, inverters, and high-current (inverting) drivers such as the specific UB types shown above. Non-inverting gates and drivers as well as all MSI and LSI B-types are by definition B types. There are special analog I/O types that are also included as B types since they conform to all B standards except that they have special analog I/O circuitry. Examples of parts that have no buffered or unbuffered significance are:

4016B	4053B
4046B	4067B
4051B	4097B
4052B	4066B
	4511B
	4528B

RCA will make available both types of CMOS gates. Logic examples of the buffered and unbuffered 2-input NOR gate are shown in Fig. 1. Note that the buffered logic can be implemented by either a 2-input NOR function followed by two inverters or by two input inverters followed by the 2-input NAND gate and an output buffer. RCA uses the latter logic configuration, which has the advantage of optimizing device noise immunity by negating the effect of stacked devices at the input. This characteristic is

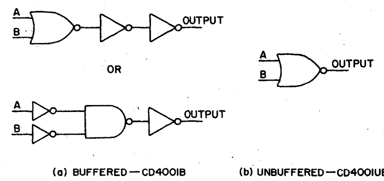


Fig. 1 – Examples of the buffered (CD4001B) and unbuffered (CD4001UB) 2-input NOR gate.

especially significant for 3- or 4-input gates where three or four PMOS or NMOS transistors are stacked in series at the input. In this case, the inputs have an effective offset in threshold and reduced input noise immunity.

Fig. 2 is a schematic representation of the RCA buffered and unbuffered 2-input NOR gates. The improved 4-diode-input gate-oxide protection circuit is shown at the inputs.

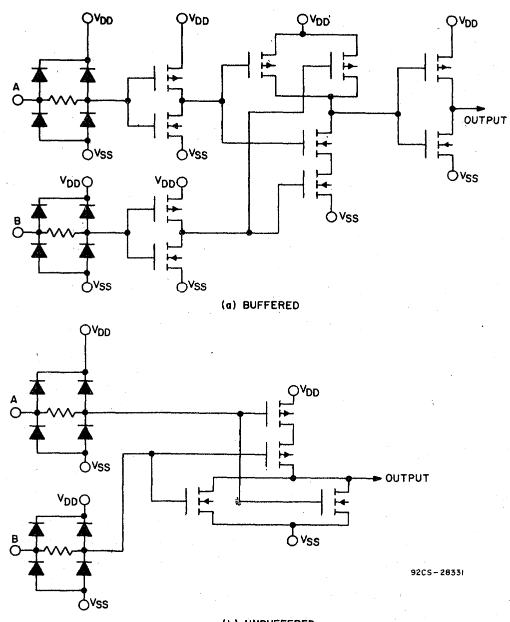


Fig. 2 – Schematic diagrams of the buffered and the unbuffered 2-input NOR gate.

Examples

Examination of the dc performance characteristics of both the buffered and unbuffered 2-input NOR gate reveals the two electrical characteristics, output impedance and noise immunity, by which the types are differentiated by the JEDEC standard specifications:

Output Impedance

–Buffered–Fig. 3 depicts the buffered output stage and shows the MOS transistor as switched on with a channel resistance R; R is the **same** value for the n-switch closed or the p-switch closed.

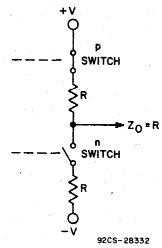


Fig. 3 – Constant output impedance of a buffered gate.

–Unbuffered–Fig. 4 depicts the unbuffered 2-input-gate p- and n-channel MOS switches and appropriate on-channel resistances. Note that the two stacked p-channel switches are designed for an on resistance of R/2 so that the output impedance is R when both the logic inputs are low, Fig. 4(b). In Fig. 4(a) the output impedance is R to the negative supply terminal (usually ground) for an input logic state of 1, input high. Fig. 4(c) shows the condition when the unbuffered gate has an output impedance of R/2 for both logic inputs high. Hence the variable output impedance of the unbuffered gate. For a 4-input gate, this variable is R to R/4! The maximum output resistance of RCA buffered or unbuffered gates is R. Thus, minimum I_{OL} and I_{OH} specifications for buffered and unbuffered gates are identical.

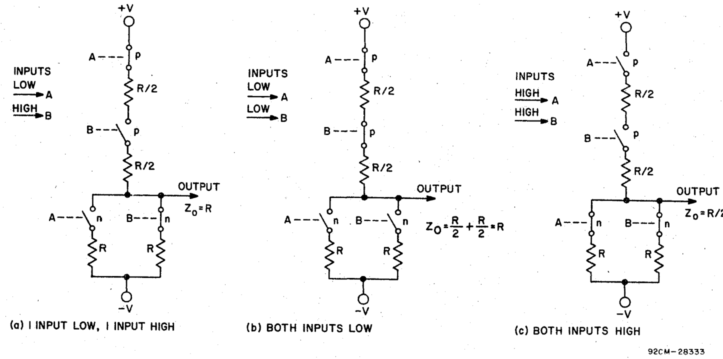


Fig. 4 – Variable output impedance of an unbuffered 2-input NOR gate. The resistors represent the on impedance of a p- or n-channel MOS transistor.

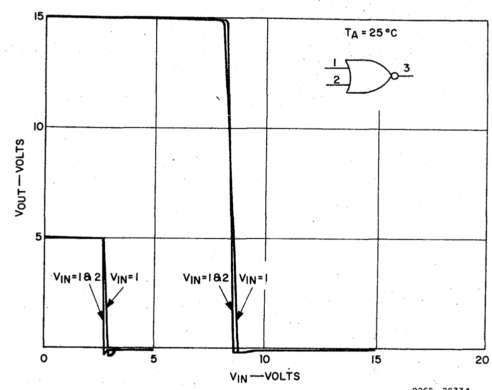


Fig. 5 – Voltage transfer characteristics of a buffered 2-input NOR gate (CD4001B).

Noise Immunity

The second JEDEC-defined difference between the buffered and unbuffered CMOS gates (or inverters) is the difference in input noise-immunity characteristics.

–Buffered–The buffered 2-input NOR gate voltage-transfer characteristics, Fig. 5, are squared because of the gain of three CMOS stages from input to output. Fig. 5 shows that noise voltage inputs of ±1.5 V at V_{DD} = 5 V and ±4 V at V_{DD} = 15 V will have little discernible effect on the output voltage; i.e., noise immunity for **all** logic states is optimally high as is noise margin: 1 volt at V_{DD} = 5 V and 2.5 V at V_{DD} = 15 V.

–Unbuffered–Fig. 6 shows the rounded voltage-transfer characteristics of the 2-input unbuffered NOR gate. Also evident is the shift in the transfer curve for the different logic input states. Compare these curves to those of Fig. 5 and the effects of the non-buffered inputs as well as the gain differences are evident. The rounded characteristics require a noise-immunity specification of ±20% of V_{DD} at 5, 10 and 15 V as well as a reduced noise margin: 0.5 V at V_{DD} = 5 V and 1.0 V at V_{DD} = 15 V.

The above definitions use gate characteristics as illustrative of the JEDEC definitions for buffered and unbuffered characteristics relative to variable output impedance and noise-immunity performance. Inverters and high-current drivers may also be defined as buffered (B) types or unbuffered (UB) types by virtue of the squared or rounded transfer characteristics of Figs. 3 and 4, respectively. Even though both types have a single NMOS and single PMOS output transistor, the rounded transfer characteristic of the unbuffered inverters makes them UB types by virtue of:

1. Reduced noise-immunity performance where the 20% rating is applicable.
2. Varying output impedance as a function of input voltage change along the rounded portion of the transfer curve.

COMPARISONS

Table I shows the qualitative comparisons of user-oriented performance characteristics of buffered and unbuffered CMOS gates, inverters, or drivers. Table II is a quantitative comparison of the key performance characteristics with explanations as follows:

Propagation Delay–Delays shown are applicable to RCA 2-, 3-, and 4-input NOR and NAND gates.

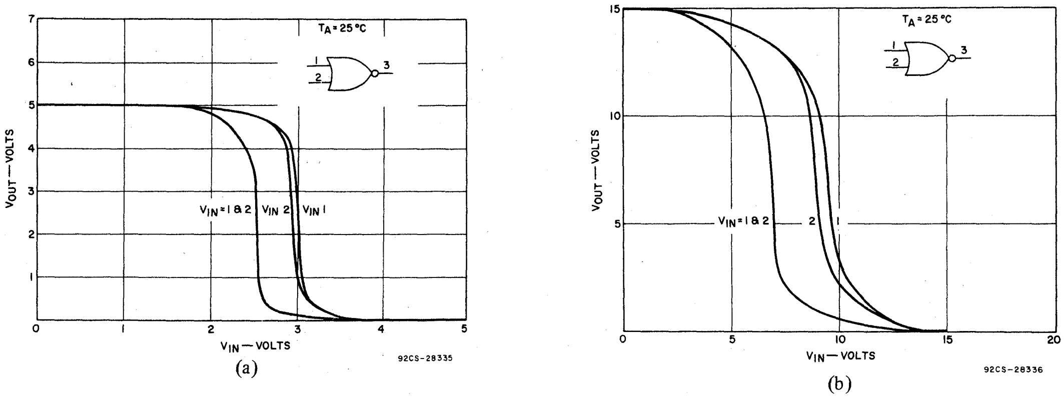


Fig. 6 — Voltage transfer characteristics of an unbuffered 2-input NOR gate (CD4001UB) with output voltages of 5 and 15 volts.

Table I—Comparison of Buffered and Unbuffered Gate Characteristics

Characteristic	Buffered	Unbuffered
Propagation Delay	Slow	Fast
Noise Immunity/Margin	Excellent	Good
Output Impedance and Output Transition Time	Constant	Variable
AC Gain	High	Low
Output Oscillation for Slow Inputs	Yes	No
Input Capacitance	Low	High

Table II—Characteristics of Buffered and Unbuffered Gates

	Buffered Gates	Unbuffered Gates
Typical Propagation Delay		
$V_{DD} = 5$ V, $C_L = 50$ pF	150 ns	60 ns
$V_{DD} = 10$ V	65 ns	30 ns
$V_{DD} = 15$ V	50 ns	25 ns
Noise Immunity	30% of V_{DD} at 5 and 10 V 27% at 15 V	20% of V_{DD} at 5, 10, and 15 V
Noise Margin $V_{DD} = 5$ V	1 V	0.5 V
10 V	2 V	1.0 V
15 V	2.5 V	1.0 V
Typical Output Impedance		
$V_{DD} = 5$ V, $V_O = \pm 0.4$ V		
2-Input Gate	400 ohms	200-400 ohms
3-Input Gate	400 ohms	133-400 ohms
4-Input Gate	400 ohms	100-400 ohms
Typical Output Transition Time		
$V_{DD} = 5$ V, $C_L = 50$ pF		
(2-, 3-, 4-Input Gates)	100 ns	50-100 ns
AC Gain $V_{DD} = 10$ V	≈68 dB	≈23 dB
AC Bandwidth $V_{DD} = 10$ V	280 kHz	885 kHz
Output Oscillation For Slow Inputs	Susceptible For $t_r, t_f > 1$ ms	Not Susceptible For t_r, t_f to 100 ms
Typical Input Capacitance		
Average	1-2 pF	2-3 pF
Peak	2-4 pF	5-10 pF

Noise Immunity—Table III shows the detailed input-voltage data-sheet specifications for buffered and unbuffered gates. From these test conditions the user-oriented noise-immunity and noise-margin data of Table II are derived. Also refer to Figs. 5 and 6 for the voltage-transfer characteristics that illustrate the reason for the different input-voltage-specification requirements for buffered and unbuffered devices.

Output Impedance—Refer to Figs. 3 and 4 and accompanying descriptions of the constant output impedance of buffered gates and the variable output impedance of unbuffered gates. Note that **both** buffered and unbuffered RCA 2-, 3- and 4-input gates are designed to meet the same maximum output impedance; output current ratings (I_{OL} and I_{OH}) have the same minimum limit on RCA data sheets.

Output Transition Time—The time required for a CMOS output to transfer high or transfer low is constant for buffered gates but varies according to input logic states for unbuffered gates. Output transition time varies as a function of the driving source resistance of the output, which is state dependent as indicated in Fig. 4, as well as the device output capacitance, which is dependent on both device size and input logic state. Because of variable output capacitance, output-transition-time variations are not a linear function of output resistance. As Table II shows, RCA 2-, 3- and 4-input unbuffered gates exhibit a net 2-to-1 difference in output transition time even though the output resistance has a net 4-to-1 variation for the 4-input gate.

Table III—Input-Voltage Specifications

Characteristic		V_O	V_{DD}	Limit Min.	Limit Max.	Units
Input Voltage Low (V_{IL})		4.5	5	–	1.5	Volts
		9	10		3	
	B	13.5	15	–	4	
	UB	4.5	5	–	1	
		9	10	–	2	
		13.5	15	–	2.5	
Input Voltage High (V_{IH})		0.5	5	3.5	–	
		1	10	7	–	
	B	1.5	15	11	–	
	UB	0.5	5	4	–	
		1	10	8	–	
		1.5	15	12.5	–	

Notes:
1. Noise-immunity voltage is the V_{IL} or V_{IH} Specification Limit.
2. Noise-margin voltage is computed as follows:

$$\text{Noise-Margin Voltage} = V_{IL} - (V_{DD}-V_O) = (V_{DD}-V_{IH}) - V_O.$$

AC Gain and Bandwidth—CMOS linear-mode gain was measured for both the buffered and unbuffered RCA 2-input NOR gate by means of the test circuit of Fig. 7. Fig. 8 shows typical linear-mode gain difference between buffered and unbuffered RCA 2-input NOR gates. While absolute performance depends on device type (inverters; 2-, 3-, 4-input gates) and test configurations, Fig. 8 defines the approximately 3-to-1 difference in linear-mode performance between buffered and unbuffered gates.

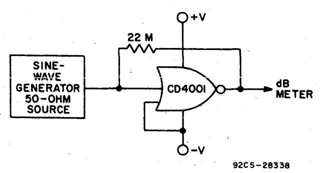


Fig. 7 — Linear-gain test circuit.

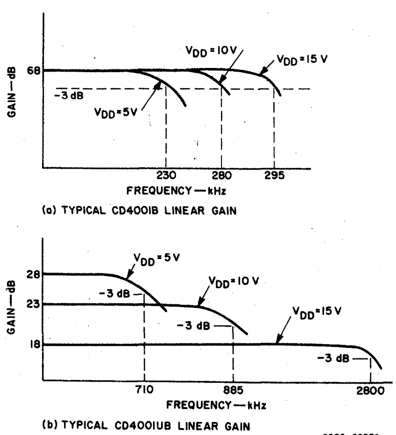


Fig. 8 — Typical linear-mode gain of buffered and unbuffered 2-input NOR gate.

Output Oscillation for Slow Inputs—The high linear-mode gain of buffered CMOS devices can lead to undesirable oscillation at outputs when input ramps are in excess of approximately 1 millisecond duration. Fig. 9 illustrates this effect when approximately 1 to 2 millivolts of ac noise within the device bandwidth on the input signal are amplified through the device and tend to develop a few cycles of oscillation between the positive and negative rails under 5-volt operation. In contrast, unbuffered gates do not tend to oscillate unless a noise voltage of 200 to 300 millivolts were present within the bandwidth of the device. An input ramp of up to 100 milliseconds duration did not create oscillation in laboratory tests of RCA unbuffered gates.

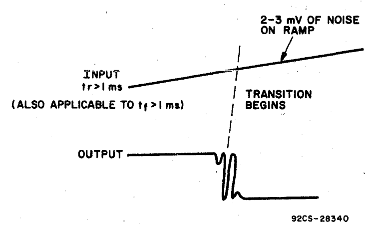


Fig. 9 — Buffered output oscillation for a slow input.

Input Capacitance—Figs. 10 and 11 show the dynamic input capacitance of the RCA buffered and unbuffered 2-input NOR gates, respectively. The large MOS transistor geometry of the unbuffered NOR gate is responsible for the higher peak input capacitance (Miller effect) in the linear switching range. The longer dwell in this linear region also tends to broaden the Miller capacitance, and therefore increases the effective average input capacitance. Buffered gates and inverters are rated at a maximum input capacitance of 1 unit load (7.5 picofarads—JEDEC standard); unbuffered gates and inverters are rated at 2 unit loads (15 picofarads maximum). High-current unbuffered drivers, such as the CD-4049UB, are rated at 3 unit loads (22.5 picofarads maximum).

Applications Guidance

Table IV summarizes preferred application areas for both buffered and unbuffered RCA B-series IC products. This information is based on the buffered and unbuffered CMOS device characteristics listed in Table II combined with the author's experience and familiarity with the application areas indicated. The information given is general guidance to allow the designer to key in on the specific performance characteristics of either device type. The data provided in this Note are derived from RCA standardized B and UB products whose circuit designs were implemented to match performance between UB and B gate types as closely as possible. For example, device sizes were selected to assure matched output drive. In addition, the process and layout rules followed in B and UB designs of RCA product are identical, as is the use of improved gate-oxide protection circuitry for B and UB product.

RCA Gate, Inverter, and Driver Products

Table V is a current list of SSI (small scale integrated) B and UB products presently in production by RCA. Refer to RCA product guides and the Databooks for detailed product information.[1]

References

1. COS/MOS Digital Integrated Circuits, Product Guide, COS-278E, 1976.
   RCA Integrated Circuits, Databook, SSD-210, 1976.

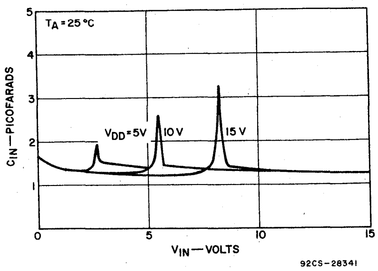


Fig. 10 – Input capacitance of a buffered 2-input NOR gate (CD4001B).

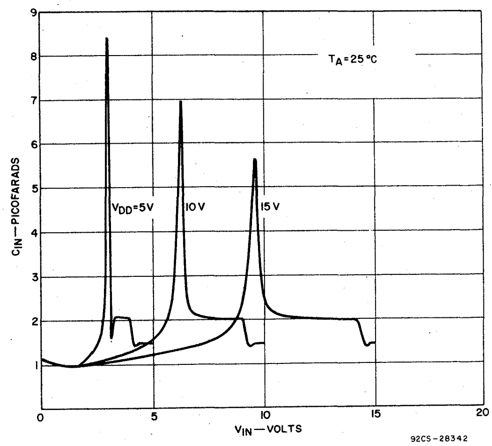


Fig. 11 – Input capacitance of an unbuffered 2-input NOR gate (CD4001UB).

Table IV–Applications of Buffered and Unbuffered CMOS Gates and Inverters

Application	Buffered	Unbuffered
High-Speed Systems	–	Preferred
High-Noise Environments, Low-Speed Systems	Preferred	–
Ultra-Low-Frequency Systems Inputs <1 kHz sine wave or ramps with t_r,t_f >1 ms* excluding Schmitt Triggers	–	Preferred
Gate Applications Requiring Constant Output Impedance Such as D/A R-2R Conversion	Preferred	–
High-Freq., Moderate Gain, Linear Amplification	–	Preferred
Low-Freq., High Gain, Linear Amplification	Preferred	–

*Applies to gates of inverter designs of Astable or Monostable multivibrators with T > 1 millisecond.

Table V–RCA COS/MOS Buffered and Unbuffered Gate, Inverter, and Driver Types

Buffered	Unbuffered
CD4000B	CD4000UB
CD4001B	CD4001UB
CD4002B	CD4002UB
CD4010B	CD4007UB
CD4011B	CD4009UB
CD4012B	CD4011UB
CD4023B	CD4012UB
CD4025B	CD4023UB
CD4050B	CD4025UB
CD4068B	CD4041UB
CD4071B	CD4049UB
CD4072B	CD4069UB
CD4073B	
CD4075B	
CD4078B	
CD4081B	
CD4082B	

Radiation Resistance of the COS/MOS CD4000A and CD4000B Series

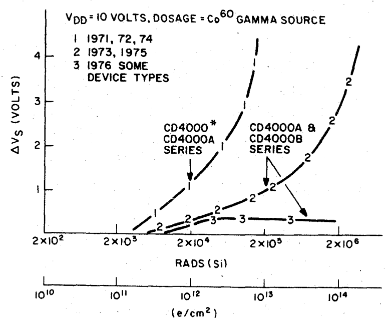
by M. N. Vincoff

Complementary MOS (COS/MOS) integrated circuits possess many advantages which recommend their use in radiation-susceptible space and military environments. Several of the most significant of these advantages are: ultra-low standby-power consumption, high noise immunity,[1] extremely high packaging density, and inherently high reliability.[2,3] These advantages, along with the improved radiation resistance of the 1975 and 1976 RCA CD4000A and CD4000B series over the previous CD4000 and CD4000A series described in earlier radiation studies,[4] exhibit the maturity reached by the MOS technology since 1969.

A number of studies of the radiation resistance of complementary MOS devices by JPL, NASA, NRL and various companies in the space industry have revealed two areas of prime concern.[5, 6] The first, **permanent** radiation exposure, as experienced in a space-satellite environment, causes a shift in threshold or switching voltage, which could result in increased leakage current, I_L. The second, **transient** radiation exposure, as experienced in an atomic environment, causes the output-voltage levels to respond to a pulse of ionizing radiation; this effect could change the state of the logic circuitry and require resetting of that circuitry for proper equipment or system operation.

Permanent-Radiation Resistance

The CD4000 series was resistant to permanent radiation levels of 2 x 10^4 rads (approximately 10^{12} e/cm^2) in 1971 and 1972. In 1973, the RCA CD4000A-series devices without special processing were found to be resistant to radiation levels up to 2 x 10^5 rads (approximately 10^{13} e/cm^2), as shown in Fig. 1.[4] In this figure the change in switching voltage V_S was plotted as a function of dose; the value of V_S was calculated from the average value of V_{TN} and V_{TP} for the devices mentioned. In 1974 a minor change was made to the process and the radiation resistance was reduced to the 1971 – 1972 level. In late 1974 and early 1975 a JPL/NASA contract study resulted in a second change to the process (gate-oxide area); the change achieved a repeated radiation-resistance level of 1 x 10^5 rads (Si). This level of radiation resistance is presently provided on Class A parts having a "Z" designation after the part number.



*POSITIVE BIAS APPLIED 100% OF THE TIME 92CS-22496R1

Fig. 1 – Permanent radiation resistance of CD4000-, CD4000A- and CD4000B-series devices.

Product with this designation is tested on a lot-sampling basis using a Gamacell-200 Co-60 radiation source. Latest radiation-process improvements and resultant production studies indicate that some 1976 product exhibits radiation-resistance levels up to and beyond 1 x 10^6 rads (Si). RCA expects to have production CD4000A and B series product available to 1 x 10^6 rads (Si) in 1977.

The new radiation level of the CD4000A and B series represents a significant improvement over the previous CD4000A series. In addition, with minimal shielding (for example, 1/16-inch of aluminum) the CD4000A or B series can be used in applications with levels of radiation up to 2 x 10^6 rads (approximately 10^{14} e/cm^2).

Transient-Radiation Resistance

The resistance of the latest CD4000A and B series (1975 and 1976) to transient radiation is expected to be better than that of the past CD4000A series, which should withstand pulses of radiation in the range of approximately 10^9 to 10^{10} rads/s.[7]

Design Considerations

The resistance of the CD4000A- and B-series devices to either permanent- or transient-radiation exposure can be increased by providing either minimal shielding in the equipment enclosure containing the devices or by locating the devices deep within the equipment. In any case, the action taken will depend on the constraints dictated by the radiation environment imposed by the system or program. Each application must be tested and the results analyzed with the data in this Note as criteria. Test items to be considered are radiation environment, which will vary greatly depending on dosage rate; time of exposure; amount of normal shielding; distance of the device from the radiation source; shielding afforded by the atmosphere; power-supply voltage selection; and switching cycles used during exposure. For example, consider the effects of permanent radiation on two spacecraft in 90-degree orbits at 600 and 1500 nautical miles from the earth, respectively. The dose-depth is determined as shown in the curves of Fig. 2.

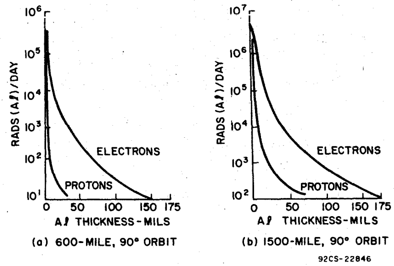


Fig. 2 – Dose-depth curves for trapped electrons and protons in spacecraft in orbit.

In these curves the dose in rads (Al)/day is plotted as a function of the thickness of spacecraft aluminum required to shield the devices from trapped electrons and protons.[5]

Conclusion

The RCA COS/MOS CD4000A and B series exhibit improved radiation resistance over the previous CD4000A series, and operate well in many applications in which permanent and transient radiation effects are factors. When stringent radiation requirements are imposed, additional shielding can be employed to increase the radiation life of COS/MOS CD4000A- or B-series devices to any desired level, i.e., to make their radiation resistance equivalent to that of bipolar devices.[6,8]

Reference

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13 Poch, W.J., and Holmes-Siedle, A.G., "The Long-Term Effects of Radiation on Complementary MOS Logic Networks", IEEE Transactions on Nuclear Science NS-17 (6), Dec. 1970 (covers CD4000 series).

14. King, E.E., Nelson, G.P., and Hughes, H.L., "The Effects of Ionizing Radiation on Various COS/MOS Integrated Circuit Structures", IEEE Transactions in Nuclear Science, No. 6, pp. 264, Dec. 1972, RCA Technical Publication ST-6161.

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Applications of CD40107BE COS/MOS Dual NAND Buffer

by D. J. Blandford and G. L. Gimber

This Note describes the characteristics of the COS/MOS dual NAND buffer, the CD40107BE, and the wide variety of practical applications in which this important addition to the CD4000-series of COS/MOS devices can be used.

CHARACTERISTICS

Fig. 1 shows the logic diagram of the CD40107BE, which consists of two 2-input NAND buffers in an eight-pin plastic package; pin assignments are shown in Fig. 2. The bar on the output line of the logic diagram in Fig. 1 indicates that the output

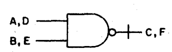


Fig. 1 – Logic diagram of the CD40107BE NAND buffer.

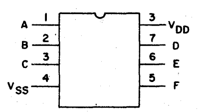
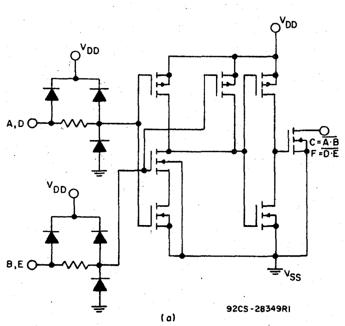


Fig. 2 – Pin assignments of the CD40107BE.

is open-drain, as shown in Fig. 3, the circuit diagram and truth table for a single buffer.



A	B	C*
0	0	1
1	0	1
0	1	1
1	1	0

(b)

* REQUIRES EXTERNAL PULL-UP RESISTOR TO V_{DD}

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Fig. 3 – (a) Circuit diagram of the CD40107BE, (b) truth table for 1 of 2 gates.

Each input includes the standard COS/MOS protection network, a 1.5 kilohm input resistor and diodes to V_{DD} and V_{SS}. The output device is a large n-channel transistor. Typical transistor sink-current characteristics are shown in Fig. 4 in which drain current, I_{DN}, is plotted against drain-to-source voltage, V_{DS}, for V_{GS} = 5 V, 10 V and 15 V (i.e., V_{DD} = 5 V, 10 V, and 15 V). Note, for example, that for a V_{DS} of 1 volt and a 10-volt supply, the NAND buffer is capable of sinking typically 120 milliamperes. Applications of this large current-sinking capability are described below.

A pull-up resistor from the output (pins 3 or 5) to V_{DD} enables the device to perform the logical NAND function, as shown in the truth table, Fig. 3(b). Useable values

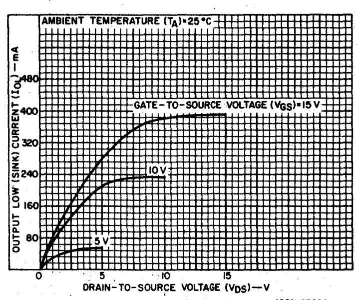


Fig. 4 – Minimum output low (sink) current characteristics of the CD40107BE.

of pull-up resistance lie between approximately 100 ohms and 1 megohm. Care should be taken when choosing a pull-up resistor or any other load not to exceed the maximum power dissipation of the device. Designers should refer to the device data sheet for allowable dissipation limits over the desired temperature range.

The three stages of gain from input to output of the CD40107BE, Fig. 3(a) result in a very sharp transfer characteristic, Fig. 5, near the ideal for a digital logic device. More complete characteristics are given in the CD40107B data sheet.[1]

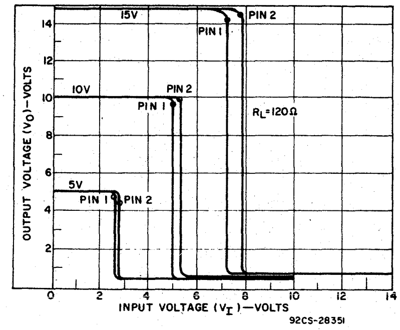


Fig. 5 – Transfer characteristics of the CD40107BE showing source-bias effect.

PRACTICAL APPLICATIONS

Practical applications of the CD40107B overlap with those of other devices in the COS/MOS CD4000 series, for example, with the logical NAND function of the CD4011 and with the buffer function of the CD4041, CD4049, and CD4050. However, the applications described in this Note are those for which, until now, no COS/MOS NAND buffer has had sufficient drive capability, in the hundred milliampere range.

In the first of these applications, Fig. 6, two NAND buffers are each driving a 2.2-watt, 12-volt incandescent lamp. The circuit is arranged as an astable oscillator with its period of approximately two seconds determined by the external capacitor and resistors. In this and other similar applications the load is used as a pull-up from the open-drain output to a power-supply voltage greater than zero and equal to or less than V_{DD}.

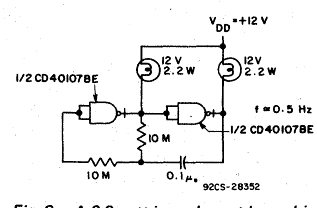
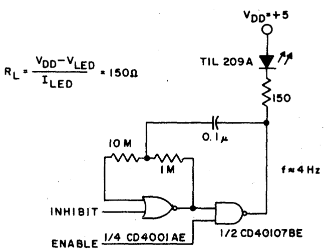


Fig. 6 – A 2.2-watt incandescent lamp-driver circuit.

The same type of astable circuit is shown in Fig. 7, but with a single load device, an LED with a current limiting resistor of 150 ohms. The NAND buffer, as well as driving the load, forms part of the astable circuit, with one of its inputs used as an enable; when this input is low, the LED is permanently off. The other half of the astable oscillator utilizes a two-input NOR gate, the CD4001AE, one input of which is used as an inhibit. With the timing components shown, the astable frequency is approximately 4 Hz.



INHIBIT	ENABLE	OUTPUT
0	0	OFF
1	0	OFF
0	1	OFF
1	1	ON

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Fig. 7 – LED driver circuit.

The NAND buffer is typically capable of sinking 120 milliamperes at a V_{DS} of 1 volt with a 10-volt supply. It therefore meets the typical requirements for the current-sinking device at the cathode terminal of a common-cathode LED multiplexed display circuit, Fig. 8. In this display circuit, data is presented in the form of four BCD numbers to be displayed on the four seven-segment LED's; the clock input determines the multiplexing rate. The two D-type flip flops of the CD4013AE or BE are arranged as a two-stage Johnson counter, the two Q outputs of which select the data transferred by the CD4052BE multiplexers to the CD4511BE decoder-driver. The same Q outputs are decoded by the four NAND buffers and used to turn on the seven-segment displays in the correct sequence. For example, when Q1 = 1 and Q2 = 0, both inputs of the NAND buffer marked B in Fig. 8 are high, and the buffer sinks current through the diodes of the second seven-segment display digit.

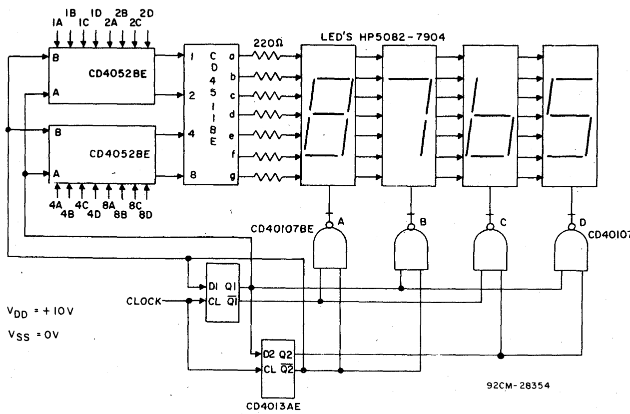


Fig. 8 – Multiplexed LED circuit.

By using the two NAND buffers of a single eight-pin DIP in parallel, it is possible to interface directly from a COS/MOS system to a heavy-duty load typified by the computer peripheral-printer hammer solenoid of Fig. 9. This type of solenoid typically requires 250 milliamperes to turn on which, at a supply voltage, V_{DD}, of 12 volts, implies a V_{DS} of approximately 0.6 volt. To prevent excessive current flow through the electrostatic-protection diodes to V_{DD} at the outputs of the NAND buffers, in applications such as the one under discussion, the switching of inductive loads, the protection diodes should be shunted with a low-dynamic-impedance switching diode, such as a 1N4154.

In many systems where COS/MOS devices are used for their wide operating-voltage range and high noise immunity, and particularly in industrial control applications, it is important to be able to drive relays directly. Fig. 10 shows a NAND buffer driving a common type of 12-volt relay, a two-pole change-over type with a coil resistance of 185 ohms. Again, a 1N4154 shunt diode is advisable.

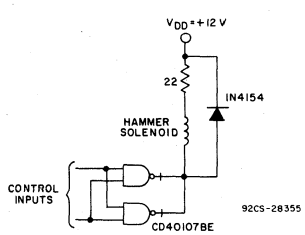


Fig. 9 – Solenoid driver circuit.

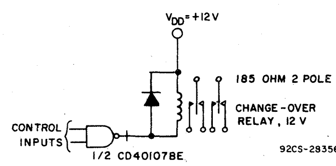
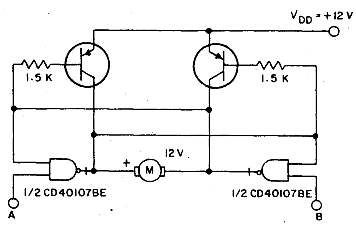


Fig. 10 – Relay driver circuit.

Fig. 11 shows a reversible 12-volt tape-recorder motor driven by two NAND buffers in a bridge circuit. Two p-n-p transistors provide an active pull-up to V_{DD}.

SCR's and triacs typically require tens of milliamperes of gate current, more than the current capability of a standard COS/MOS device output. The NAND buffer, however, is able to sink sufficient current, and in



A	B	MOTOR FUNCTION
0	0	OFF
1	0	COUNTER CLOCKWISE
1	1	AS PREVIOUS STATE
0	1	CLOCKWISE
1	1	AS PREVIOUS STATE

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Fig. 11 – Motor-controller circuit.

Fig. 12 is seen driving a 2N5756 triac. If isolation is required between the COS/MOS

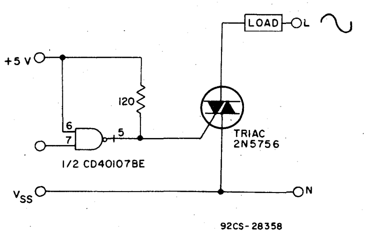


Fig. 12 – Direct dc drive interface of CD40107BE with a triac.

and triac systems, the circuit of Fig. 13 is used. In the figure, the NAND-buffer load is the primary coil of a pulse transformer

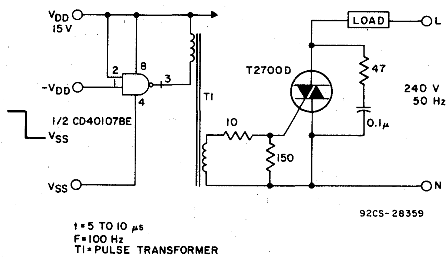


Fig. 13 – Interface of CD40107BE with triac, with COS/MOS component and triac isolated.

T_1, and when 5- to 10-microsecond pulses are applied at a 100-Hz repetition rate to the COS/MOS input, sufficient current flows in the transformer secondary to keep the triac, a T2700D, turned on. The NAND-buffer circuits make it possible for a COS/MOS system to control several amperes of current at line voltage.

Line driving is another application requiring large current pulses; Fig. 14 shows two NAND buffers driving a twisted-pair transmission line. Clock rates up to 8 MHz are readily achieved by circuits driving five meters of a 130-ohm line twisted at two turns per inch.

One of the most important applications for the open-drain NAND buffer is the COS/MOS to TTL interface shown in Fig. 15. The V_{DD} pin of the CD40107BE is connected to the power supply of the COS/MOS system, the external pull-up resistor to the 5-volt TTL supply. The values of the pull-up resistor required and the number of loads that may be driven are shown in the table accompanying Fig. 15.

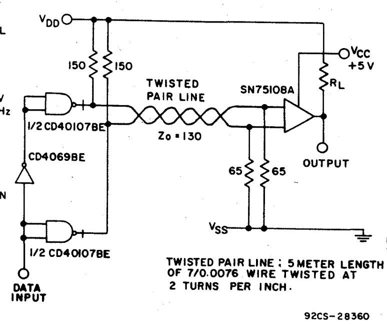
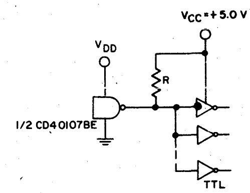


Fig. 14 – Line-driver circuit.



V_{DD}	V_{CC}	R	LOADS STD. TTL	LOADS LS TTL
5	5	2.7K	9	36
10	5	1.2K	20	80
15	5	1K	27	108

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Fig. 15 – COS/MOS to TTL interface.

References

1. Preliminary Data Sheet for the CD40107BE, COS/MOS Dual 2-Input NAND Buffer/ Driver, 1976; or RCA Databook, Series SSD-210, 1976.

COS/MOS Electrostatic-Discharge Protection Networks

by H. L. Pujol

RCA's two families of CMOS devices, the standard A series (3 to 15 volts) and the high-voltage B series (3 to 20 volts), are equipped with networks to protect the gate oxide of the devices against damage resulting from discharge of electrostatic energy between any two pins.

The gate input of a CMOS device is equivalent to a small, low-leakage capacitor (typically 5 picofarads) in parallel with a very high resistance (typically 10^{12} ohms). Because of this extremely high impedance which lends itself to the buildup of electrostatic charge, even a very low energy source (such as a static charge) is capable of developing voltages in the order of 80 volts, the typical breakdown voltage of an MOS gate oxide. In contrast with other semiconductor devices in which the breakdown can be tested any number of times without damage, the MOS gate oxide can be shorted, and the device destroyed, as the result of only one voltage excursion to the breakdown limit.

Protection Networks

Figs. 1 through 4 show the various protection networks incorporated in all COS/MOS product.

Standard Protection Networks

Fig. 1 shows the standard protection network incorporated in all A-series and some B-series devices. Input-diode D_2 is a

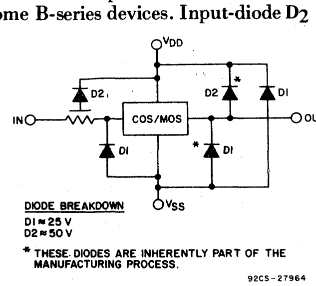

Fig.1 – Standard protection network.

distributed resistor-diode network that appears as two diodes to V_{DD}.

Improved Protection Network

Fig. 2 shows the improved protection network incorporated on all new B-series devices as well as on all A-series B-converted types.

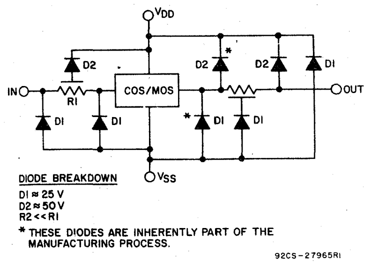

Fig.2 – Improved protection network.

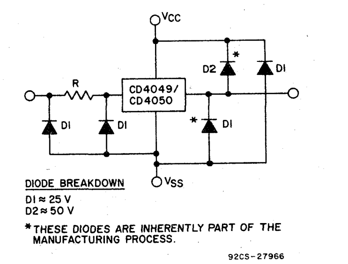

Fig.3 – Modified protection network.

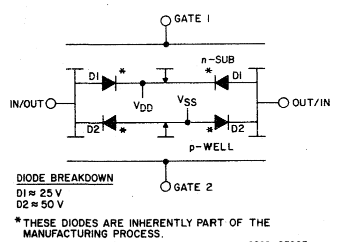

Fig.4 – Transmission gate with intrinsic diodes that protect against electrostatic discharge.

Other Protective Networks

Fig. 3 shows the modified protective network for a CD4049/4050 buffer. The input diode to V_{DD} is not incorporated so that the level-shifting function can occur.

Equivalent-Body Discharge Network

The protection networks described in this Note are evaluated and characterized by using the equivalent-body discharge network of Fig. 5. As C is increased, the amount of static energy dumped into the CMOS device increases. As R is decreased, the energy dissipated outside the device is reduced, thereby increasing the energy dissipated in the unit. A mercury relay is used to switch the RC source because such relays are fast and free from arcing or bouncing effects. Characterization of the various protection networks is done in 12 different combinations of inputs, outputs, and

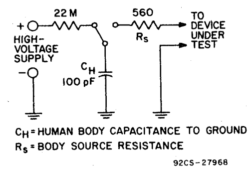

Fig.5 – Equivalent-body discharge network.

polarities. The combinations include all combinations of any two of the following pins: input, V_{DD}, V_{SS}, and output.

Evaluation of a protective network begins with the charging of a 100-picofarad capacitor through a 22-megohm resistor and a mercury relay to the desired voltage. The capacitor C_H of Fig. 5 is then discharged through the same mercury relay and a 560-ohm resistor into the pins under test. Results of repetitive tests are used to determine the worst-case capability of the protective networks, Table I.

TABLE I – Worst-Case Capability of Protective Networks

Protective Network	Worst-Case Capability
Standard (incl. CD4049, CD4050)	1 kV to 2 kV
Improved	4 kV
Transmission Gate	<800 V

Additional protection can be obtained by adding external series resistors at device inputs. The value of this resistance should be approximately 10 kilohms for gate inputs and 1 kilohm for transmission gate inputs. In addition, zener diodes at the output pins can clamp the voltage to a safe level. The zener-voltage should not exceed the absolute maximum rating of the part. On-chip protection networks are not used on transmission gates so that their low "on" resistance can be maintained. The 800-volt worst-case capability shown in Table I is provided by the intrinsic diodes shown in Fig. 4.

The value of the input resistor on all protection networks, except that used in transmission gates, can vary between 100 ohms and 2.5 kilohms because of circuit-design differences. This resistance, in conjunction with the capacitance of the gate and the associated protective diodes, integrates and clamps the device voltages to a safe level. The diagrams of Figs. 6, 7, and 8 demonstrate that the standard protection networks prevent higher than normal voltages from reaching the gate of the MOS device. In addition, the low RC time constant assures that circuit speed remains unchanged in spite of the additional components.

Because of the presence of the integral protection network, the V_{DD} power supply must not be turned off while a signal from a low-impedance pulse generator is being applied at an input of a COS/MOS circuit. Should the V_{DD} supply be turned off under such conditions, the V_{DD} line would be essentially grounded, and a positive voltage from the pulse generator would be impressed across the input diode to V_{DD}. This voltage could cause permanent damage to the diode or burn out the V_{DD} metallization. If it is expected that any input excursion will exceed $+ V_{DD}$ or fall below V_{SS}, the current through the input diodes should be limited to 10 milliamperes or less to assure safe operation.[1]

Reference

1. For additional operating considerations see "Guide to Better Handling and Operation of CMOS Integrated Circuits," J. Flood, H. L. Pujol, RCA Solid State Application Note ICAN-6525.

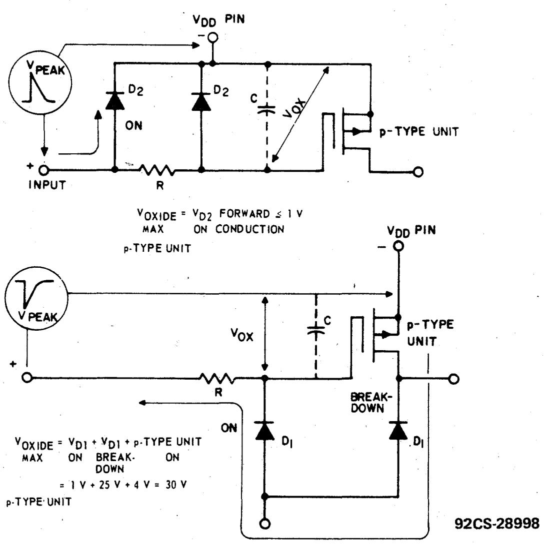

Fig.6 – Circuits used to provide protection between input pin and V_{DD} pin.

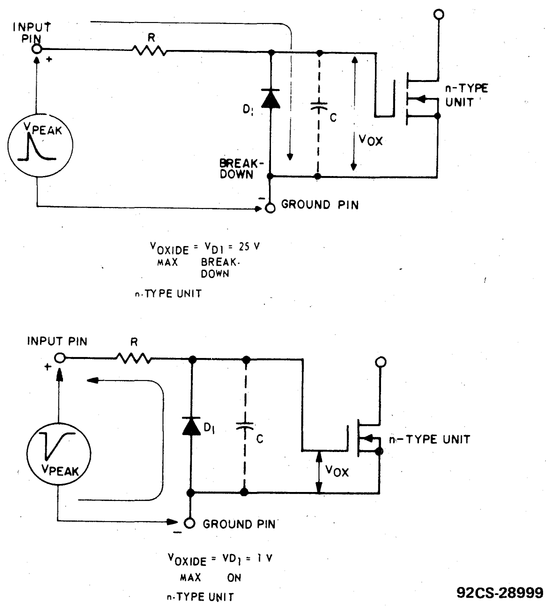

Fig.7 – Circuits used to provide protection between input pin and ground pin.

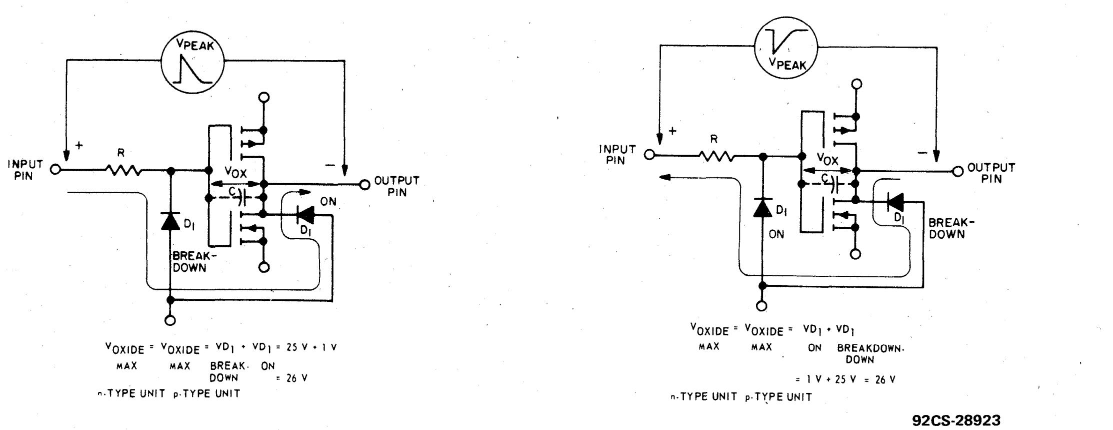

Fig.8 – Circuits used to provide protection between input pin and output pin.

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Power-Supply Considerations for COS/MOS Devices

by H.L. Pujol

RCA COS/MOS Digital Integrated Circuits operate at extremely low power dissipation levels. They function reliably with high noise immunity over a wide operating-voltage range. The RCA COS/MOS product line includes a standard line designed to operate with voltage supplies from 5 to 15 volts and a low voltage "A" series line designed to operate from 3 to 15 volts. These properties enable system designers to operate RCA COS/MOS devices from unregulated, poorly-filtered supplies, or from a wide variety of single- or multiple-cell battery sources.

This Note describes the salient features of COS/MOS devices which permit operation from such a wide range of power sources and provides the system designer with the necessary information to permit him to design the most economical power source for his COS/MOS system. This Note is applicable to both COS/MOS product lines mentioned above.

REVIEW OF PERTINENT COS/MOS DEVICE FUNDAMENTALS

Enhancement-Mode Device Characteristics

The MOS enhancement transistor is a majority-carrier device (See Fig. 1) in which the current in a conducting channel between two diffused electrodes (denoted as the source and the drain) is controlled (enhanced) by a voltage applied to a third terminal (the gate), which is insulated from the source and drain.

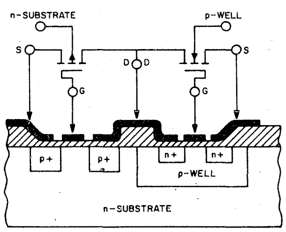


Fig. 1— Cross-section of COS/MOS transistor.

In an n-type device, the majority carriers are electrons. A positive voltage on the gate is required to enhance the conducting channel. For all gate voltages less than a threshold value (V_{th}), the conductivity of the channel is negligible and the device is said to be cut-off. For gate voltages greater than V_{th}, the channel is "enhanced", and current flow in the channel will occur if a suitable voltage is applied between the source and drain. The resultant device characteristics are shown in Fig. 2a.

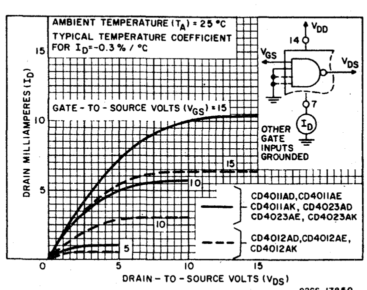


Fig. 2a— Typical n-channel characteristics.

The operation of the p-type device is analogous to that of the n-type, except that the carriers are holes, and the applied voltage required to enhance the channel must be negative rather than positive. (See Fig. 2b).

The gate electrode for a device of either polarity is insulated from the body of the device; therefore, current flows only from source to drain in the channel, never from the gate into the channel.

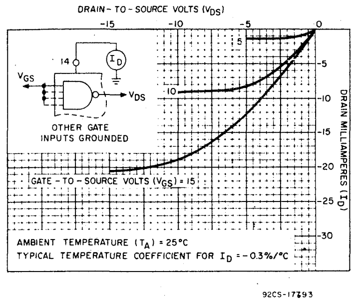


Fig. 2b— Typical p-channel characteristics.

CHARACTERISTICS OF A BASIC COS/MOS LOGIC INVERTER

Quiescent Device Dissipation.

The basic logic inverter (or gate) formed by use of only a p- and an n-type device in series is shown schematically in Fig. 3. When the input lead is grounded or otherwise connected to 0 volts (logical "0"), the n-device is cut-off, and the p-device is biased on. As a result, there is a low-impedance path from the output to V_{DD}, and an open circuit to ground. The resultant output voltage is essentially V_{DD}, or a logic "1".

Similarly, when the input voltage is a logic "1", or V_{DD}, then the n-channel device becomes a low impedance, while the p-channel device becomes an open circuit. The resultant output becomes essentially zero volts (logic "0").

Note that one of the devices is always cut-off at either logic extreme, and that no current flows into the insulating gates. As a result, the inverter quiescent power dissipation is negligible (equal to the product of V_{DD} times the leakage current).

A cross section of the COS/MOS inverter as it is formed in an integrated circuit on an n-type substrate is illustrated in Fig. 1. The source-drain diffusions and the p-well diffusion form parasitic diodes (in addition to the desired transistors) at the basic inverter nodes, as shown in Fig. 4. These parasitic elements are back-biased (across the power supply) and contribute, in part, to the device leakage current and thus to the quiescent power dissipation.

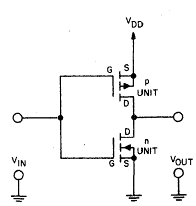


Fig. 3— Basic COS/MOS inverter (schematic).

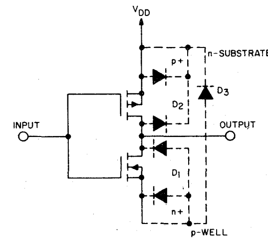


Fig. 4— Basic inverter showing parasitic diodes.

RCA's product line of COS/MOS devices consists of circuits of varying complexity (i.e., from the dual 4-input logic gate that contain 16 MOS devices, to the more complex 64-bit static shift registers that contain over 1000 devices). These devices occupy different amounts of silicon area and are composed of varying numbers of circuits formed from inverters. Consequently, each device in the family exhibits a particular magnitude of leakage current, depending upon the total effect of device count and parasitic diode area. For example, some logic gates are specified to operate with a typical power dissipation of 5 nW (V_{DD} = 10V), but 7-stage counters or registers are specified to operate with a typical power dissipation of 5 μW (V_{DD} = 10V). Published data includes both typical device quiescent-current levels and maximum levels (V_{DD} = 5V and V_{DD} = 10V). The maximum values are rarely encountered in RCA devices.

Device — Switching Characteristics.

The input/output characteristics for the COS/MOS inverter are shown in Fig. 5. As mentioned earlier the signal extremes at the input and output are approximately zero volts (logic "0") and V_{DD} (logic "1"). The switching point is shown to be typically 45 to 55% of the magnitude of the power-supply voltage (regardless of the magnitude of the power-supply voltage) over the entire range from 3 to 15 volts (or 5 to 15 volts). Note the negligible change in operating point from -55°C to + 125°C.

These excellent switching characteristics permit COS/MOS devices to be operated reliably over a wide range of voltages, a property not found in other logic forms.

AC Dissipation Characteristics.

During the transition from a logic "0" to a logic "1", both devices are momentarily on. This condition results in a pulse of instantaneous current being drawn from the power supply. The magnitude and duration of this current depends upon the following factors:

(a) the impedance of the particular devices being used in the inverter circuit

(b) the magnitude of the power-supply voltage

(c) the magnitude of the individual device threshold voltages

(d) the input driver rise and fall times

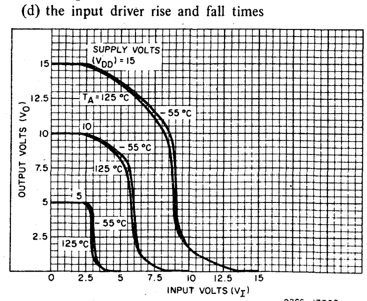


Fig. 5— Typical COS/MOS transfer characteristics as a function of temperature.

An additional component of current must also be drawn from the power supply to charge and discharge the internal parasitic node capacitances and the load capacitances seen at the output.

The device power dissipation which results from the above current components is a frequency-dependent parameter. The more often the circuit switches, the greater is the resultant power dissipation. The heavier the capacitive loading, the greater is the resultant power dissipation. The power dissipation is not duty-cycle dependent. For all intents and purposes it may be considered frequency (repetition-rate) dependent.

Because the RCA COS/MOS product line ranges widely in circuit complexity from device to device, the ac device dissipations vary widely from device to device. The effect of capacitive loading on the individual devices also varies. Figs. 6a and 6b show a family of curves for a typical gate device and a typical MSI device. These curves, from the published data for the individual devices, illustrate how device power dissipation varies as a function of frequency, supply voltage and capacitive loading.

AC Performance Characteristics.

During switching, the node capacitances, within a given circuit, and the load capacitances external to the circuit, are charged and discharged through the p- or n-type device conducting channel. As the magnitude of V_{DD} increases, the impedance of the conducting channel decreases accordingly. This lower impedance results in a shorter RC time constant (this non-linear property of MOS devices can be observed from a close scrutiny of the characteristic curves in Fig. 2). The result is that the maximum switching frequency of a COS/MOS device increases with increasing supply voltage. (See Fig. 7a).

Fig. 7b shows curves of propagation delay as a function of supply voltage for a typical gate device. However, the the trade-off for low supply voltage (i.e., lower output current to drive a load) is lower speed of operation.

The power dissipated during switching (if the load is assumed to be capacitive) is equal to:

$C_o V_{DD}^2 f$ [power is equal to energy per unit time]
where C_o is the output and load capacitance, V_{DD} is the supply voltage, and f is the operating frequency in hertz. A measure of this power dissipation as function of frequency can be obtained from the model shown in Figs. 8a and 8b which assumes step inputs and zero mode capacitance.

The average power for the square-wave input voltage shown (repetition rate $f_o = 1/t_o$) is calculated as follows:

$$P = \frac{1}{t_o}\int_0^{\frac{t_o}{2}} I_N(t) V_o \, dt + \frac{1}{t_o}\int_{\frac{t_o}{2}}^{t_o} I_P(t)(V_{DD} - V_o)\, dt$$

For P with $I_N(t) = I_P(t) = C_o \frac{dV_o}{dt}$ (step inputs only),

$$P = \frac{C_o}{t_o}\int_0^{V_{DD}} V_o dV_o + \frac{C_o}{t_o}\int_{V_{DD}}^{0} (V_{DD} - V_o)\, d(V_{DD} - V_o)$$

$$\therefore P = \frac{C_o V_{DD}^2}{t_o} = C_o V_{DD}^2 f$$

Thus, for a step input, the average power dissipated is directly related to the energy required to change and discharge the circuit capacitance to the supply voltage, V_{DD}. It should be noted that this power is independent of the device parameters. Although this equation was derived using an input voltage with a rise time of zero, it has also been shown to be a good approximation for circuits where the input voltage rise and fall times are small with respect to the repetition rate.

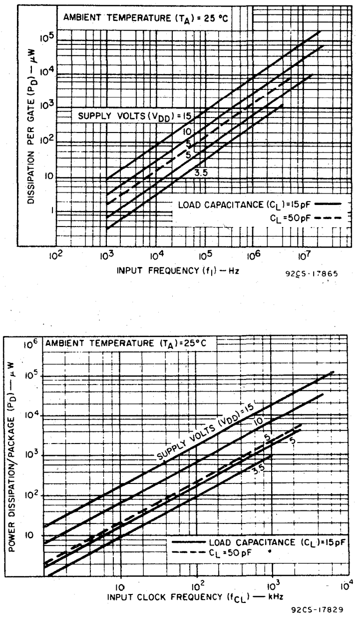


Fig. 6— Typical power dissipation characteristics (a) Basic gate power dissipation characteristics (b) MSI device power dissipation characteristics.

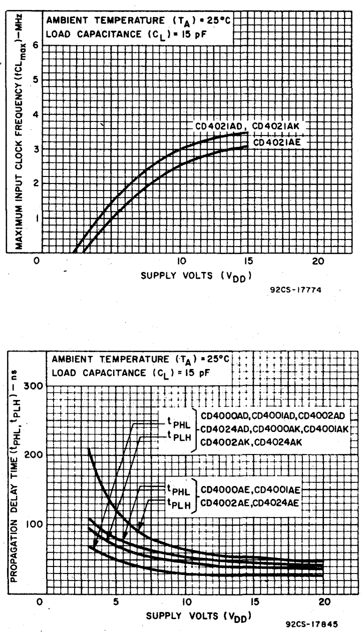


Fig. 7— Operating frequency and propagation delay as a function of power-supply voltage (a) Maximum guaranteed operating frequency as a function of power-supply voltage (b) Propagation delay as a function of power-supply voltage for the basic gate.

Calculating System Power

The foregoing material presented fundamental reasons why COS/MOS devices exhibit extremely low quiescent power. Also presented were reasons why ac power dissipation increases with operating frequency and why it varies from device to device.

For these reasons certain guidelines have been developed to assist the designer in estimating system power. Total system power is equal to the sum of quiescent power and dynamic power. Therefore, the two-step approach outlined below can be used:

1. Add up all typical package quiescent power dissipations (as shown in the RCA COS/MOS published data). Because quiescent power dissipation is equal to the product of quiescent device current times supply voltage, this parameter may also be obtained by adding all typical quiescent device currents, and multiplying the sum by the supply voltage, V_{DD}. Quiescent device current is shown in the published data for supply voltages of 5 volts and 10 volts only.

   In cases where the supply voltage is other than that shown in the published data, the quiescent device current can be interpolated because this current varies approximately linearly with voltage.

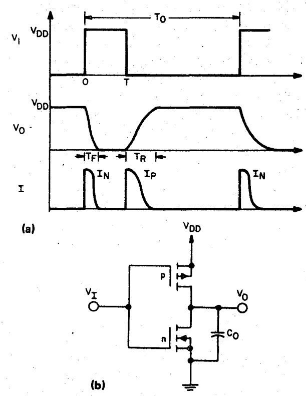


Fig. 8— Model for the evaluation of power dissipation (a) Waveforms (b) Circuit.

2. Add up all dynamic power dissipations using typical curves of dissipation per package as a function of frequency shown in the published data. In a fast-switching system, most of the power dissipation is dynamic, therefore, quiescent power dissipation may be neglected.

   The example below illustrates how these rules are used to calculate total system power dissipation. The system illustrated consists of ten 2-input NOR gates, eleven inverters, one D-type flip-flop, and one 7-stage binary counter. The system operates with a supply voltage of 10V at a frequency of 100 kHz, and has a load capacitance of 15 pF. (See Table 1)

Table I

Types	$P_{Quiescent}$ µW	$P_{Dynamic}$ mW
Gates	0.03	2
Inverters	0.01	2
D-type F/F	0.05	0.2
Counter	5	0.6
$P_T = P_Q + P_D = 4.8$mW (neglecting P_Q)		

This example assumes that all devices are switching at the clock-rate (100 kHz). Not all of the logic circuits will be switching states at this rate, thus, the total power dissipation will be significantly lower than that stated in the example.

Power-Supply Regulation Requirements.

The preceding discussion demonstrated that COS/MOS devices exhibit reliable switching properties over a wide range of power-supply voltages. This fact implies that an unregulated supply may be used with the provision that

(1) maximum voltage limits are not exceeded or

(2) system speed is no greater than the speed which can be supported by the COS/MOS devices operating at the lowest value of the V_{DD} expected from the unregulated supply.

To establish the extent of the regulation required, the system designer must first determine the maximum operating frequency required. Usually, the maximum frequency of the system is limited by the slowest responding devices in a logic chain. By reference to the curve of frequency as a function of V_{DD} and C_L given in the published data for that device, a minimum V_{DD} voltage (required for proper operation) can be determined. Any value above this V_{DD} (minimum) will provide acceptable performance in the system. By selection of a nominal V_{DD} half way between V_{DD} (minimum) and the 15-volt maximum rating for COS/MOS devices, the designer can estimate the percentage regulation required for his system to perform adequately.

For example, the published data of the RCA CD4004A 7-stage binary counter shows a curve (shown in Fig. 9) of frequency as a function of operating voltage for that device. For operation of this counter at 5 MHz, with a loading capacitance of 15pF, the minimum operating V_{DD} permitted for reliable operation is 10 volts, as shown on the curve.

Because the maximum V_{DD} is 15 volts, a half-way voltage of 12.5 volts should be the nominal value used. In this case, the maximum percentage regulation is 20%. If the designer desires a nominal V_{DD} closer to V_{DD} minimum, then better regulation is required, (for example in battery-operated equipment where a standard cell is available).

Filtering Requirements

Power-supply filtering requirements for COS/MOS systems are minimal. Two factors account for this situation: (1) the low quiescent power dissipations involved, and (2) the fact that the peak value of the ripple does not go below a minimum V_{DD} (which supports the required switching frequency), so that the COS/MOS logic performs satisfactorily.

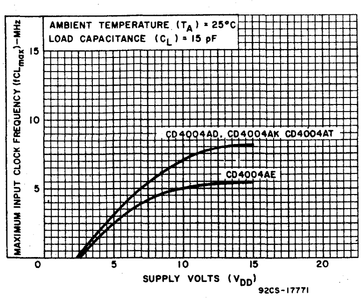


Fig. 9— Maximum frequency as a function of power-supply voltage for the CD4004 and CD4004A types.

This performance has been demonstrated in the laboratory (see Fig. 10). The amount of ripple on the power supply is quite high, yet the device functions properly.

Typical Supplies

The following circuits indicate some examples of adequate supplies for COS/MOS systems.

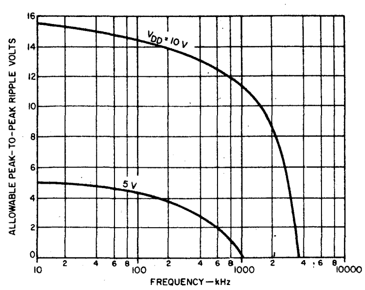


Fig. 10—Peak-to-peak ripple voltage as a function of frequency.

Battery Standby System

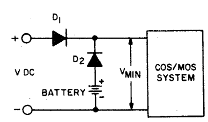


Fig. 11—Battery standby for COS/MOS systems.

This system is advantageous in cases where the dc supply becomes open or short-circuited.

With a low battery voltage the COS/MOS system will continue to function without interruption. In order to drive this system the battery voltage and dc supply voltage should relate as follows:

$V_{battery} = V_{min.} + 0.7V$, (0.7V ≈ one diode drop)

$V_{max.} > V_{DC}$ supply $> V_{min.} + 1.4V$

In the event the supply drops below $V_{min.}$, the battery will forward bias diode D2 to form a closed-circuit and the COS/MOS system will continue to function properly through the battery.

High DC Source

For applications (especially in aircraft equipment) where the supply voltage exceeds the RCA COS/MOS maximum rating of V_{DD}, the circuit of Fig. 12 can be used to reduce the high supply voltage to the normal COS/MOS voltage range. This configuration uses a Zener diode, a resistor R and a capacitor C.

The low current demand of the COS/MOS system permits an inexpensive but effective Zener diode regulator.

Some of the design considerations are as follows:

1. Selection of Zener Diode and Resistor R

   The amount of current that must be maintained through the diode (I_d) is a function of the difference between the worst-case average current required by the COS/MOS systems and the current required by the Zener diode for regulation based on its particular breakdown characteristics.

   The diode current (I_d) and the worst-case average system current (I_{avg}) determine the value of the resistor (R) for a particular Zener regulating voltage.

2. Selection of Capacitance C

   Before the proper capacitance can be selected the following system requirements must be decided upon:

   a. Peak charge requirement. This requirement is a function of the peak current and its pulse width. It must be measured for the particular system speed and load capacitance.

   b. Permissible V_{DD} minimum: As mentioned in previous sections, this minimum voltage will determine the maximum operating speed of the COS/MOS system.

The size of the capacitor (C) may then be determined from the following formula:

$Q = I_p t$ (charge = peak current x pulse width)

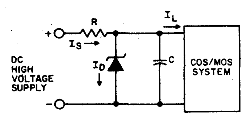


Fig. 12—Circuit for interface of COS/MOS systems to high-voltage supply.

SUMMARY

This Note shows that RCA COS/MOS devices offer many advantages in the area of simplified power-supply requirements. The wide operating voltage range (3 to 15 volts or 5 to 15 volts) from a single supply, low power dissipation, and high noise immunity permit system designers to use less expensive, unregulated, power supplies. This wide voltage range makes COS/MOS logic circuits ideal for battery-operated equipment because a better selection of cells is feasible. Another advantage is the direct compatibility of COS/MOS devices with bipolar devices which eliminates expensive and power-consuming interface circuits. (See Ref. 1.)

COS/MOS transistors show great potential for use in large arrays because of the low power dissipation and effective use of chip area. The relatively small area consumed by COS/MOS circuits, as well as the elimination of area and power-consuming resistors, results in high circuit-density per unit-silicon-area.

The performance features mentioned in this Note, as well as the reduced costs inherent in IC technology make COS/MOS circuits extremely attractive in many digital systems.

1. "Interfacing COS/MOS WITH OTHER LOGIC Families", ICAN6602 by A. Havasy and M. Kutzin.

Noise Immunity of COS/MOS B-Series Integrated Circuits

by T. Chesney
R. Funk

The excellent noise-immunity characteristics of COS/MOS (complementary-symmetry/metal-oxide-semiconductor) digital IC's is a paramount reason for their preferred and successful use in high-noise automotive, process-control, production-monitoring, and similar harsh-noise-prone applications. The introduction of the RCA B-series COS/MOS devices furthers the well-known noise immunity advantages of the COS/MOS technology in two important ways:

1. Improved noise-energy immunity as a result of balanced low-impedance output circuitry in all RCA B-series COS/MOS devices.
2. Standardized (EIA-JEDEC standards) dc noise-immunity and noise-margin ratings covering buffered and unbuffered CMOS-logic types.

Included in this Note are brief discussions of logic-system noise and rejection concepts, COS/MOS dc/ac noise-immunity specifications and definitions, and dc/ac noise-immunity performance data for several B-series COS/MOS gates, inverters, and high-current drivers.

Logic-System Noise Concepts

Successful application of any digital-logic IC family requires consideration of the following:

1. Externally or internally generated noise — both radiated and conducted.
2. The inherent noise-immunity capability of the logic family selected.
3. System noise-rejection measures.

Without coordination of these three points, a system design may perform unfavorably.

Consider first the various system or environmental noise generating sources. External system noise may include the noise imposed upon a logic system by electric motors, welders, rf transmitters, x-ray machines, high-current solenoids or relays, pulsed lasers, and circuit breakers. All of the preceding emit EMI (electromagnetic interference), and many produce power-line or ground-path noise disturbance. External noise is characterized by randomly occurring high-energy transients that are not easily anticipated. Usually, this noise is coupled electromagnetically or capacitively to signal, supply, and ground lines. Internal logic-system noise is usually generated on logic-signal lines by capacitively coupled crosstalk or by logic-switching current surges on supply lines or ground lines. In ultra-high-speed logic families such as ECL, reflection noise resulting from an impedance mismatch is also an internal noise problem; but because of relatively long output transition times of CMOS devices (more than 10 nanoseconds), reflection noise can be excluded from further consideration.

Since both external and internal noise must be considered, logic systems must be designed to survive in a medium to severe noise environment, a fact that leads to the second consideration, selection of an IC logic family having noise-rejection characteristics appropriate to the application. As is demonstrated below by considerable data, B-series COS/MOS devices have good dc and ac and noise-energy immunity characteristics. No matter how good the noise-rejection capability of a logic IC family, such as COS/MOS, system design measures to reduce noise entry into logic signal lines, power supply lines, and the ground are usually necessary to some extent. The methods most commonly used to minimize noise effects in COS/MOS logic systems are:

1. **Power-source line decoupling** - Good practice suggests use of a small-value series resistor and zener diode and a capacitor to ground on each logic card or each 50 to 100 IC's. High-voltage supply transients can usually be rejected by this simple measure. Separate lines should be used for logic circuits and power switching circuits.
2. **Ground-Line Noise** - In a system in which many high-current switching components, such as motors, relays, and SCR's are involved, logic grounds should be separated from high energy component grounds. The logic grounds should be returned to a common point.
3. **AC noise on system signal inputs** - 60 Hz is a commonly used frequency reference. Raw ac power lines should be isolated using a transformer or optical coupler. Zener-diode limiters are also effective. 60-Hz signals can be shaped by using COS/MOS Schmitt-trigger circuits.

NOISE SPECIFICATIONS

COS/MOS noise immunity is characterized by dc specifications, ac noise-immunity performance, and noise-energy immunity performance. Each of these characteristics is defined below and supported by performance data.

DC Specifications

Table I shows the industry standardized (JEDEC) noise immunity and noise margin ratings, V_{IL} and V_{IH}, for B-series devices. Note that separate specifications have been established for B (buffered) types and UB (unbuffered) types.[1]

Two important noise characteristics can be defined by using the V_{IL} and V_{IH} ratings:

1. **Noise Immunity** - The V_{IL} and

V_{IH} limits are the device input-signal noise-immunity ratings which, as defined in Table II, are 30, 30, and 27 percent, respectively, of the 5, 10, and 15-volt supply voltages for the B-series types. Percentages are lower for unbuffered gates, as shown in Table II. The V_{IL} and V_{IH} ratings define the maximum permissible additive noise voltages at an input terminal when input signals are 50 millivolts off the supply rails.

2. **Noise Margin** - The difference between V_{IL} and V_O or V_{IH} and V_O is the device noise-margin voltage for the noninverting case. Table II designates the B and UB noise-margin voltages. Noise margin voltage is defined as that noise voltage that can be impressed upon V_{IN} at any (or all) logic I/O terminals without upsetting the logic or causing any output to exceed the V_O ratings of Table I.

Of the two COS/MOS dc noise definitions, immunity and margin, RCA prefers the noise-immunity specification as the more practical COS/MOS system definition because CMOS outputs are normally 50 millivolts off the rails.

However, designers familiar with TTL may prefer to use the noise-margin voltage for system analysis.

AC Noise Immunity

COS/MOS ac noise immunity takes into account both the device switching threshold (dc noise immunity) and the noise-pulse width. The latter is affected primarily by the COS/MOS IC bandwidth, especially output transition times. Fig. 1 shows the usual COS/MOS noise-voltage amplitude, V_t, as a function of noise-pulse-width characteristic, t_p.

Because noise pulses are narrow compared with device output transition time, noise-voltage rejection is high. As the pulse widths approach the IC bandwidth, the curve flattens out at the device switching-threshold voltage. AC noise-voltage

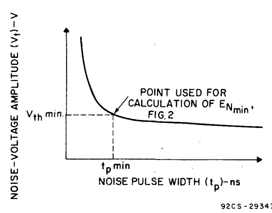


Fig. 1 Generic ac noise-immunity curve.

immunity curves, such as those in Fig. 1, are applicable to:

- Positive noise pulses on signal lines in the 0 state.
- Negative noise pulses on signal lines in the 1 state.
- Positive noise pulses on the ground terminal.
- Negative noise pulses on the positive supply terminal.

Curves of this type indicate the frequency (as defined by noise-pulse characteristics) at which the user has satisfactory dc noise performance. The curves are especially useful in calculating typical noise-energy performance, a parameter that takes into account the circuit impedance.

Table I — B-Series DC Noise Immunity and Noise Margin (T_A = 25°C)

Characteristics	Test Conditions		Input Voltage
	V_O (V)	V_{DD} (V)	(V)
Input Low Voltage V_{IL} max.			
B types	0.5/4.5	5	1.5
	1/9	10	3
	1.5/13.5	15	4
UB types	0.5/4.5	5	1
	1/9	10	2
	1.5/13.5	15	2.5
Input High Voltage V_{IH} min.			
B types	0.5/4.5	5	3.5
	1/9	10	7
	1.5/13.5	15	11
UB types	0.5/4.5	5	4
	1/9	10	8
	1.5/13.5	15	12.5

Table II — B-Series Noise Immunity and Noise Margin

	Noise Immunity (%)		Noise-Margin Voltage (V)	
V_{DD}	B-Series	UB-Series	B-Series	UB-Series
5	30	20	1	0.5
10	30	20	2	1
15	27	17	2.5	1

Noise-Energy Immunity

Noise-energy immunity takes into account the pulse width and the circuit impedance at the point where the noise is introduced. Noise-energy immunity, E , in nanojoules, is calculated as follows:

$$E_N = \frac{V_{th}^2}{R_O} t_p$$

where E_N is noise-energy immunity in nanojoules, V_{th} is the device switching-voltage threshold for a given noise-pulse width, t_p is the noise-voltage pulse width in nanoseconds, and R_O is the impedance to ground in ohms at the point of noise entry. R_O is usually the output resistance of the COS/MOS device.

By using values of V and t_p obtained from the curve of Fig. 1, the noise-energy immunity curve of Fig. 2 is generated for a given value of R_O. A comparison of Figs. 1 and 2 shows that the minimum values of

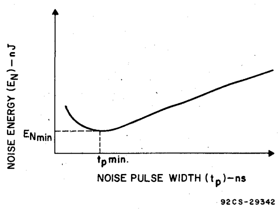


Fig. 2 Generic noise-energy-immunity curve.

noise-energy immunity occur at an input-noise pulse width for which the noise-voltage amplitude of Fig. 1 begins to approach the dc noise-immunity or threshold voltage of a device. The minimum noise-energy immunity is the basis for the calculations and comparisons involving most IC families.

NOISE-IMMUNITY TEST DATA

DC Noise-Immunity Test Data

CMOS dc noise-immunity performance is obtained by plotting the voltage-transfer characteristic of a CMOS gate, inverter, or buffer. Figs. 3 and 4 show the voltage-transfer characteristics of the CD4001B, a

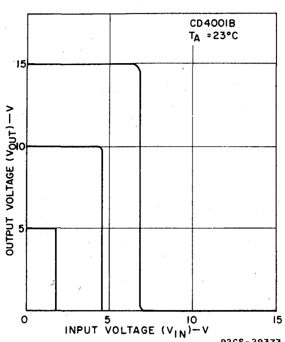


Fig. 3 CD4001B voltage transfer characteristic.

buffered, quad 2-input NOR gate, and the CD4001UB, an unbuffered version of the same gate. Comparison of Figs. 3 and 4 and Table I indicates that the values of V_{IL} and V_{IH} for these devices are well

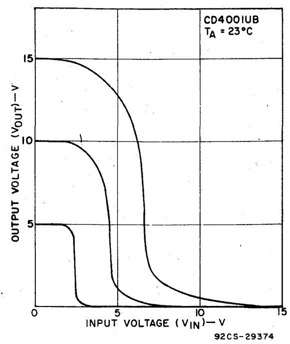


Fig. 4 CD4001UB voltage transfer characteristic.

within the standard JEDEC specifications. The V_{IL} and V_{IH} values for any typical COS/MOS device indicate a typical dc noise immunity close to 50 percent of the supply voltage, a paramount advantage of CMOS logic devices over TTL, ECL, PMOS, and NMOS logic devices.

AC Noise-Immunity Test Data

Fig. 5 shows the test circuit used in the evaluation of the ac noise immunity of B-series COS/MOS devices. The criterion used is the triggering of a typical CD4013B flip-flop at the clock input. The

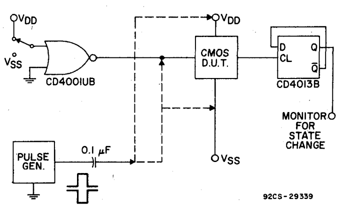


Fig. 5 Test circuit used in the evaluation of B-series COS/MOS devices.

circuit of Fig. 5 accounts for typical CMOS loading factors and generally reflects the ac noise performance of typical B-series devices. The device types used in the evaluation include the following:

CD4001UB unbuffered quad 2-input NOR gate,
CD4001B buffered quad 2-input 2-input NOR gate,
CD4011UB unbuffered quad 2-input NAND gate,
CD4069UB hex inverter,
CD4049UB hex inverting buffer.

The above list includes the most commonly used COS/MOS gates, inverters, and buffered devices. The ac noise-immunity characteristics of the buffered NOR gate (CD4001B) reflect the noise-immunity performance of buffered CMOS products of all descriptions.

SIGNAL-LINE OR EXTERNAL NOISE IMMUNITY

The following analysis was used to determine the immunity of a COS/MOS gate to noise on the input line at both the 0 (low-level) and 1 (high-level) logic states.

0-State Analysis

The signal-line noise immunity of COS/MOS gates and inverters was evaluated by means of the test circuit shown in Fig. 6. The COS/MOS units

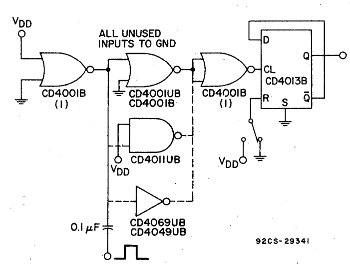
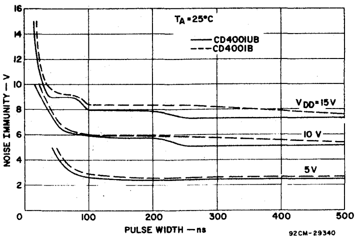


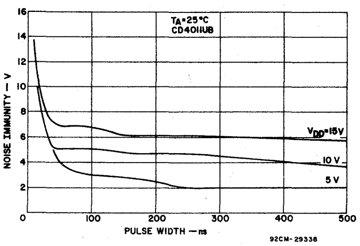
Fig. 6 Test circuit used to evaluate signal-line noise immunity of COS/MOS gates and inverters.

tested were the CD4001UB, CD4001B, CD4011UB, CD4049UB, and CD4069UB. Fig. 7 shows the results obtained. The test circuit is designed to measure the voltage required at the input of the unit under test to trigger a CD4013 flip-flop.

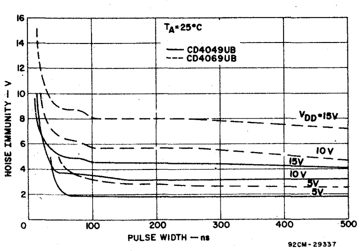
During test, a positive-going noise pulse is introduced into the signal line of the unit under test. At some voltage level, depending on the width of the pulse and the gate thresholds, this pulse causes the flip-flop to be clocked via the CD4001B gate. This voltage level defines the permissible input range for a logical 0.



(a) CD4001B, CD4001UB



(b) CD4011UB

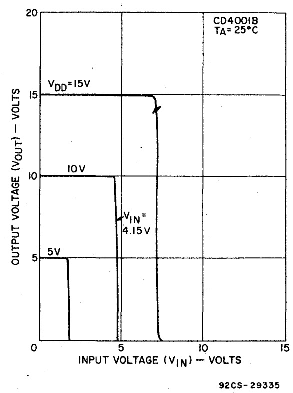


(c) CD4049UB, CD4069UB

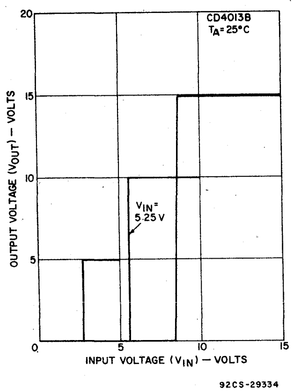
$T_A = 25°$

Fig. 7 Results of 0-state signal-line noise-immunity tests.

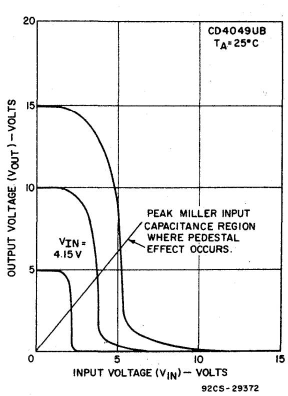
A dc analysis of the transfer characteristics of the components included in the test setup can also be used to determine the noise level required to clock the flip flop. Fig. 8(a) shows that a signal of 4.15 volts is required at the input to the CD4001B gate to produce an output of 4.5 volts at a supply voltage, V_{DD}, of 10 volts. Fig. 8(b) shows that an input of 5.25 volts is required to trigger the CD4013 flip-flop at a supply voltage, V_{DD}, of 10 volts. All measured values shown in Fig. 8 were obtained from measurements on gates that have typical threshold-switching characteristics.



(a) CD4001B



(b) CD4013B



(c) CD4049UB $T_A = 25°C.$

Fig. 8 Transfer characteristics of components used in the circuit of Fig. 6.

Careful analysis of the ac noise curves of Fig. 7(c) (for the CD4049UB) for 0-state signal-line noise shows a voltage-pedestal effect occurring at noise pulse widths associated with the noise-threshold region of the units under test. A comparison of the voltage-transfer curves of Fig. 8(c) with the dynamic input capacitance curves for the CD4049UB, Fig. 9, reveals that this pedestal effect occurs in the same region as the peak Miller input capacitance, where the inverter is in its maximum linear-gain region. Most 0- and 1-state noise-voltage characteristics curves in this Note exhibit this pedestal effect to some degree.

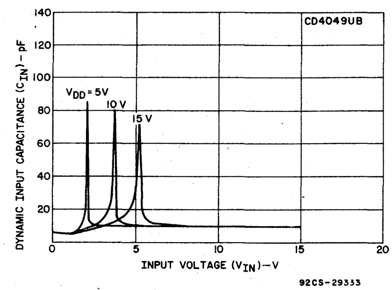


Fig. 9 Dynamic input capacitance curves for the CD4049UB. $T_A = 25°C.$

1-STATE ANALYSIS

Fig. 10 shows the test arrangement used and Fig. 11 the results obtained from noise-immunity measurements on the COS/MOS logic gates and inverters identified above when the input is high and a negative-going pulse is superimposed on the signal line.

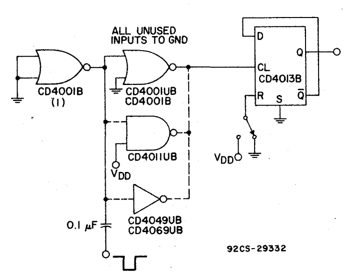
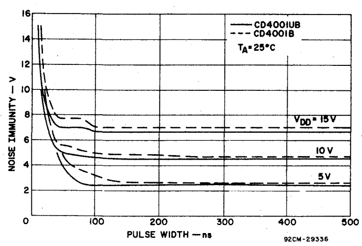
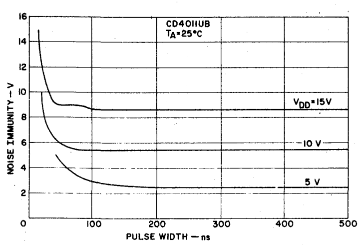


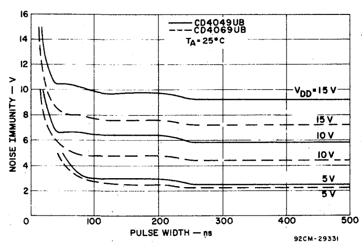
Fig. 10 Test circuit used to measure noise immunity of COS/MOS logic gates and inverters when the input is high and a negative-going pulse is superimposed on the signal line.



(a) CD4001B, CD4001UB



(b) CD4011UB



(c) CD4049UB, CD4069UB

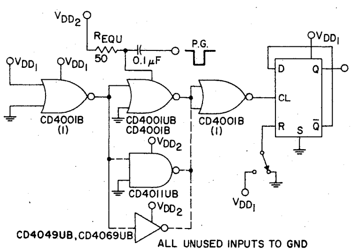
$T_A = 25°C.$

Fig. 11 Results of 1-state signal-line noise-immunity test.

POWER-SUPPLY NOISE IMMUNITY

The test configuration shown in Fig. 12 measures the ability of test units to withstand a negative-going noise pulse superimposed on the supply line without a change in state; Fig. 13 shows results of tests. A pulse of sufficient amplitude causes the output of the gate to decrease so that, at some point, the CD4013B flip-flop is triggered from the rising voltage at the output of the driving inverter stage.

It should be noted that two power supplies are used in the arrangement of Fig. 12. An equivalent resistor or inductor

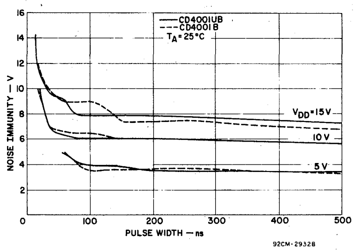


EQUIVALENT RESISTANCE, R_{EQU} (ohms)	MINIMUM PULSE WIDTH* (nanoseconds)
100	53.4
50	55.5
33	47.5
25	51.1

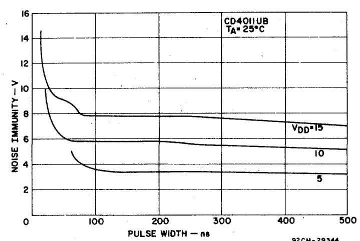
* VARIATION THE RESULT OF WAVE SHAPING

92CS-29329

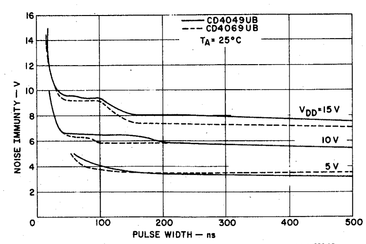
Fig. 12 Test circuit used to measure the ability of test units to withstand a negative-going noise pulse on the supply line without a change in state.



(a) CD4001B, CD4001UB



(b) CD4011UB



(c) CD4049UB, CD4069UB

$T_A = 25°C.$

Fig. 13 Power-line noise immunity.

for simulating contact resistance and lead length is used in the V_{DD} line of the unit under test. Without this resistance the test unit will not react to the noise pulse.

GROUND-NOISE IMMUNITY

Noise on the power line may be effectively reduced or eliminated by the use of decoupling capacitors; however, ground-line noise cannot be reduced so easily and, therefore, is more objectionable. Fig. 14 shows the test circuit used to measure the ground-line noise immunity of COS/MOS gates and inverters; Fig. 15 shows curves of the results obtained. Again, the units under test would not react to the noise unless a 25-ohm resistor or small inductor simulating lead length or contact resistance were placed to ground.

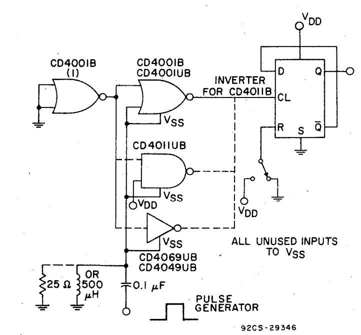
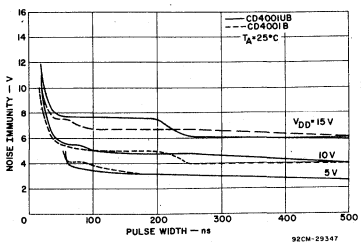


Fig. 14 Circuit used to measure ground-line noise immunity.

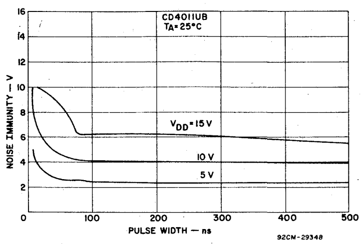
CROSSTALK NOISE IMMUNITY

A test circuit used to evaluate crosstalk is shown in Fig. 16. A noise pulse from a pulse generator is coupled to the signal line of the gate or inverter through a capacitor. The noise voltage necessary to trigger the flip-flop is then measured for different values of capacitance under high and low input conditions. Fig. 17 shows the effect of capacitance on the inputs of the units under test.

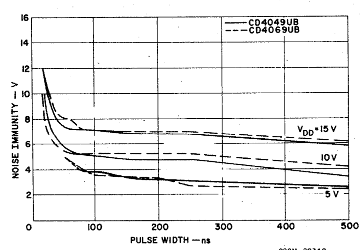
The circuit shown in Fig. 18 more closely approximates crosstalk caused by adjacent signal lines. The response of the test circuit to a noise pulse may be explained by analysis of the response of a high-pass RC circuit to a ramp input of $V_i = \alpha t$, where α is the coefficient of



(a) CD4001B, CD4001UB



(b) CD4011UB



(c) CD4049UB, CD4069UB

Fig. 15 Ground-line noise-immunity measurements.

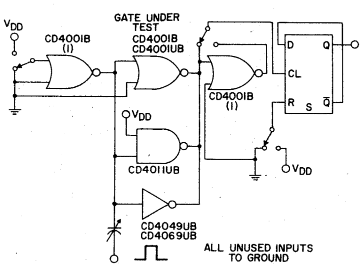
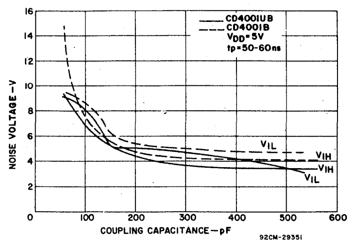
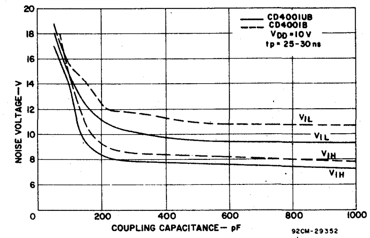
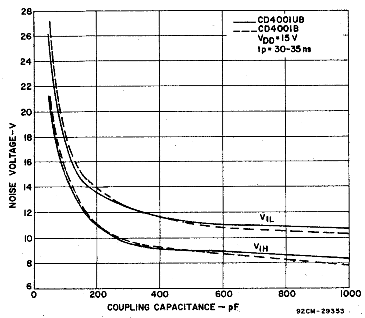
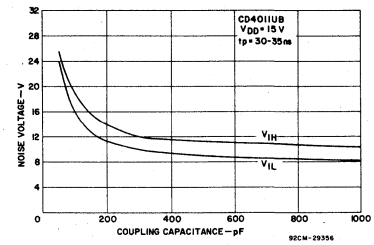


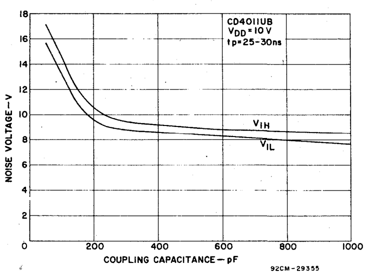
Fig. 16 Circuit for measuring noise voltage as a function of coupling capacitance.

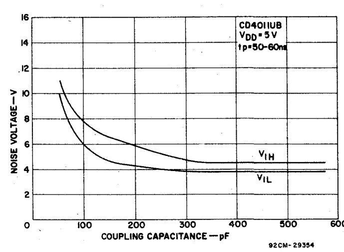


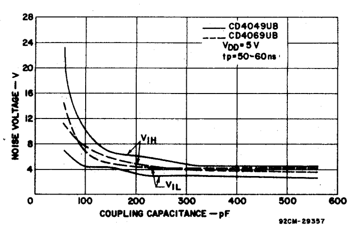


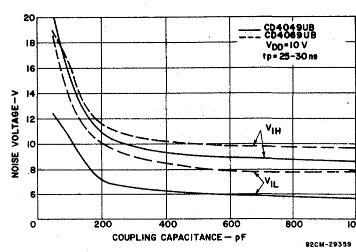












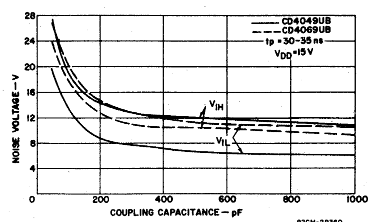


Fig. 17 Effect of coupling capacitance on the inputs of the units under test (T_A = 25°C).

coupling and t is rise time, 10 to 90 percent. The output voltage V_O may be expressed by the following equation:

$$V_O = \alpha RC\,(1 - e^{-t/RC}) \qquad (1)$$

The equivalent circuit for the part of the test configuration used in this analysis is shown in Fig. 19. On the basis of this equivalent circuit, Eq. (1) may be rewritten as follows:

$$V_{O\,max} \cong \alpha\,(Z_O \parallel Z_{IN}\,C\,[(1 - e^{t/2 Z_O \parallel Z_{in}})\,C] \qquad (2)$$

If V_i is assumed to be $\propto t$ during the period in which the output voltage switches from 10 to 90 percent of its total value, this change in output voltage can be expressed as follows:

$$\Delta V_{O\,max} \approx \frac{V_i\,(Z_o \parallel Z_{in})\,C}{t} \cdot [i - e^{-t/2\,Z_o \parallel Z_{in})\,C}] \qquad (3)$$

The results of this analysis may be applied to the various crosstalk waveforms obtained.

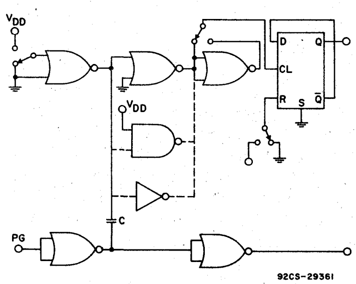


Fig. 18 Circuit closely approximating conditions for crosstalk on adjacent signal lines.

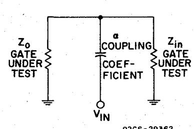


Fig. 19 Equivalent circuit used in crosstalk analysis of test configuration shown in Fig. 18.

Crosstalk measurements that simulate actual operation are made by use of the test circuits shown in Figs. 20 and 21. The circuit of Fig. 20 simulates a round-cable system and Fig. 21 a ribbon-cable system.

In Fig. 20, a sense line is placed tightly within five surrounding wires (No. 22 gauge) to form a 6-foot-long cable with a capacitance of 18 picofarads per foot (determined by measurement).

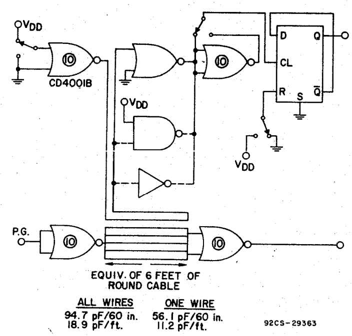


Fig. 20 Circuit simulating a round-cable system.

In Fig. 21, a sense line is placed between two adjacent driving lines (No. 22 gauge) of a 6-foot-long ribbon cable with a capacitance of 16 picofarads per foot (determined by measurement).

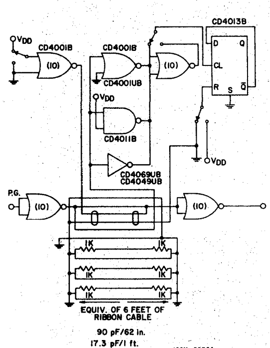


Fig. 21 Circuit simulating a ribbon-cable system.

The results of crosstalk are shown in the photographs of Figs. 22 and 23 for round cable and ribbon cable, respectively. The crosstalk was insufficient to trigger the CD4013B under all conditions of the circuits of Figs. 20 and 21.

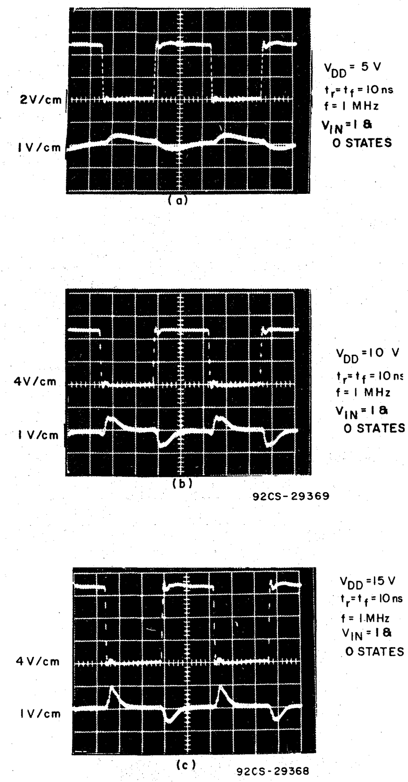


Fig. 22 Crosstalk in the round-cable system.

NOISE-ENERGY-IMMUNITY PERFORMANCE DATA

Table III shows computed values of noise-energy immunity for the gate, inverter, and buffer types identified above. Noise pulse width, t_p, and noise threshold voltage, V_T, data were obtained directly from the 1 and 0 signal-input ac noise-immunity test curves presented earlier in this Note, Figs. 7 and 11. Values of R_O are typical output impedances for the CD4001B driving gate used in obtaining the curves. Fig. 24 is a plot of high- and low-input state noise-energy immunity for the CD4001B gate as a function of input pulse width. These curves show that noise-energy immunity is high for noise bandwidths that exceed the speed capability of the device, and a minimum of approximately 1.3 nanojoules where the noise-pulse width (50 to 100 nanoseconds) approximates the device output transition time. Noise-threshold energy increases steadily with greater pulse widths.

Table III — Typical Values of Noise-Energy Immunity.

TYPE	SUPPLY VOLTAGE V_{DD} (V)	NOISE PULSE WIDTH t_p (ns)		NOISE THRESHOLD VOLTAGE V_t (V)		TYPICAL SIGNAL LINE IMPEDANCE R_O (ohms)		TYPICAL NOISE-ENERGY IMMUNITY* LOGIC STATE	
		LOW	HIGH	LOW	HIGH	R_{OL}	R_{OH}	LOW E_{NL}(nJ)	HIGH E_{NH}(nJ)
CD4001UB	5	100	100	2.75	2.65	700	700	1.08	1.00
	10	60	40	6.3	5.1	270	270	8.82	3.85
	15	40	40	9.0	7.0	190	190	17.05	10.32
CD4001B	5	160	150	2.58	2.85	700	700	1.52	1.74
	10	80	40	6.2	5.6	270	270	11.40	4.65
	15	40	40	9.6	7.8	190	190	19.40	12.81
CD4011UB	5	100	140	3.0	2.67	700	700	1.29	1.43
	10	40	80	5.0	5.45	270	270	3.70	8.80
	15	60	40	6.9	9.1	190	190	15.03	17.43
CD4049UB	5	60	120	2.0	2.9	700	700	0.343	1.44
	10	40	40	3.7	6.7	270	270	2.03	6.65
	15	60	40	4.9	10.4	190	190	7.58	22.77
CD4049UB	5	150	150	2.75	2.60	700	700	1.62	1.45
	10	60	60	6.4	5.2	270	270	9.10	6.01
	15	40	60	8.7	8.0	190	190	15.94	20.21

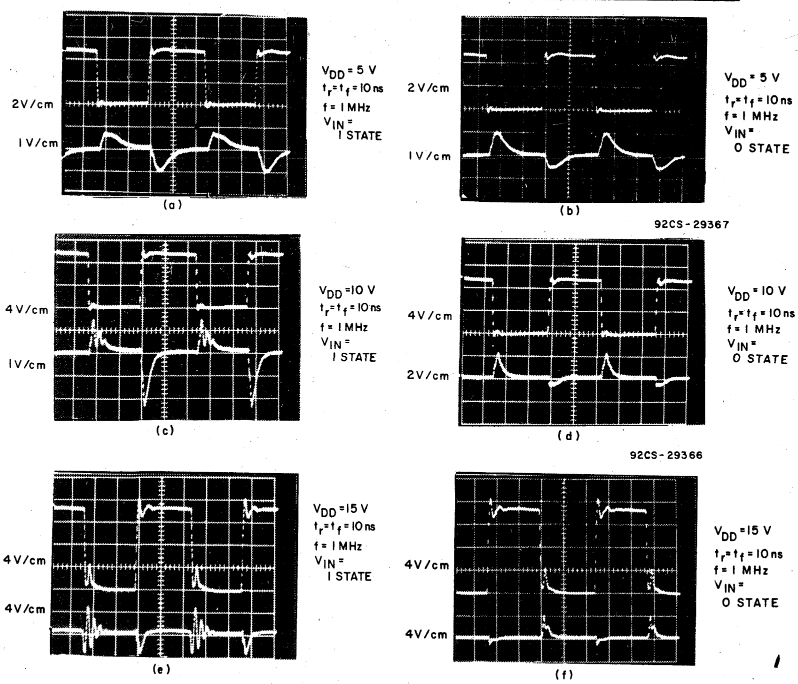


Fig. 23 Crosstalk in the ribbon-cable system.

CONCLUSIONS

The noise-immunity test data demonstrates the high noise immunity of COS/MOS digital integrated circuits. Typical ac noise-voltage immunity for an unbuffered gate is 2 volts for a 5-volt supply, 5 volts for a 10-volt supply, and 7 volts for a 15-volt supply. As expected, the low-level ac noise-immunity for the CD4049UB buffer is slightly lower because of the lower effective input threshold of the large NMOS transistor used.

Of paramount interest is the good noise-energy performance of approximately 1.3 nanojoules for B-series gates, which is comparable to the performance of bipolar TTL gates at 5 volts despite their much higher output drive current. At operation above 5 volts, the noise-energy immunity of COS/MOS devices ranges up to 20 nanojoules at 15 volts, far exceeding the noise-energy immunity of TTL. This improved noise immunity makes CMOS logic devices far more economical to use in high-noise automotive and industrial control environments than TTL devices. This noise-rejection capability exceeds even that of bipolar high-threshold logic, which has only approximately 5 nanojoules of noise-energy rejection in the high logic-input state.

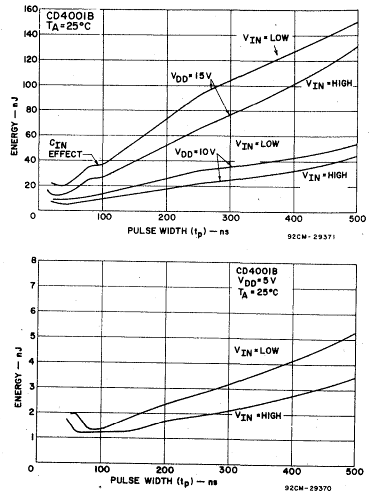


Fig. 24 High- and low-input state noise-energy immunity for the CD4001B gate as a function of input pulse width. $T_A = 25°C$.

The good inherent noise immunity provided by COS/MOS devices leads to design economy, and complements the accompanying benefits of COS/MOS: low-cost, medium- to high-speed operation, wide operating voltage range, good temperature stability, wide selection of SSI, MSI, and LSI device types, etc.

References

1. "Understanding Buffered and Unbuffered CMOS Characteristics," R.E. Funk, RCA Solid State Application Note ICAN-6558.
2. "Noise Immunity of COS/MOS Integrated Circuits," S.S. Eaton, RCA Solid State Application Note ICAN-6176. Discusses noise immunity of A-series devices.
3. "Designing Logic Circuits for High Noise Immunity," Verell Boaen, IEEE Spectrum, Jan. 1973.
4. JEDEC Standard for B-series COS/MOS devices.

Interfacing Analog and Digital Displays with CMOS Integrated Circuits

by J. E. Gillberg

Many forms of displays are available for interfacing digital and analog information from electronic circuits with the individual end user. The display choice generally takes into consideration not only technical feasibility but also visual impact and often aesthetic appeal. Until recently, the analog display, primarily motors (both synchronous and stepper) with gears, hands, or drums, has been the most widely used. At present, however, new developments are making the digital display the more dominant method.

This Note describes some of the COS/MOS integrated circuits most suitable for interfacing the electronic circuit and the display. In the case of digital displays, it describes basic display operation to help simplify the equipment designer's task in selecting both the most appropriate display and the most suitable interfacing device.

Analog Display Drivers

Analog displays are usually driven from either a synchronous motor or a stepper motor. The synchronous motor receives an incoming signal at a frequency of approximately 60 Hz and continuously rotates at that frequency. The stepper motor receives an incoming signal at about 0.5 to 2 Hz and rotates only during the active pulse interval. The stepper motor gives the effect of a non-continuous movement of the motor or wheel.

One of the major users of digital circuits with analog displays is the timekeeping market. This market has continued to use analog displays because of the many basic advantages of the familiar clock or watch face with moving hands. These advantages include low cost, high reliability, simplified electronics, familiarity of display mode, and low current drain.

A number of IC's are available for interfacing the electronic clock circuitry and the analog display. An excellent example is the CD4045, a COS/MOS 21-Stage Counter. As shown in Fig. 1, this device can be used in timing applications not only to generate the crystal oscillator output, but also, because of its output current capability, to directly drive a stepper motor. Fig. 2 gives curves illustrating the current capabilities of the CD4045.

One method of reducing the current drain of a stepper motor is to terminate the incoming pulse at the precise moment the armature achieves enough momentum to rotate to the next position without any additional current. The Low-Voltage COS/MOS Analog Timepiece Circuit CD22010E has the capability of detecting, as shown in Fig. 3, when no additional current is required by the motor. It operates as follows. At the beginning of the output pulse because the load is inductive no current will immediately flow (V = L di/dt) and the voltage at the output will be at ground, as shown in Fig. 4 at t_0. After time, the current will begin to flow into the pull-down n-channel transistor of the CD22010E. This current flow raises the output voltage until the motor begins to rotate and cause a back electro-motive force thereby reducing the voltage at the output. Once the motor has achieved enough momentum to move on its own inertia, however, any added current again raises the output voltage. The time interval from t_0 to t_3 in Fig. 4 is the nominal output pulse. Time t_1 indicates the end of an internal activation period after which any rising edge on the output will trigger internal circuitry to terminate the pulse width, thus saving battery current.

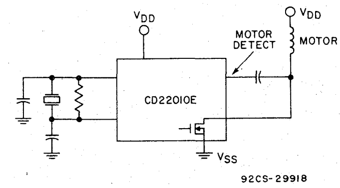


Fig. 3 - CD22010E, a low-voltage COS/MOS analog timepiece circuit, used to detect status of stepper motor current.

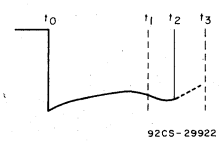


Fig. 4 - Nominal output pulse of stepper motor.

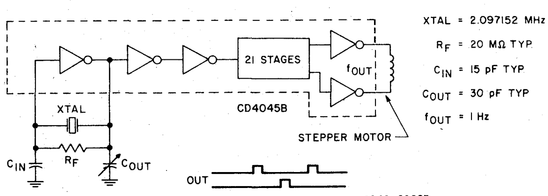


Fig. 1 - CD4045, COS/MOS 21-stage counter, used to generate crystal oscillator output and to drive stepper motor.

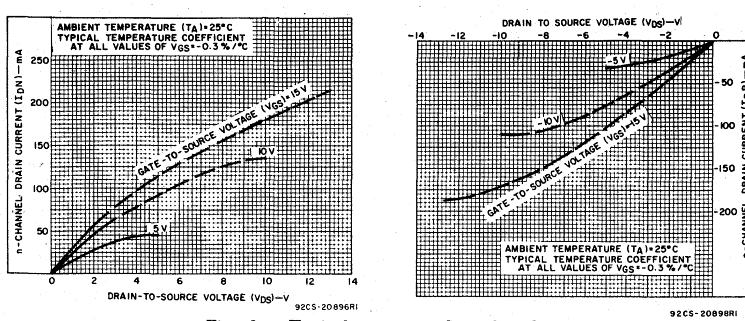


Fig. 2 - Typical output n-channel and p-channel drain characteristics of the CD4045.

The battery-operated wall clock is one of the major areas for analog displays primarily because of the low-voltage (1.5 to 3.0 V typical) and low-current (60 A typical) operation. A number of display interface circuits are available for this application. The most suitable depends upon the type motor and the voltage being used. Several of these circuits are illustrated in Fig. 5. In Fig. 5(c), the capacitor C_D increases the maximum pulse or spike current supplied to the

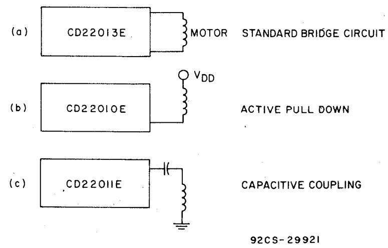


Fig. 5 - Typical motor interface circuits for analog watch or wall clock circuits.

motor. The value of this added capacitor is typically between 1 and 10 microfarads and is dependent upon the frequency of operation.

Many integrated circuits are available from RCA that can be used to interface an analog high-current-drive display. Table I lists several of these devices. For technical data on these devices see the RCA INTEGRATED CIRCUITS DATABOOK SSD-250 or the technical data sheet for the specific device.

Digital Display Systems

With the development of MSI and LSI, digital displays emerged as an important method of information transfer and many new display systems appeared. The most popular or promising types of digital displays are listed in Table II along with a brief summary of their major advantages and disadvantages. In the following material each display system is discussed with the emphasis on adaptability to interfacing electronic circuitry.

Liquid Crystal Displays

The most important advantage of the liquid crystal display is its very low power consumption, typically 50 microwatts per character. The reason for this low power consumption is that the liquid crystal display does not generate or emit light, but controls reflected or transmitted light generated elsewhere.

The liquid crystal display device consists of a layer of liquid crystal material sealed between two conductive-coated glass plates. The liquid crystals are fluids having molecule alignment characteristics very similar to those of solid crystals. The alignment of the molecules can be changed by the application of an ac signal. This change in alignment can produce image patterns determined by the physical construction of the device. Electrical contact is made to the liquid crystal by means of a transparent conductor. Because the image pattern depends upon molecular alignment, the direction which light strikes the liquid crystal is very critical. As a result, light polarizers are attached to the front and back to control whether the display is dark on a light background or light on a dark background. Fig. 6 shows the sandwich-type construction and the arrows illustrate the molecular polarization of a liquid crystal material resulting from an ac field.

There are two basic types of LCD's: dynamic scattering devices and field-effect devices. When an ac field is applied to a dynamic scattering liquid crystal, the molecules which are normally aligned, and hence transparent, are rearranged to scatter any available light, and the display becomes opaque. The field-effect type displays a visual change when the molecule alignment is rotated from one plane to another, as illustrated in Fig. 6. The field-effect liquid-crystal device has become the more popular display.

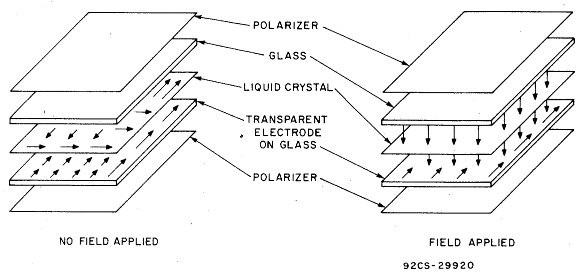


Fig. 6 - Basic operation of field-effect type liquid crystal device showing molecule alignment and major elements.

Two kinds of liquid-crystal devices are available in either the dynamic-scattering or field-effect cateogry: reflective and transmissive. The only difference is that for the former, reflective material is added to the back of the display to reflect the light entering the front. This type is well-suited for applications where substantial ambient light is available. In applications where the ambient light is small, the transmissive display could be used with some form of back lighting.

Liquid-crystal devices require an ac drive signal having no dc component. A dc component can cause an electrolysis plating action which can eventually damage the display. For field-effect displays, this drive signal may be from 2 to 10 volts at 60 to 10,000 hertz; for dynamic-

Table I – Analog-Display Driver and Counter COS/MOS Integrated Circuits

Type	Family Dev. No.	Package	Volts	Freq.	Description
Clocks					
CD22010E	TA6656	8-DIP	1.5	32 kHz	Portescap stepping-motor drive, with pulse-width control (1 Hz)
CD22011E	TA10294	8-DIP	1.5	4 MHz	SOS stepping-motor drive (2 Hz push-pull)
Auto Clocks					
CD22012E	TA6489	14-DIP	12	4 MHz	Quartz analog auto clock (0.5 Hz push-pull)
CD22013E	TA10176	8-DIP	12	3 MHz	Quartz analog auto clock (64 Hz push-pull)
CD22014E	TA6817	8-DIP	12	4 MHz	Quartz analog clock (60 Hz)
CD22015E	TA10177	8-DIP	12	2 MHz	Quartz analog auto clock (30 Hz push-pull)
Industrial Timers					
CD22017E		16-DIP	10		Universal industrial timer

Table II – Digital Display Technologies

Type	Advantage	Disadvantage
Liquid Crystal	Low power, low voltage	AC signal – difficult to multiplex
Light-emitting diode	Low cost, simple interface	High current, visibility
Gas discharge	Easily read	High voltage
Fluorescent	Low segment current, low cost	High filament current/fragile
Incandescent	Brightness, low cost	High current

scattering devices, the signal may be from 7 to 30 volts at 20 to 400 hertz.

When a liquid-crystal segment is activated by a drive signal, the phase relation between it and the transparent electrode applied to the glass backplane is 180° and a visual display results. When no drive signal is applied to the segment, the backplane and segment are in phase and the visual display is off.

The usual method of activating a segment is to apply a square wave which is out of phase with the square wave applied to the common backplane. As shown in Fig. 7, when the segment square wave is in phase with the back-plane square wave, the segment is not activated. By the use of a square wave for both the common (backplane) and the selected segment drive signal, the effective dc voltage across the display is always zero regardless of whether the display is activated or not.

Liquid crystals offer the important advantages of requiring very little power and low voltage. Their disadvantages are:

1. Because they need an ac signal for operation, multiplexing is difficult.
2. They need good ambient light or back lighting.
3. They have a limited operating temperature range: -20 to 60 or 85°C.
4. Their cost in relation to other displays is high.
5. Their response time is slow: 100 to 300 milliseconds.

RCA offers several display drivers for liquid crystal devices: the CD4054, a 4-segment display driver; the CD4055, a BCD-to-7-segment decoder/driver with "display frequency" output; and the CD4056, a BCD-to-7-segment decoder/driver with strobed-latch function. These devices have level-shifting capability for interfacing low-voltage logic signals to higher-voltage display signals. In addition, a full line of direct drive LCD watch chips is available.

Light-Emitting Diodes

The light-emitting diode (LED) has also received wide acceptance as a digital display in the last several years because of its low-voltage operation, long life, ease of multiplexing, high reliability, and fast response time. An LED is a semiconductor diode composed of a p-n junction. In forward-biased operation, because of recombination of holes and electrons, the diodes radiate a colored light in a narrow spectrum. LED displays are normally constructed of either gallium phosphide (GaP) or gallium arsenide phosphide (GaAsP) semiconductor material. Both types of LED displays have approximately equal advantages and disadvantages. The GaAsP type, however, is more prevalent for red displays. The forward drop is approximately 1.6 volts for GaAsP diodes and 2.1 volts for GaP diodes. Two configurations of LED are available: common anode (requiring sink current) and common cathode (requiring source current). Fig. 8 illustrates both types of device.

Any single LED segment is electrically the same as any conventional solid-state diode although the LED does have a slightly higher forward voltage drop. Once the forward voltage reaches approximately 1.6 volts, the current which up to that point has been very small increases rapidly. A typical GaAsP LED needs approximately 5 to 30 milliamperes for a reasonable amount of brightness. If current continues to increase, the LED will reach a light saturation mode at approximately 100 to 150 milliamperes. At this point any increase in current will not increase the amount of light generated. Because the efficiency is greater for higher currents and the electrical and light output rise times are in nanoseconds, LED's are well suited for multiplexed or pulsed output drive. Pulsed output drive can also decrease the total amount of power required to achieve a given brightness by as much as 30 per cent.

As an example, consider the design of a four-digit multiplexed LED display system to interface with a four-digit information storage device. The LED needs an average of 6 milliamperes of current to achieve the desired brightness. Because there are four digits, the multiplexed signal requires a 25 per cent duty cycle. The peak current, therefore, must be 4 x 6 milliamperes to achieve the 6-milliampere average current. The CD4511 BCD-to-seven-segment latch decoder driver is designed with emitter-follower n-p-n bipolar outputs and is therefore able to supply the needed peak current of 24 milliamperes. The digit driver must be able to sink a peak current of 7 x 24 or 168 milliamperes when all segments are turned on. Many available discrete or integrated bipolar devices can meet this requirement. Fig. 9 illustrates a suitable circuit. This circuit uses a CD4511, a BCD-to-7-segment latch decoder driver; CD4052's, differential four-channel multiplexers; CD4094's, eight-stage shift-and-store bus registers; and CD4011 NAND gates.

The multiplexing digit signal, which can also be used to clock a counter to control the CD4052, can be derived by use of a CD4017 as shown in Fig. 10. The CD4017 is a counter/divider having ten decoded outputs. The number of digits multiplexed can be increased beyond four by taking the digit drive from a higher output on the CD4017. The output should be N + 1 where N equals the number of digits to be multiplexed. The CD4017 must be interfaced to a bipolar driver to be able to sink or source the current needed by each digit (168 milliamperes).

Fig. 11 shows a typical digit driving circuit. The calculation of the value of resistor R_1 can be made as follows:

Let β = the gain of the transistor

then $\beta I_1 \geqq 168$ mA

or $I_1 \geqq 168/\beta$ mA

Once V_{DD} is established, a given V_{DS} can be taken from Fig. 11b for current I_1.

Therefore, $R_1 = (V_{DS} - 0.7)/I_1$ kilohms

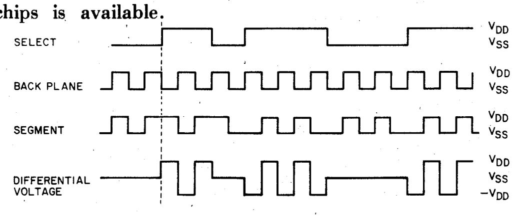


Fig. 7 - Timing diagram of liquid crystal element voltages showing how segments are activated by square waves to avoid damaging effects of a dc component.

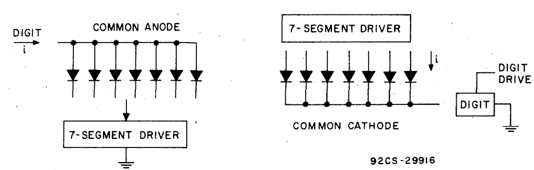


Fig. 8 - Common cathode and common anode light-emitting diode configurations.

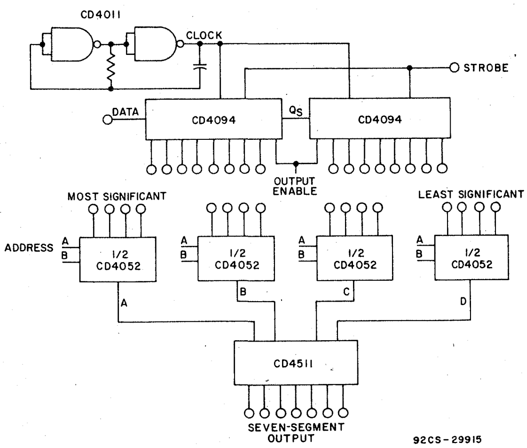


Fig. 9 - Interfacing of four-digit multiplexed LED display system with a four-digit information storage device.

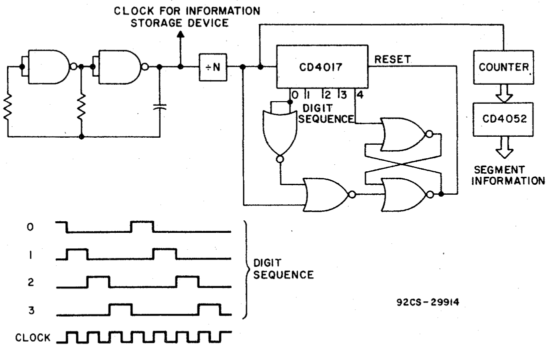


Fig. 10 - Use of CD4017, a counter/divider having ten decoded outputs, to provide the multiplexing digit signal.

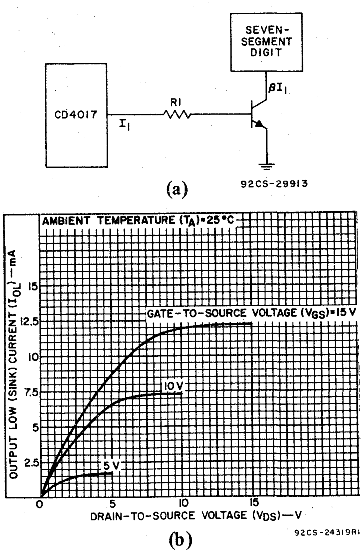


Fig. 11 - Typical digit driving circuit and minimum output n-channel drain characteristic used for calculating value of resistor R1.

Fig. 12 shows the segment and digit drive. Resistor R_2 is necessary to avoid current "hogging" in the LED segments. The value of R_2 is calculated from the curves in Fig. 13 showing output current as a function of output voltage for the CD4511B and from the information supplied with the LED.

Let I_S = peak current in segment

V_{OUT} = voltage out of the CD4511B from Fig. 13 at the V_{DD} being used in the system

V_D = voltage across LED segment for required brightness

V_{CE} = voltage across digit driver transistor

Then,

$$R_2 = \frac{V_{DD} - (V_{OUT} + V_D + V_{CE})}{I_S}$$

In this example

$$R_2 = \frac{V_{DD} - (V_{OUT} + V_D + V_{CE})}{24\text{ mA}} \text{ kilohms}$$

If the value chosen for R_2 is too low, uneven segment lighting can occur. Resistor R_2, therefore, should be as large as possible.

One major drawback to the use of LED displays is that the contrast ratio of the display is very low in bright light. The easiest means of correction is to place an optical filter in front of the LED. This filter increases the contrast ratio of the LED display and makes it easier to read in any ambient light.

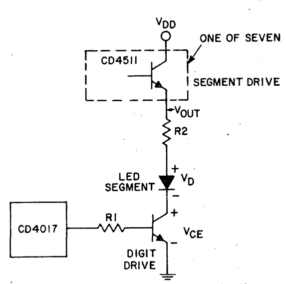


Fig. 12 - Segment and digit drive circuit for LED.

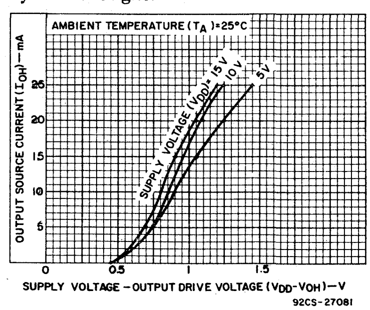


Fig. 13 - Typical voltage drop (V_{DD} to output) vs. output source current as a function of supply for the CD4511.

Gas-Discharge Displays

Gas-discharge or cold-cathode displays are available in both seven-segment and one-of-ten decoded displays. The one-of-ten decoded displays operate by energizing one of a series of stacked cathodes each in the shape of the numeral to be displayed. This stacked arrangement causes some viewing problems because the different numbers appear to move in or out within the display. A CD4028 BCD-to-decimal decoder could be used for the one-of-ten-decoding necessary for this type of device. The seven-segment decoded gas-discharge displays operate in a very similar manner to the seven-segment LED displays mentioned earlier.

One disadvantage of gas-discharge displays is the high potential needed to activate the display. Typically, a voltage between 80 and 200 volts is necessary to cause ionization of the enclosed gas. Once

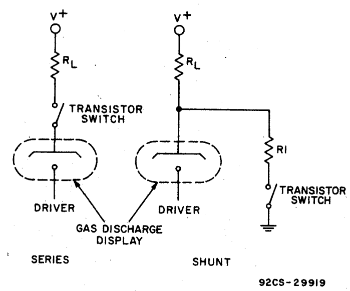


Fig. 14 - Basic series and shunt circuits for multiplexing gas-discharge displays.

ionization takes place, the cathode glows a dull red or orange-like color. In multiplexing these devices, care must be taken to make sure that segments energized for one digit are completely deionized before the next digit is activated.

For multiplexing gas-discharge displays, either the shunt or the series method can be used. See Fig. 14. The series method has the advantage of lower power dissipation, but it requires that the switching transistor have higher voltage and lower leakage than the shunt method requires. Fig. 15 illustrates the multiplexing of a one-of-ten gas-discharge display. Because of diode D1, the oscillator using the CD4011 produces a non-symmetrical output having an off period long enough to assure that all characters are deionized.

Fluorescent Displays

The fluorescent display, like the LED, is a seven-segment device. Its operation is similar to that of a vacuum tube. The major difference is that the anode of the display has a phosphorescent coating which when struck by an electron beam emits blue-green light. Because this light is of a very wide spectrum, it can be filtered with little loss of display brightness. A positive potential of about 15 to 25 volts from anode to cathode is typically used to accelerate electrons emitted from the cathode. When the cathode is activated, the current flow is approximately 0.5 to 2 milliamperes depending upon the type of display.

The potentials of the anode, grid, and filament are crucial in the operation of the fluorescent display. The potential of the filament in the fluorescent display must be directly related to both the grid and anode voltages because the filament is acting both as a heater and as the cathode of the display. The potential at which the electrons are emitted from the cathode or filament, therefore, is critical in determining whether or not those electrons are accelerated toward the phosphor-coated anode.

Advantages of fluorescent display systems include low power, low cost, ease of multiplexing, and ease of interfacing to integrated circuits. A disadvantage is that they are more fragile than many other forms of display because they require an evacuated envelope.

A typical circuit for driving a fluorescent display is given in Fig. 16. The display segments are connected to the anodes of the display device and can be driven directly from any COS/MOS High-Voltage B-Series Integrated Circuit at about 20 volts. In many instances, however, the control logic for the information being displayed is operating at a voltage lower than the 20-volt display supply. In these cases, the CD40109B Quad Low-to-High Voltage Level Shifter can be used to interface the device.

In a multiplexed system, the grid or cathode of the fluorescent display device operates in a manner equivalent to the digit drive on LED devices. A typical grid voltage value necessary to activate the display is 10 volts. If a system is operating below 10 volts, it may be necessary to shift the voltage levels of both the segment and the digit information.

In an unmultiplexed system, the grid voltage should always be enabled to allow the display of the seven-segment information. An example of such a system is given in Fig. 17. Because the grid voltage is constant and not at the control of the system, the only possible level shifting necessary would be for the segment display.

Unlike the LED display, the fluorescent display quite often needs the level-shifting capability of a transistor-inductor flyback circuit to achieve the high potentials necessary for operation. Fig. 18 gives three typical up-converter circuits. The circuit of Fig. 18(a) is pulsed by V_{IN} thus causing a current flow through L. This change in current causes an increase in the voltage across the inductor ($V_L = L \cdot di/dt$). The amount of current ($i_{peak} = V_{DD}/R_2$) is inversely proportional to the value of R_2. With R_2 adjustable in value, the output voltage can be increased by lowering the value of R_2 or decreased by raising its value. Capacitor C_2 filters the voltage spikes caused by the input frequency, and diode D_1 keeps the capacitor charged while the voltage spike from L di/dt is low.

Fig. 18(b) differs from Fig. 18(a) in that it has a self-contained RCL oscillator and obtains its voltage increase by transformer action. The oscillator formed by R_o, C, and L drives the n-p-n bipolar devices forcing an ac signal across the transformer input windings. Because the turns ratio of the transformer from output to input is greater than one, there is an increase in output voltage. The transformer gives a more precise increase in voltage than the circuit in Fig. 18(a) provides. Capacitor C and diodes D and D_Z clamp the voltage V_{OUT} to the breakdown voltage of D_Z and filter and isolate C from discharging during the period of low output voltage from the transformer.

Fig. 18(c) is similar to Fig. 18(b) in the transformer action, but its input is similar

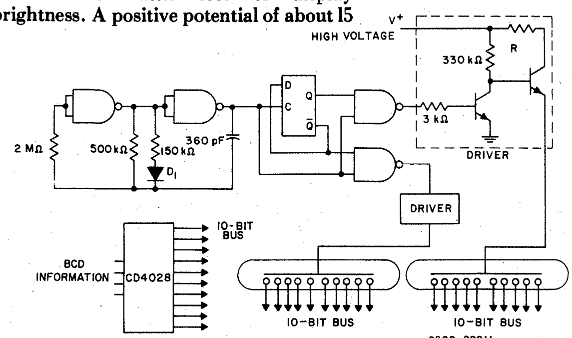


Fig. 15 - Series-type multiplexing of a one-of-ten gas-discharge display.

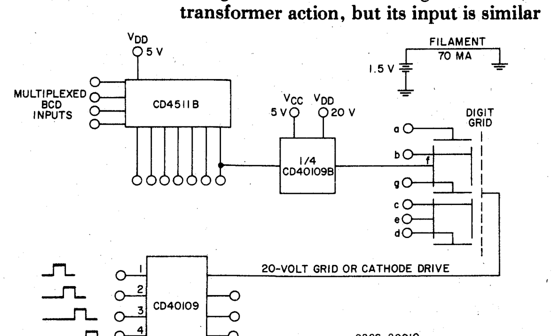


Fig. 16 - Typical circuit for driving a fluorescent digital display.

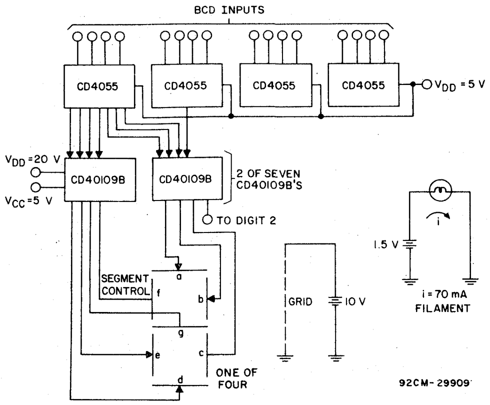


Fig. 17 - Example of unmultiplexed system for driving a fluorescent display.

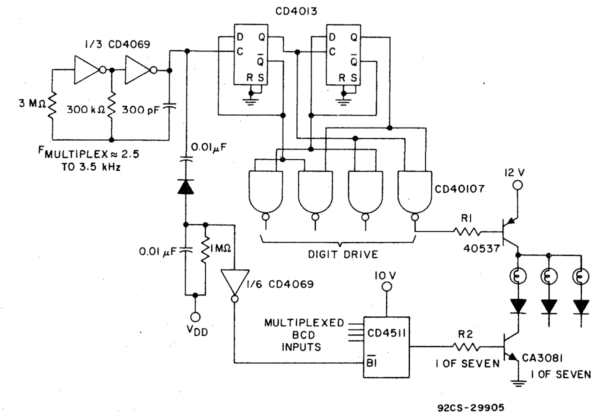
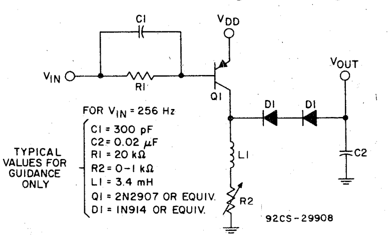


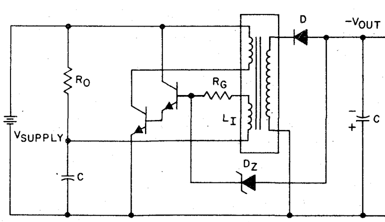
Fig. 19 - Circuit for interfacing a multiplexed incandescent-type digital display.

to that of Fig. 18(a) in that it is driven by an external input.

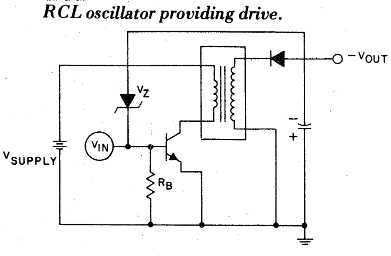
Circuits similar to those in Fig. 18 can be used to level-shift voltages for the gas-



(a) *Pulsed, single-transistor-inductor flyback circuit.*



(b) *Transformer-type circuit with RCL oscillator providing drive.*



(c) *Transformer-type circuit with external drive.*

Fig. 18 - Typical up-converter circuits for fluorescent digital displays.

discharge type of display discussed previously. It is necessary, however, that the transformer, capacitors, transistors, and other components be rated to withstand the 200-volt signals which may be necessary to operate the gas-discharge display and be capable of meeting the higher power requirements.

Incandescent Displays

One other display which has had wide acceptance is the incandescent display. Its low cost, high brightness, and ready availability have lead to considerable use of this display. Its disadvantages are its high power dissipation and the high amount of heat it generates. Typical power requirements are 1.5 to 5 volts at 8 to 24 milliamperes.

Incandescent displays are available in many sizes and colors. Multiplexing of the digits is easily accomplished by pulsing each segment for a given time period. The wattage for an incandescent lamp at the stated brightness remains constant regardless of duty cycle or waveform shape provided that the multiplexing rate is faster than the thermal time constant of the filament. When incandescent displays are multiplexed, an increase in the forcing voltage by an amount equal to the square root of the number of multiplexed displays will maintain the same brightness on each display that it would have in a static condition.

With incandescent displays, it is recommended that diodes be used in series with each segment to prevent erroneous display indication through stray electrical paths. Fig. 19 illustrates the interfacing of a multiplexed incandescent display. In this circuit, the CD4013 dual "D"-type flip-flop combines with the CD4069 oscillator to generate the four pulse intervals needed to multiplex four digits. For a typical incandescent display requiring 4.5 volts, the voltage necessary for the four-digit display is $4 \times 4.5 = 9$ volts. The CD40107 dual NAND buffer/driver and the p-n-p transistor 40537 assure that sufficient current is generated at this voltage. With a typical filament segment current of 50 milliamperes, the current sourced from transistor 40537 is 50 x 7 or 350 milliamperes. The minimum beta of the 40537 is 20. Its base current, therefore, is given by

$$I_{B1} = 350/20 = 17.5\ \text{mA}.$$

At V_{DD} of 12 volts and I_{OUT} of 17.5 mA, V_{OUT} from the CD40107B is 0.11 volt. Then,

$$R_1 = (11.3 - 0.11)/17.5 = 640\ \text{ohms}.$$

For 50 milliamperes in each segment and a β of 40

$$I_{B2} = 50/40 = 1.25\ \text{mA}$$

At V_{DD} of 12 volts and I_{OUT} of 1.25 mA, V_{OUT} from the CD4511B is 11.4 volts. Then,

$$R_2 = (11.4 - 0.7)/1.25 = 8.56\ \text{kilohms}.$$

These calculations depend upon the current gain of each bipolar device and the voltage necessary on the incandescent display. As mentioned previously, the diodes in series with each display segment minimize the possibility of stray leakage currents. Use of the blanking input of the CD4511 assures that if the oscillator were to cease to function for any reason, the indexed digit and segments would not be destroyed by the static voltage and current applied to the display.

Simplified Design of Astable RC Oscillators Using the CD4060B or Two CMOS Inverters

D. Rodman

Application Notes are available that deal with theoretical approaches to oscillator design; this Note stresses practical aspects of design and provides easy-to-use algebraic equations that permit values of R and C for a given oscillator frequency to be quickly determined.

Astable Design Approach

The most basic RC oscillator circuit is that shown in Fig. 1. The time period T for one cycle of this oscillator is given by the equation:[1]

$$T = -RC\left[\ln\frac{V_{DD}-V_{TR}}{V_{DD}} + \ln\frac{V_{TR}}{V_{DD}}\right] \quad (1)$$

where:

V_{DD} = supply voltage
V_{TR} = transfer voltage

By letting $V_{TR} = 0.5\ V_{DD}$, equation 1 can be simplified to:

$$T = -RC\,(\ln 0.5 + \ln 0.5)$$
$$T = 1.39\,RC \quad (2)$$

The problem with this circuit is that transfer voltage can vary from 33 to 67 percent of V_{DD}. Therefore, the maximum variation in the time period, T, can be as high as 9 percent, with a ±33 percent variation in transfer voltage from unit to unit.

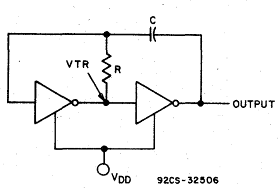


Fig. 1 - The most basic RC oscillator circuit.

An improvement to this basic circuit can be made by adding resistor R_S, as shown in Fig. 2. The resistor makes the frequency independent of supply-voltage variations and reduces the time-period variations to less than 5 percent with variations in transfer voltage.

Rs should be 10 times the value of Rx. If Rs is made less than 10 Rx, the variation in period T increases to about 10 percent as the value of Rs approaches zero.[1] If Rs is made too large, a time constant and phase shift is produced by Rs and stray wiring and breadboard capacitance. This shift creates a switching delay in the circuit which changes the time period.

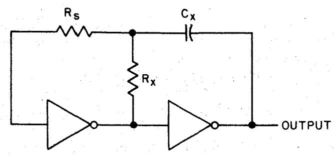


Fig. 2 - An improved oscillator circuit made by adding resistor R_S to the circuit of Fig. 1.

The time period T for the circuit in Fig. 2 is:[1]

$$T = -R_XC_X\left[\ln\frac{V_{TR}}{V_{DD}+V_{TR}} + \ln\frac{V_{DD}-V_{TR}}{2V_{DD}-V_{TR}}\right] \quad (3)$$

If $V_{TR} = 0.5\ V_{DD}$, equation 3 can be simplified to:

$$T = -RxCx\,(\ln 1/3 + \ln 1/3)$$
$$T = 2.2\,RxCx \quad (4)$$

Equation 4 will only be true in the CD4060B for values of R greater than 50 kilohms and for values of C greater than 1000 picofarads. At values of C less than 1000 picofarads, stray capacitance will have a much greater effect on the entire system.

It is advised that a buffer circuit, Fig. 3, be added to the circuit of Fig. 2 to prevent the jitter that would otherwise be introduced into the circuit by noise picked up by connecting cables and by stray wiring and breadboard capacitance. The buffer circuit is not needed with the CD4060B since it has an internal buffer and is internally connected to a counter.

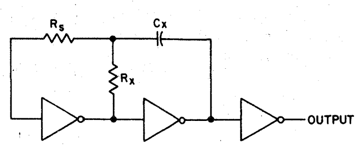


Fig. 3 - A buffer circuit used to improve the performance of the circuit of Fig. 2.

Compensation for 50-Percent Duty Cycle

A true square-wave pulse is obtained only when the transfer voltage occurs at the 50-percent point. If the transfer voltage is at either 33 or 67 percent, the duty cycle will not be 50 percent. The duty cycle can be controlled, however, if part of the resistance of the RC time constant is shunted out with a diode, as shown in Fig. 4.

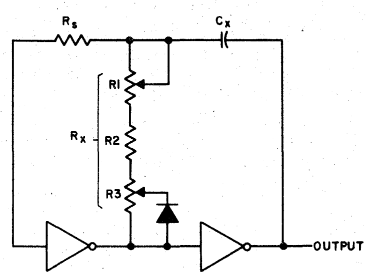


Fig. 4 - Method of controlling the duty cycle of the RC oscillator.

Because adjustment of this diode shunt to obtain a specific pulse factor causes the frequency of the circuit to stray, a frequency control, R1, is added. This circuit is not needed when using the CD4060B since it is used in conjunction with a counter. A 50-percent duty cycle will be derived from the divider/counter outputs.

References and Bibliography

1. "Astable and Monostable Oscillators Using RCA COS/MOS Digital Integrated Circuits," RCA Solid State Application Note ICAN-6466.
2. "COS/MOS 14-Stage Ripple-Carry Binary Counter/Divider and Oscillator," RCA Solid State Data Bulletin File Number 1120.

Abstracts of Other Application Notes

ICAN-6080 . . . . 6 pages
Digital-to-Analog Conversion Using the RCA-CD-4007A COS/MOS IC
The use of the RCA-CD4007A COS/MOS dual complementary pair plus inverter as a digital-to-analog (D/A) switch is demonstrated. The op-amp output stage for the digital-to-analog converter (DAC) uses COS/MOS and bipolar transistor-array IC's. Resistance networks for DAC's, the design of a voltage-follower amplifier for single supply operation, and a 9-bit COS/MOS DAC are described.

ICAN-6166 . . . . 16 pages
COS/MOS MSI Counter and Register Design and Applications
Logic and schematic diagrams for counter and register types CD4006A, CD4014A, CD4015A, CD4018A, CD4020A, CD4021A, CD4022A, and CD4024A are presented; circuit designs are outlined and device-design trade-off's are discussed. Performance criteria are summarized and applications by type are outlined by means of logic or subsystems diagrams and waveforms photographs.

ICAN-6176 . . . . 8 pages
Noise Immunity of COS/MOS Integrated-Circuit Logic Gates
The types of noise usually encountered in a logic system are discussed and the noise immunity of a COS/MOS integrated-circuit logic-gate test circuit in relation to system variables is evaluated. The evaluation is performed on a circuit that includes a CD4000A dual 3-input gate plus inverter and a CD4001A quad 2-input gate connected in cascade to drive a CD4013A flip-flop. Measurement of the voltage required at various gate leads to switch the flip-flop defines the noise immunity threshold of the gate circuits.

ICAN-6210 . . . . 11 pages
A Typical Data-Gathering and Processing System Using CD4000A-Series COS/MOS Parts
This Note is developed in terms of a typical system for process controls. The flexibility of system design and common data-bus architecture made possible by the three-state outputs and bidirectional input/outputs incorporated in many COS/MOS circuits are stressed, as is the ease of system design for data handling in increments of 4 bits made possible by the CD4000A family. The implementation of the system is shown in terms of the COS/MOS standard parts that can be used to perform the desired system functions. Attention is focused on the multiplicity of applications and the scope of information processing that can be covered by standard parts.

ICAN-6289 . . . . 12 pages
A COS/MOS PCM Telemetry and Remote Data Acquisition Design
Descriptive background material on telemetry systems is given along with systems for both immediate and remote data conversion and transmission. Parts from the CD4000 family are used to show how various sections of the system may be realized in the general case. The exact configuration of any specific system will, of course, depend on the unique requirements of the application.

ICAN-6362 . . . . 10 pages
Using the CD4520B to Design Dividers with Symmetrical Outputs
The general-purpose COS/MOS dual up-counter, the CD4520B, a counter that may be used in various counting and dividing applications is discussed. Dividers of the form $N=2^i \pm 1$ and $N=2^i \pm 1$ and described. Applications of symmetrical dividers are also discussed.

ICAN-6374 . . . . 8 pages
The COS/MOS CD4059A Programmable Divide-by-N Counter in FM and Citizens-Band-Transceiver Tuners
The frequency synthesis capability of the CD4059A programmable divide-by-N counter is demonstrated in applications in an FM digital tuner and in the digital tuner for a citizens-band tranceiver. The digital approach described in the paper allows desired frequencies to be selected by depressing numbered buttons on a keyboard. By using the appropriate basic circuitry along with a phase-locked-loop circuit, the local oscillator of the receiver is adjusted and locked to the proper frequency, thus assuring proper station selection. Alternate methods of station selection that enhance the flexibility of the system are described.

ICAN-6498 . . . . 6 pages
Design of Fixed and Programmable Counters Using the RCA CD4018A COS/MOS Presettable Divide-by-N Counter
The use of the CD4018A single-decade and multidecade fixed and programmable divide-by-N counters are described. System considerations such as switch simplifications, components minimization, and speed are also discussed.

ICAN-6600 . . . . 6 pages
Arithmetic Arrays Using Standard COS/MOS Building Blocks
The design of a COS/MOS arithmetic unit capable of adding, subtracting, multiplying, and dividing is described. The device is also able to perform the logical functions of OR, AND and the Exclusive OR of two 4-bit words. Three 4-bit registers are provided that permit either of two words to perform a desired operation with a third word. The system is configured with standard, commercially available COS/MOS devices, which include registers, AND-OR select gates, a full adder, and NOR and NAND gates.

ICAN-6601 . . . . 12 pages
Transmission and Multiplexing of Analog or Digital Signals Utilizing the CD4016A Quad Bilateral Switch
The CD4016A quad bilateral switch is the ideal semiconductor switch for use in switching applications; it can be used for the transmission of analog or digital signals with low distortion. The Note discusses features of the device; operation of the COS/MOS switch; switch and logic applications, including switch and logic functions; multiplexing/demultiplexing; digital control of signal gain, frequency, and impedance, including resistor networks, and variable frequency control; digital-to-analog conversion, including weighted resistor networks for the D/A converter, and an R-2R resistor ladder D/A converter; sample-and-hold applications; and squelch control (level detection).

ICAN-6602 . . . . 12 pages
Interfacing COS/MOS with Other Logic Families
The RCA CD4000A COS/MOS series circuits operate from power-supplies of 3 to 15 volts. Thus, they can drive and be driven by a number of logic families, including all DTL and TTL families, within certain conditions and limitations. This Note describes the conditions of interface.

ICAN-6716 . . . . 15 pages
Low-Power Digital Frequency Synthesizers Utilizing COS/MOS IC's
A digital frequency synthesizer that employs a digital phase-locked loop and other COS/MOS circuits is described. Following a reveiw of phase-locked-loop fundamentals, the use of COS/MOS devices in FM receiver systhesizers is discussed.

ICAN-6733 . . . . 16 pages
Battery-Powered Digital-Display Clock/Timer and Metering Applications Utilizing the RCA CD4026A and CD4033A Decode Counters – 7 Segment Output Types
This Note describes the CD4033A and CD4026A and their use with various 7-segment display units presently available. Interface packages and methods are discussed to help the the designer select the best system to meet his demands. Also included are battery-operated systems for digital clocks and watches.

ICAN-6739 . . . . 12 pages
COS/MOS Rate Multipliers – Versatile Circuits for Synthesizing Digital Functions
COS/MOS rate multipliers, the CD4527B and CD4089B, can be used as building blocks to generate a range of digital functions in low-power systems where minimum package count is desirable. The circuits may be employed in numerical control, instrumentation, digital filtering, and frequency synthesis. When used with an up/down counter and control logic, they can be used to perform such operations as multiplication, addition, subtraction, generation of algebraic equations and differential equations, integration, and to raise numbers to various powers. Symmetric rate multiplication, the problem of eliminating round-off error in a direct frequency-synthesis application in a common-carrier multiplex system is also covered.

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High-Reliability IC Capability

RCA Solid State is a leading supplier of high-reliability integrated circuits to the military and aerospace community. Years of commitment, dedication, experience, and know-how make possible shipment of hundreds of thousands of quality high-reliability microcircuits annually.

RCA specialists fully understand the needs of component and systems engineers in the design of high-reliability equipment, are thoroughly familiar with the objective and requirements of MIL-STD-883 and MIL-M-38510, and work closely with governmental agencies in the establishment of detailed specifications for high-reliability microcircuits. Moreover, RCA Solid State provides complete facilities for processing and testing integrated circuits to these specifications. RCA Solid State is justly proud of its many significant accomplishments with respect to the development, production and shipment of high-reliability integrated circuits, including:

- First supplier of MIL-M-38510 to attain Class S certification
- First supplier of MIL-M-38510 COS/MOS integrated circuits
- Leader in the production of radiation-resistant microcircuits
- Initiator of scanning-electron-microscope (SEM) inspections in the production of high-reliability microcircuits—in use at RCA since 1972
- Initiator of MIL-STD-883, Condition A inspections—in use at RCA since 1972

Standard-Product High-Reliability IC's

RCA offers high-reliability versions of virtually its entire line of standard-product integrated circuits from the CD4000 series of COS/MOS digital logic types, the CDP1800 series of microprocessor and associated memory and input/output (I/O) types, and the CA3000 series of bipolar linear types. These integrated circuits are processed and screened to either MIL-STD-883 or MIL-M-38510 Class B requirements. Extensive inventories are maintained for rapid, off-the-shelf delivery. RCA also offers high-reliability versions of standard-product types that are processed and screened to special customized specifications, especially for the aerospace user and others who procure types to Class S specifications.

RCA solid State maintains an extensive computer file of customer specifications and has the methodology required to translate these customized specifications into internal RCA standards and factory operating procedures. In addition to the detailed device specifications, the computer file lists the customer specification number, any revision number, and the RCA custom number assigned to a specific device type.

Radiation-Hardened High-Reliability IC's

RCA also offers radiation-hardened versions of high-reliability (Class S or equivalent) CD4000- and CDP1800-series COS/MOS integrated circuits. Radiation-hardened types, which are identified by addition of a "Z" or "J" suffix to the device type number, are electrically and mechanically identical to their prototype with the exception that they are processed and screened to withstand a total gamma-radiation dosage of 10^5 rads(Si) for Z-suffix types or 10^6 rads(Si) for J-suffix types.

High-Reliability Custom IC's

RCA Solid State has complete custom-circuit capabilities for various COS/MOS and bipolar integrated-circuit technologies. Custom circuits are offered whenever this approach to integrated-circuit design is determined to be economically feasible. Various custom-design techniques have been developed to meet specific time and volume requirements. RCA high-reliability custom integrated circuits can be processed and screened to MIL-STD-883 Class B specifications.

"RCA High-Reliability Integrated Circuits," RIC-300, provides detailed information on types available, controlled ratings and characteristics, processing and screening schedules, and the reliability levels and classes to which the types in each RCA high-reliability IC product series are supplied.

RCA Solid State

COS/MOS Integrated Circuits